(R)Evolution Towards Solutions Day

Advanced Purge Ready to Rollout

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Abstract

As the More Moore law is going on tight, hunting molecular contamination has become a commitment for Semiconductor Equipment suppliers. This challenge requires a continuous system improvement to fit evolving demands and performance requirements.

How can an SME cope with that permanent Technology Chase, and ride from a scientific concept to a full production line without being jacked by timing, lack of materials, funds, and competition pushing at the gate?

Standing on RECIF Technologies' experience and its Advanced Purge development with a renowned FOUP supplier and tested @ imec within a Collaborative ECSEL Program, we will grasp the decisive impacts of joint collaboration on SME's technologies development:

The origin of the need for development is an issue determined by Entegris, reporting a decreasing purge performance when the FOUP door is off and constraining the user to heighten his N2 consumption to maintain Relative Humidity at the lowest level. RECIF has tested and reproduced this phenomenon and has worked with the consortium on prototype design and tests.

How have the partners ensured their technology deployment by sharing advanced technology research to define a solution simple to implement on existing tools for a smooth deployment and definitely tailored to market expectations with the right timing?

RECIF managed to enhance FOUPs Purge efficiency on its sorter without any N2 consumption excess and thus optimized the cost of ownership. The development steps were monitored and qualified by imec, guaranteeing system's proven ability.

For an SME, Collaborative Projects also provide a solid networking and offer a seamless visibility for the distribution ahead, in this worldwide semiconductor business.

In short, this introduction will expose how being unified into an Industrial consortium can lower the risks and achieve the bridge to a successful deployment.

Biography
Working for RECIF Technologies since 2000, Thomas BRILLOUET has evolved along with the company.

Graduated in electrical and automatic engineering, he then started as a Field Service Engineer for RECIF USA, prior to becoming Technical Coordinator of the East Coast area. Thomas left the USA in 2005, and then successfully managed several Field Task Forces in different Asian countries.
This strong field experience drove him to Development & Project Management. Named R&D Manager in RECIF HQ in 2012 he took in charge products developments since then and committed in multiple European Collaborative Projects, through different frameworks. He contributed in those programs as work-package or task leader from the very first EEMI450 through each 450mm development and demonstration program (NGC450 among them), and TSV-HANDY.

The most Efficient Way to Transport Data

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Abstract

ZeroEC has developed a technology that questions a cornerstone of the IT-Industry: Data Transport. While everyone is looking to increase data bandwidht density, the widely known physical principle of free eletrons in computer devices have not been considerd to be applicable in Semiconductor Products. But ZeroEC developed a technology that uses free electrons for data transport in small scale, which represents the physically most efficient data transport technology.

It will enable to build IT Applications which do not consume energy for data transport and the technology itself can provide up to 1.000 Gbps per channel, at a min. Channel size of 1 nm.

This revoultionary new concept that has been developed in cooperation with world leading scientists from e.g. the Weizmann Institute of Science will build the fundament for green IT and will solve the bottlenecks in data bandwidht density especially for High Performance Computing, Packaging Technologies and many more.

Biography

Daniel Graf is Head of Business Development at 0eC. 0eC presents a revolutionary new way of transporting data based on a physical discovery, discovered by Erez Halahmi and Prof. Ron Naaman from the Weizmann Institute of Science. Mr. Graf is mainly responsible for marketing and investor relations and organises the public presentation of 0eC. Prior to his work with 0eC, he was working in the telecommunication and automotive branch as a system engineer and a freelance IT consultant for more than 10 years, and he has worked in projects for process analysis and customisable system administration. In 2015, he founded a consulting company, Freimuth & Graf Consulting UG, which focuses on methods to build reliable, scalable companies. He has engaged in several startup projects, including AI and app development, where he has implemented agile methods and taken the lead in company building. Through his experience in these projects, Mr. Graf has become an advisor for an investment fund, where he mainly consults in tech investment cases.

In January 2019, he joined ZeroEC as Head of Business Development and started to convert the scientific physical breakthrough that Erez Halahmi's team have achieved into a startup that will change the fundamental principles of data transfer.

A New Quantum Computing Architecture based on Carbon Nanotubes

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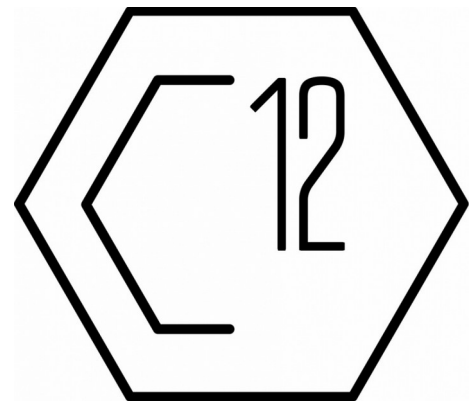
Abstract

C12 develops quantum processors with the goal of speeding-up some information processing tasks. A promising scalable platform for such tasks uses spin qubits coupled to a microwave cavity. The spin has long been recognized as an ideal qubit to store quantum information. Interfacing spins with microwave photons brings interesting perspectives for their individual control and manipulation as well as for the circuit architecture [Science2015].

The qubits stability is essential for scalability, in the mid-term to reach quantum advantage as well as in the long-term to reduce hardware overhead for fault-tolerant computing. A suspended isotopically pure ^{12}C nanotube holds great promises in terms of stability, as it will reduce all sources of decoherence (charge noise, nuclear spin noise, phonon relaxation) [PRL2010]. The goal of C12 is to master the manipulation and the integration of carbon nanotubes to unlock their full potential. C12 will benefit from the expertise on this material developed at ENS Paris and from the newly promising technique of stapling carbon nanotubes [npjQI2019]. If well mastered, this technique brings interesting flexibility for the ambitious tasks of building quantum processors, fully compatible with silicon semi-conductor chips. This will enable to highly integrate it with CMOS technologies for the qubit controls.

Here, we use a circuit QED spin–photon interface to drive a single electronic spin in a carbon nanotube-based double quantum dot using cavity photons. The microwave spectroscopy allows us to identify an electrically controlled spin transition with a decoherence rate which can be tuned to be as low as 250 kHz. We show that this value is consistent with the expected hyperfine coupling in carbon nanotubes.

Biography

Pierre Desjardins is CEO & co-founder of C12 Quantum Electronics. He studied engineering at Ecole Polytechnique, completed with a Master of Science (2013) at Columbia University in quantum physics. He worked as a research assistant in the Quantum Photonics Lab at MIT. From 2014 to 2020, he worked as strategy consultant at Roland Berger, a global consultancy firm. He managed or was involved in 40+ projects worldwide, advising corporate clients and investment funds on strategic and operational assignments. He is now leading C12 to connect quantum power to reality.

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Challenges and Opportunities for Adopting Digital Twins in Semiconductor Industry

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Abstract

To address challenges like rapid yield ramp-up, waste reduction and throughput optimization, advanced process control (APC) came to the forefront in 1990s and became pervasive in the semiconductor industry by 2000s. To deal with similar issues, Industry 4.0 initiative is highlighting concepts like digital twins. Virtualization of a real-life object, process or system is not new; what brings the concept of digital twins to the forefront is its potential real time connection to the real world and leveraging AI and big data analytics to interact with and evaluate different "what if" scenarios.

In this context, we believe that an analysis of opportunities and challenges for its adoption in semiconductor industry is missing.

With our hands on experience with the development of a digital twin solutions framework for semiconductor equipment manufacturers, we share the findings of an analysis on the adoption of digital twins in semiconductor industry.

By replicating manufacturing systems and processes, digital twins afford an opportunity for online and offline support for extending the APC technologies [IRDS2020] like Equipment Health Monitoring for assessing tool health as a function of deviation from normal behavior, Predictive Maintenance for using process and equipment state information to predict maintenance needs, Predictive Scheduling for improving scheduling of system by utilizing current and projected information on tool and factory state, capabilities and schedule, Virtual Metrology for the prediction of post process metrology variables using process and wafer state information, and Yield Prediction for monitoring information to predict process or end of line yield.

The value of digital twins depends on the core perspective of the stakeholder. OEMS and integrators would have an outgoing focus by finding its value for product improvement, customer service and new business models. On the contrary, fabs would have an incoming focus by finding its value for cost reductions, process improvements and safety.

For adopting digital twins, the stakeholders will have to prepare themselves for new challenges. The product teams need to become proficient in both hardware and software by developing new skills like design, simulation, analytics, etc. The integration, management and maintenance of both physical and digital twins would need to be taken into account. Maintenance of digital twins and their links to the physical twins shall become a core approach for upgrades and thus would require new business models.

An additional effort to standardize data interchange, not only between the physical and digital twins but also for the integration of digital twins would be required. With more data from digital twins, unless the stakeholders are able to find innovative "what if" scenarios, its value would remain unclear. The ownership of data is already becoming an important concern. The stakeholders would need to devise procedures for data sharing and partitioning and ensure the confidentiality of data and intellectual property security.

Finally, it is important that SEMI association participates in the development of a consensus around the use of digital twins and specifies standards that can help for digital twins integration.

Biography

Fahad Golra is working as a research coordinator at Agileo Automation, France. He did his doctorate from

IMT Atlantique, France in the domain of software process modeling. His research focuses on the problems associated with the development of complex software systems. He is currently involved in research on modeling methodologies for interoperability in industrial software systems. His research interests are Industry 4.0, industrial automation, semiconductor fabrication standards & methodologies, OPC UA architectures, Model Driven Engineering for systems and processes. He is involved in various working groups of OPC Foundation for the development of companion specifications.

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