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Materials Day

Strategies for Doping 2D Transition Metal Dichalcogenides: Atomic Layer Deposition of *p*-type Al-doped MoS_2

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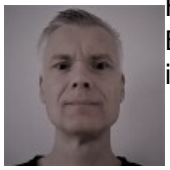
Abstract
Two-dimensional layered transition metal dichalcogenides (TMD) such as MoS_2 and WS_2 are of interest for nanoelectronics because of their promising electronic characteristics and their predictable properties even in the few- and monolayer regime. The merits of TMDs for transistor applications have already been demonstrated by fabrication of field-effect transistors (FET) mainly using intrinsic TMDs (*i.e.* without intentional doping). However, doped variants of these TMDs are essential for the fabrication of high-performance devices and the realization of advanced transistors concepts. The fabrication method of these doped TMDs has to be compatible with large area deposition and scalable to allow adoption in device fabrication workflows.

In this presentation, the most promising approaches towards doped TMDs will be briefly reviewed with an emphasis on semiconductor fabrication compatibility. In particular, the synthesis of Al-doped MoS_2 by plasma-enhanced atomic-layer deposition (ALD) will be discussed as this process demonstrated the highly sought after *p*-type behavior, widely tunable electronic properties, and excellent control over the carrier density. Going beyond control over carrier density, the control over the doping profile on the nanometer scale - made possible by this ALD based approach - was highlighted by cross-section transmission electron microscopy (TEM) imaging and energy-dispersive X-ray spectroscopy (EDX). Compatibility with semiconductor fabrication is ensured by the conformallity, uniformity, low deposition temperature (< 350 °C), and the sub-nm thickness control inherent to ALD. To conclude, the scalable synthesis of doped TMDs with good control over the electronic properties is key for future TMD based nanoelectronics but these materials are also desirable in other fields including photovoltaics, catalysis, and energy storage.

Biography
Vincent Vandalon is a post-doctoral researcher in the Applied Physics department of the TU/e. He obtained his MSc and PhD in Applied Physics from the Eindhoven University of Technology focusing on nonlinear optics to study the growth of metal and metal-oxide atomic-layer deposition (ALD). For this work he received the American Vacuum Society (AVS) ALD-conference best paper award in 2015. After obtaining his PhD in 2017, his area of research shifted towards the growth and characterization of 2D transition-metal dichalcogenides (TDMs) with a special interest in alloys and doped TMDs for nanoelectronic applications.

InGaZnO4, a New Material for Nano-electroncs



H. Dekkers
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Abstract
Oxides of the Indium-Gallium-Zinc family are a semiconducting material with a high band gap, a carrier concentration that is exclusively n-type, and a relatively high mobility. With those properties, $InGaZnO_4$ (IGZO) achieved its merits as a transparent channel of thin film transistors (TFT) for electronic flat panel displays (FPD). Relative high electron mobilities are maintained in the amorphous phase which enables scaling of TFT's resulting in a significant increase of FPD resolution. The lack of mobile holes decreases the leakage current of the TFT dramatically, which enables the refresh time of still image data and therefore lowers power consumption.
Longer refresh times are also attractive for memory switches. For example, one application is the low leakage terminal transistor in DRAMs. Relatively low deposition temperatures allow IGZO TFTs to be integrated in the back end of line (BEOL). This possibility enables several scenarios for added functionality to memory and logic circuits using 3-D stacking. Challenges for this integration is the suppression of oxygen scavenging by subsequent process steps. Imec is looking into several options to improve the stability if IGZO by engineering the crystal phase. Spinel IGZO is one candidate which can be engineered using atomic layer deposition (ALD) or pulsed-DC physical vapor deposition (PVD).

Biography
Hendrik F.W. (Harold) Dekkers graduated for industrial engineering in applied physics at the HTS Dordrecht (The Netherlands) in 1994. After working for the semiconductor equipment vendor ASM he joined the research group of silicon photovoltaic devices at IMEC in Leuven (Belgium) in 1999. There he contributed to the development of vacuum process techniques for silicon solar cell manufacturing. In 2008 he received his Ph.D. (Electronic engineering) at the Catholic University of Leuven (KUL) on this topic. In 2007 he joined the Thin Films group of imec, being responsible for the plasma-enhanced CVD processes in the front-end-of-line (FEOL) of IC manufacturing. Since 2011 he contributes to the development of work-function metals of metal gate stacks as a part in the replacement metal gate program of IMEC. Currently he is involved in the development of semiconductor oxides for several applications in nanotechnology.

Heterogenous Integration – A key enabler for electronic systems

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Abstract
Heterogenous integration through SiP (System-in-Package) can leverage the advanced capabilities of packaging technology to create systems close to the SoC form factor but with better yield, lower overall cost, higher flexibility, and faster time to market; the latter has especially shifted the paradigm from SoC-centric to SiP-centric in the recent past even for volume products. This presentation highlights the market needs, technology paths, difficult challenges and potential solutions when addressing high-density system integration with advanced packaging materials, tools and techniques, with projections on required developments over the next 10 to 15 years.

Biography
Rolf Aschenbrenner received the B.S. degree in mechanical engineering from the University for Applied Science, Gießen, Germany, in 1986 and the M.S. degree in physics from the University of Gießen, Germany, in 1991. From 1991 to 1992 he has worked at the University of Gießen and in 1993, he joined the Research Center for Microperipheric Technologies at the Technical University of Berlin. Since March 1994 he has been employed at the Fraunhofer Institute for Reliability and Microintegration Berlin (IZM) where he is presently the Deputy Director and Head of the Department System Integration and Interconnection Technologies.
He received the iNEMI International Recognition Award in 2005, the CPMT David Feldman Outstanding Contribution Award 2013 and the European Semi Award 2016.
As a member of the IEEE EPS Society Board of Governors Rolf Aschenbrenner has worked as a European representative on the Conference Advisory Board Committee, and has played an active role in the globalization of IEEE EPS in terms of membership and chapter development. He served as IEEE CPMT Vice President, Technical and IEEE EPS Vice President, Conferences. From January 2010 until December 2011 he was IEEE EPS President and in 2012 he became IEEE Fellow.

Thin Film Processing of Innovative Ionic Synaptic Transistors for Neuromorphic Applications

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Abstract
Recent hardware developments have enabled the successful application of new computing techniques based on artificial intelligence (AI) concepts to diverse domains. Currently, all these applications rely on CMOS implementations of AI algorithms, taking advantage of either deep (DNNs) or spiking neural networks (SNNs) where layers of artificial neurons are connected to each other via synaptic elements characterized by a weight factor. Recently, developments in nanoscale ionic/electronic transistors mimicking electrochemical principles at the biological synapse level have spurred a great interest in achieving powerful neuromorphic computing systems.

In this context, it is expected that the development of novel channel (intercalation host) and solid state ion conductor (electrolyte) materials as well as interfacial engineering at the gate stack level would provide opportunities to enhance the device performance and widen the scope of possible integration schemes. Several options have been explored at LETI, including key enabling technologies such as physical vapor deposition, atomic layer deposition as well as a combination thereof. Here we will discuss our recent efforts to develop advanced cation based intercalation and conductor materials for synaptic ion transistors.

Biography
Sami Oukassi received his PhD in electrochemistry in 2008 from Paris XII University, France. He is currently a full-time researcher at the CEA-LETI. His current research interests include the development of thin film devices based on solid-state ionics, with a focus on energy and data storage. He is author of 15 publications and holds 35 patents.