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Advanced Packaging Conference (APC)

S. Kroehnert
President and Founder
ESPAT-Consulting - Steffen Kroehnert, Dresden, Germany

Biography
Steffen Kroehnert is President & Founder of ESPAT-Consulting based in Dresden, Germany. He is providing a wide range of consulting services around Semiconductor Packaging, Assembly, and Test, mainly for customers in Europe. Until June 2019, he worked for more than 20 years in different R&D, engineering, and management positions at large IDMs and OSATs in Germany and Portugal, namely Siemens Semiconductors, Infineon Technologies, Qimonda, NANIUM and Amkor Technology, where he most recently served as Senior Director Technology Development. Since 2016 Steffen has chaired the European SEMI integrated Packaging, Assembly, and Test - Technology Community (ESiPAT-TC). Steffen has authored or co-authored 23 patent filings and many technical papers in the field of Packaging Technology. He also co-edited the book “Advances in Embedded and Fan-Out Wafer Level Packaging Technologies”. He is an active member of several technical and conference committees of IEEE EPS, IMAPS, SEMI Europe, and SMTA. Steffen holds an M.Sc. in Electrical Engineering and Microsystems Technologies from the Technical University of Chemnitz, Germany.

Packaging in Europe - Micro Balling on Chips with a High Ball-count for Space Applications - an Extension of the Process Capabilities at AEMtec

D. Negrea
SVP New Technologies
AEMtec GmbH, Berlin, Germany

AEMtec

Abstract
Packaging in Europe – and not in Asia - seems a strange business model. But it is not, if you consider the technology IP aspects, the challenges, the drive of some European industries (mainly the space industry) towards emancipation from the dominance of the US and Asian providers.

AEMtec started the internalization of the Wafer Back End solder balling technologies for 4 years and

increased permanently the portfolio of customers and products, mainly in the high sensitivity products, considered by our European customers and strategically critical to their business. The vision of a one-stop-shop for core technology products, for small and medium quantities became reality.

The requirements specific to the "New space" projects target in the first line the cost reduction of all components but without compromising on the required quality and performance.
The drive to miniaturization, considering the costs of the payload for satellites, leads to the use of chips with a high Ball count (whereby 5000 and more are rather the rule than the exception).
We like to focus in our presentation on the challenges, both from a technical as well as from a regulatory perspective for the use of the non-hermetic, soldered, flip chip technology for space applications on the technological, down-to-earth, explanations concerning the implementation of the wafer back end processes.

AEMtec actively participates in different projects and workgroups around ESA.
By qualifying in house processes, having extremely stringent requirements in terms of reliability, AEMtec can guarantee very high Cpk levels for all relevant processes, followed in the SPC.

The level of quality which needs to be achieved for the space applications, opens the way to multiple other types of applications, including high density large size chips for companies active in the detection technology, but also for applications in the automotive industry.

So far the achieved performances of the wafer back end solder bumping line, which comprises all the necessary stages of the process, from wafer inspection to balling, washing, dicing, and which has been validated on multiple tens of thousands of chips, allow the use of micro balls with a diameter of 50 µm, on chips with up to 12,000 connections.

Of course this miniature size of balls and the physical size of the chips cause a high unitary stress/strain on the balls, due to the difference in thermal coefficient in normal use - therefore the major importance of the cleanness and of the underfill processes. The tests performed for the qualification go far beyond the normal RTV cycles, thus guaranteeing a flawless quality.

Biography
For information purposes only

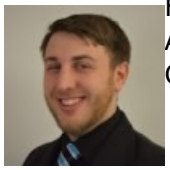
A New Approach for IR Failure Analyses of Components with Low-emissivity Surfaces without Blackening

D. Wargulski
Scientific Staff Member
Berliner Nanotest und Design GmbH, IR Thermography, Berlin, Germany

Abstract
Failure analysis and quality assessment are crucial for the production of electronic devices and components. In contrast to conventional methods such as scanning acoustic microscopy (SAM) and X-ray, Infrared thermography (IR) enables an analysis without the need of a liquid coupling medium, as necessary for time-consuming SAM analyses, and it enables the detection of delamination, a frequently occurring defect for solder or sinter joints, which is in general not detectable by X-ray.
Pulsed Infrared thermography (PIRT) is a very fast and non-destructive testing technique and commonly used for the inspection of large production parts such as composites, but it can be used as well for the detection of defects in die attaches in electronic components.
For precise temperature measurements by infrared thermography, especially for rather small thermal signals, it needs surfaces with high emissivity. Reflective surfaces such as metallized die surfaces usually are spray-coated with black, high-emissivity coatings to measure temperature distributions using an IR camera.
As spray-coating contaminates the devices and components, it is not widely accepted. The drying process of such coatings takes time and the necessary removal without residues after the inspection is an extra time-consuming effort. That's the main reason, why IR failure analyses have not established yet for die attach and other thermal joints inspection in the electronics industry.
We will present a procedure and a device for fast and automatic IR inspections of electronic components without sample preparation by spray-coating even on samples with reflective and low emissivity surfaces. This technique is based on a film lamination process, where the film can be automatically applied and removed within seconds. It enables 100% inline inspection of sintered and soldered electronic components.

Biography
Dan Wargulski completed his master's degree in physics in 2015 at the Technische Universität Berlin and his bachelor's degree at the Freie Universität Berlin in 2012. From 2014 to 2016 he worked as student assistant at the Helmholtz-Zentrum Berlin on material characterizations of novel materials for photovoltaic applications. Since 2016 he is full staff member at the Berliner Nanotest und Design GmbH and responsible for IR failure analyses, development of the failure analysis systems and thermal and electrical characterization of bulk materials.

Aerosol Jet Printed Interconnects: Benefits and Performance Characterization



K. Homan
Applications Engineer
Optomec GmbH, Dubendorf, Switzerland

Abstract
More than 90% of the chip interconnections produced annually, more than 15 trillion wires, are produced with wire bonding. While low cost and reliable, wire bonds are not ideal in all situations. In Z-limited applications such as memory cards and cell phones, the 70 um loop height can consume a significant part of the device height budget. Also, the small diameter wires elevated over the device can result in increased inductance and reduced capacitance at the connection causing unwanted reflections in RF signals, especially those approaching mmWave frequencies. Additionally, potential mechanical damage to the semiconductor's sensitive bond pad structure limits the placement of active circuitry under the bond pad and necessitates the use of thick metal pads or more advanced wire bond recipes with narrower bonding parameter windows, and typically slower UPH to prevent cratering. Finally, the wire bonding process is very likely to crack future thin, flexible die (e.g. <10 um thick) on compliant substrates.

Printed interconnects have the potential to provide improvements in all these areas, by conformally connectorizing die bond pads at different levels. The work to be presented will show test structures used to demonstrate RLC performance as well as reliability data on several different conductor inks and dielectric insulators printed with Aerosol Jet. These will be used to create transitions from substrate to die and die to die connections. The overarching goal of the work is to demonstrate a reliable, high performance interconnect method which can be used by chip designers and back end chip packaging houses to reduce overall XY footprint, minimize Z height, enable double sided heterogenous integration without wire bonds & enable new packaging form factors not previously possible.

Biography
Mr. Homan is an Applications Engineer for Optomec GmbH based in Dubendorf, Switzerland at the EMPA campus. Mr. Homan provides product and application support to Optomec's European customers as well as coordinating closely with the US team on technology and material advances. Prior to joining Optomec in 2018, Mr. Homan received his MSEE in 2015 from the University of Massachusetts Lowell and worked as a researcher for the Printed Electronic Research Collaborative (PERC) and Raytheon Umass Research Institute (RURI) focusing primarily on printed RF electronics.

Innovative Microstructures in Glass for Advanced Packaging Applications

R. Santos
Technical Sales Manager LIDE
LPKF Laser & Electronics AG, Garbsen, Germany

Abstract
Glass is not a new material in packaging applications and related technologies, however, its use is still very limited. Despite its low material cost and incredibly interesting properties, traditional glass micro processing technologies inevitably increase its price while negatively affecting the characteristics of glass that made it initially interesting.

Developed by LPKF Laser & Electronics, Laser Induced Deep Etching (LIDE®) is a processing technology which enables reliable, high precision and high aspect- ratio micro structures in glass. After LIDE® processing, the glass is completely defect-free (no cracks, induced thermal stress, etc.) and retains all of its properties. LIDE® consists of a two-step process: i) a maskless, direct-writing laser process that only requires a single pulse to modify the whole glass thickness, and ii) a wet etching process done in batch. In summary, LIDE® is an incredibly economical technology capable of processing functional glass for microelectronics and enabling its full potential for advanced packaging applications.

In this work, we will demonstrate how LIDE® unlocks the use of glass for RF applications by taking full advantage of fused silica's low transmission loss and by enabling the creation of metallized paths in glass connected to through glass vias (TGV). This paper also presents the making of high aspect-ratio glass interposers for more affordable 2.5D architectures and the formation of spacer wafers with high-accuracy openings of any shape. We will also show advanced capping wafers with anisotropically-etched straight sidewalls that significantly increase their die density and the use of glass springs for high precision passive die alignment features. Finally, high quality, high throughput and hence cost-effective dicing/singulation of glass wafers will also be introduced.

Biography
Rafael Santos completed a MSc. in Materials Engineering at NOVA in Portugal and developed thermoelectric materials for his PhD in Wollongong, Australia. In September 2019, he joined LPKF Laser & Electronics AG, in Germany, as a Process Development Engineer for the Laser Induced Deep Etching (LIDE) technology. Recently, Rafael was assigned the position of Technical Sales Manager for LIDE.

Maskless Lithography Optimized for Heterogeneous Integration

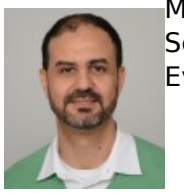
B. Matuskova
Business Development Manager
EV Group (EVG), St. Florian am Inn, Austria

Abstract
Moving from monolithic to the second and to the third dimension is becoming increasingly important within industry trends. Heterogeneous and chiplet integration making use of advanced packaging technologies have increased in complexity over years as well as in number of options. The vision of improving the device efficiency and system computing and communication performance necessitates faster data processing as well as lower communication latency. Additionally, higher bandwidth and lower power consumption requirement drives the approach toward 3D integration, whereas the need of finer RDL line/spacing as well as smaller µbumps and µpillars critical dimension delineates integration design rules at package and substrate level too. An individual chiplet's I/O bumps and interconnects pitch scaling moves typically toward 2/2µm L/S. Although partitioning of larger dies into smaller chiplets re-integrated from various technology nodes has shown numerous advantages over monolithic based SoC technologies, this approach still represents certain optimization challenges for lithographic patterning processes. A profound evaluation of high resolution thin and thick resists typically used in advanced packaging for RDL & µbump/µpillar creation is shown in this work with the aim of employing maskless exposure method and presenting its patterning performance capability. Generated results comprising resolution tests, focal position & exposure matrix including resist sidewall profiles are discussed in respect to the heterogeneous integration requirements fulfilling fine 2/2µm L/S. Nevertheless, the importance of design flexibility and the ability not only to adopt both die- and wafer-level designs simultaneously but also the viability of fast tapeout changes is addressed in order to cover the scope of application for wide range of packaging technologies.

Biography
Bozena Matuskova is business development manager at EV Group, where she is focused on advanced packaging market, especially lithography solutions including maskless exposure, precision mask alignment and resist processing systems.

Bozena holds a master's degree in Microelectronics from Slovak University of Technology and has 8+ years of professional experience in engineering, business development and technical product marketing activities, in both semiconductor & automation engineering industry.

Pushing Boundaries in Ultra-thin Flexible Substrate-like PCB Manufacturing



M. Elghazzali
Senior Scientist
Evatec AG, Trübbach, Switzerland

Abstract
Evatec AG, Switzerland: Scientist Mohamed Elghazzali, Roland Rettenmeier
in cooperation with GS Swiss PCB, Switzerland

To cope with requirements of the next generation medical devices and implanted electronics, feature densities, substrate thicknesses and substrate materials are pushing boundaries of the state of the art.

Process and application teams from Evatec and GS Swiss PCB collaborated over the past two years to develop a robust manufacturing solution for sputtered seed layers and the subsequent processes (resist lamination, electro-plating, etc.) on ultra-thin substrates (down to 12µm thin). The main focus was to maximize the adhesion for the deposited titanium/copper seed layer in combination with the subsequent processes,
all under the very demanding reliability requirements from GS Swiss PCB and their customer (reflow, HAST, peel tests, etc.).

Evatec's outgassing method and surface-treatment technology, RIE (Reactive Ion Etching), Ar-sputter Etching and sputtering capability is the established POR for Panel Level Fan-Out.

The Evatec and GS Swiss PCB teams worked together to solve the below mentioned challenges:

What are the best polymer materials capable of fulfilling customer's performance specifications?
How could these thin foils be handled safely for the complete process flow without additional cost for changing the existing fabrication systems?
What plasma surface treatment/cleaning is necessary to create the best interface to the subsequent adhesion layers?
How to optimize thermal management, surface treatment, deposition process for the best adhesion promoter and reliable seed layer?
How to integrate this new process into the existing IC-substrate manufacturing?
This joint JDP lead to outstanding results and demonstrated that varying pretreatment and process conditions had a big impact on the adhesion results. Equally important however, was the optimization of the overall process along pre-treatment, metal film deposition and managing to handle the very thin and flexible substrates.

Biography
Mohamed Elghazzali has over 20 years of professional experience in the development of vacuum deposition systems and its processes. After he obtained his diploma on Material of Science in Erlangen-Nürnberg, (Germany), he worked several years for Ceramics and Glass Industries and developed new ways to improve fiber glass production at Glasseiden, Oschatz.
Mohamed joined the R&D department of the thin film division of Oerlikon in 2000. As a project leader for numerous innovation projects, he was responsible for the development of components and processes for the Semiconductor, MEMS and the Advanced Packaging Industry. Since 2015 he holds a Senior Scientist position at Evatec AG. In 2018 Mohamed joined the FO-PLP and IC-Substrate development processing

system team within the Advanced Packaging Business unit of Evatec.

FHE Manufacturing Technologies to Reduce Assembly Thickness

M. Grooten
Managing Director
DoMicro BV, Eindhoven, Netherlands

Abstract
In the quest for size reduction, stepping outside the die-in-package approach meets many practical challenges: EMS lines mount packages, not dies, and SiPs still need a board. The FHE approach combines packaging and pick&place functionality into a set of assembly processes, enabling ultra-thin and flexible assemblies, giving space to new product designs.

The set of assembly processes DoMicro is showing comprises thinned die handling, die bonding and die interconnect. Passives integration is discussed as well.

Starting from a flexible PEN substrate, DoMicro presents experimental work on die handling of thinned dies, both for the die-first and the die-last approach. A process for die bonding in a die-first sequence on a flexible substrate is then described and characterised.

Ink jet printed interconnects for dies on foil is shown as a FHE alternative to wire bonding or lithographically manufactured interconnects. Various technical challenges related to alignment, accuracy, routing and reliability are addressed. Also, bumping is discussed. As an alternative FHE technology, die-last bonding with anisotropic conductive adhesive is shown and characterised.

With the presented technology, a functional assembly with a thickness below 200 µm is realized and demonstrated.

Biography
As Managing Director for DoMicro BV Marcel Grooten MSc. drives the industrialisation of new production technology for hybrid electronics. Previously he acted as independent consultant with respect to industrialisation projects and operational management. After graduation (ME) he started his career within Royal Philips Electronics NV, acquiring skills in equipment engineering, project management, human resources and operations. Hereafter he has been engaged in several start-up companies performing

operational and turn-around management in high tech industry including data storage, solar, semicon and printing. His leadership and entrepreneurship is based on many years of profound knowledge and experience in international networks.

An Ultra-thin and Multilayered Parylene based Printed Circuit Board with a High Flexibility

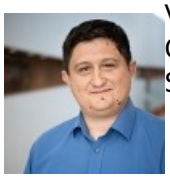
F. Selbmann
scientist
Fraunhofer Institute for Electronic Nano Systems,
Chemnitz, Germany

Abstract
Following the ongoing trend towards the Internet of Things and Industry 4.0, flexible electronics and sensors are a key enabling technology for the realization of geometry adaptive devices and wearables. However, besides the components themselves, also flexible packaging technologies, i. e. flexible printed circuit boards (PCB) have to be established. A variety of different technologies for the realization of flexible PCB are currently under investigation or already established. However, they feature still a comparably high thickness. We present a new approach for the fabrication of highly flexible PCBs, which features an ultra-low thickness at the same time. Doing so, Parylene acts as the substrate as well as the encapsulation and protection layer, respectively. The ultra-thin flexible Parylene PCB can be fabricated with multiple metallization layers, which are connected by vias. For the realization of the PCB standard microsystem technologies are applied. Doing so, a minimum structure size of 10 µm was realized up to know. Between two metallization layers Parylene is used for the dielectric isolation. The total thickness of the ultra-thin flexible PCB is 20 µm or even less, depending on the number of metal layers. Due to the unique properties of Parylene, i. e. chemical inertness, optical transparency and ISO 10993 certified biocompatibility, the obtained PCBs can be used in harsh environments, for the integration of optical components or for medical applications. Thus, a versatile new platform for the realization of highly flexible electronics, sensors and devices is created for a variety of different applications. The presentation includes the concept of this new approach, the fabrication technologies as well as possible application scenarios.

Co-authors: Frank Roscher, Maik Wiemer, Thomas Otto, Yvonne Joseph

Biography
Franz Selbmann studied Electronic and Sensor Materials at the Technische Universität Bergakademie Freiberg and completed his masters degree in 2015. He worked in solar cell development at SolarWorld Innovations GmbH. Since 2015 he works in the field of biocompatible packaging and material integration at the Fraunhofer Institute for Electronic Nano Systems ENAS in the department System Packaging. Since 2019 he is head of the group “Flexible Devices” at the Institute for Electronic and Sensor Materials at TU Bergakademie Freiberg

Ultra-Thin Capacitors with Carbon Nanofibers with High Capacitance Density



V. Desmaris
CTO
Smoltek AB, Gothenburg, Sweden

Abstract
Advanced packaging is primarily considered to enable further size reductions, increase of the cost efficiency and multifunctionality by utilizing System on Chip (SoC) and System in Package (SiP) solutions. As a result, there is a rising need for on-chip, or in-package, capacitors to be used, not only in traditional integrated circuits, but also for integrated components on interposers. High-density capacitors with small footprint and low-profile height are therefore in high demand, e.g, for when implementing integrated power delivery networks and enabling efficient decoupling and noise suppression in close vicinity to the active component. We present miniature MIM capacitors with carbon nanofibers (CNFs) as electrode material featuring ultra-high capacitance densities together with an unprecedented ultra-thin form factor. The performance of the capacitors (CNF-MIM) can be tuned, depending on application. Taking advantage of the large 3D surface featured by vertically aligned and tightly spaced carbon nanofibers directly grown on the capacitor's electrode, capacitance densities (per device footprint area) in excess of 650 nF/mm^{2}have been achieved at a profile height of only 7 µm. In addition, Also, this truly solid-state, 3-D integrable, on-chip CNF-MIM have shown breakdown voltages up to 25V.
CNF-MIMs with capacitance densities of about 500 nF/mm^2 exhibits leakage currents typically below 0.004 nA/nF at 1V, while sustaining voltages up to 6 V. The CNF-based capacitors also retain their remarkable capacitance density against voltage and temperature variations. In addition, equivalent series resistances and inductances lower than 40 mΩ and 6 pH, respectively, have been measured. The results strongly support the potential for CNF-based solid-state capacitors to compete with established high capacitance density technologies and the suitability of such capacitor for on-chip solutions as well as in discrete electronic applications at a minimal component volume.

Biography
Vincent Desmaris received a MSc in Material Science from the Institute of Applied Science, Lyon France (1999). He received a PhD in EE from Chalmers University of Technology, Gothenburg, Sweden (2006). His thesis concerned the fabrication, characterization, and modeling of AlGaN/GaN microwave transistors.
In 2007 he joined Smoltek AB, where he now is the CTO, focusing on the development and modeling of devices, components and prospective technologic solutions for the microelectronics industry, based on Carbon Nanofibers (CNF).
Since 2006, he has also been with the Group for Advanced Receiver Development, Chalmers University of Technology, Gothenburg, where he now is a professor in microwave electronics and THz Technology. His research deals with nanotechnology for radio-astronomy instrumentation and superconducting electronics.
Vincent Desmaris authored or co-authored +150 articles and patents

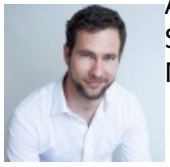
Control of Advanced Packaging by Improved Optical Profiler Metrology

S. Lesko
Applications development director
Bruker, Nano Surfaces and Metrology, San Jose, United States

Abstract
Advanced packaging challenges standard metrology means, notably optical profilers, by shrinking dimensions and spacings between interconnect (RDL, Bump, via). Stacking of NAND memory in as well as die to die or wafer to wafer bonding in heterogeneous integration bring new metrology needs such as die flatness and fine CMP optimization.
In this talk, we will introduce optical profiler based on White Light Interferometry principle (WLI) which has inherent advantages combining lateral resolution below micron level as well as providing sub-nanometer vertical resolution at all magnifications. We will explain how this technology can address within single measurement head all controls for critical integration steps such critical dimensions of Re-Distribution Layer (RDL), defect inspection for bump, depth and diameter of high aspect ratio Through Silicon Via (TSV) and overlay offset. Talk will also provide tangible proof of scalability to future roadmap so scope through new development.
Practical examples will be shown along monitoring of post-CMP die flatness in case of Chip-on-Wafer-on-Substrate (CoWos) or chiplet building processes, next generation high density RDL in wafer level packaging (InFO) as well as overlay control between two stacked layers. For die flatness, high throughput, sub-µm lateral resolution and sub-nanometer repeatability results will discussed. New optical super-resolution algorithms will provide evidences of RDL width metrology capability up to 0.2µm while advanced analysis combined with optical signal calculation will allow offset repeatability for overlay application better than 20nm.

Biography
Samuel has Ph.D. and engineering degree in material science from the University of Burgundy (France). Since 2000, he has built extensive experience in optical profiler, particularly in using white light interferometry applied to MEMS and semiconductor through local application and global European Middle East application managing positions. He is now leading the applications development teams at Bruker San Jose (CA) to provide tailor solutions solving current and future metrology challenges on worldwide basis.

Rapid packaging of system components



A. Krause
Scientist
MicroPack3D, Dresden, Germany

Abstract
Current electronic packaging consists of long-lasting steps of bonding and housing to get an integrated circuit into a standard format package. The effort requires time and money and is only feasible for a large amount of devices. With new additive manufacturing technologies, new process chains arise with incredible amount of design freedom, miniaturization potentials and material customization for specific customer needs.

We are MicroPack3D, a startup of the technical university of Dresden and we developed the KONEKT process (KONEKT – connection of embedded components as technological solution) to take advantage of these new possibilities of manufacturing. Our aim is to bring additive manufacturing to small and medium-sized companies beyond standard limits of packaging, especially to those, who were not able to afford the price of highly adaptive production. The disruptive feature of our technology comes within the freedom of design in both shape and choice of parts. We use a fast and flexible free shapeable embedding process technology for housing together with a copper metallization process to form the whole package without the restriction of standard PCB manufacturing. As a key feature, the KONEKT process requires a significantly smaller amount of production steps, offering a full package produced in down to one day, of course in dependence of the complexity of the package. This advantage gives the customer the possibility of very short development cycles at an affordable price. Especially for smaller or mid-sized companies, this offer may give them the advantage of quickly testing new ideas or concepts to stay ahead of other competitors. The flexibility of the KONEKT process further allows the increase of the functional density by miniaturization using bare dies or smaller pitch copper interconnects or even the potential of 3D stacking and connection of electronic devices and with it a much higher design freedom. The high conductivity copper interconnections are fabricated without a soldering step and can reduce the thermal stress to highly sensitive circuits or sensors. Housing materials are selected by the required application, offering adaptable properties to ensure safety from water, heat, physical stress and radiation protection amongst others.

With MicroPack3D, the KONEKT process will be open and affordable to everyone.

Biography
Andreas Krause studied physics at the TU Dresden with the specialization on semiconductor and laser physics as well as nanotechnology and chemistry. After his successful diploma, he started his PhD at the nanoelectronic materials laboratory (NaMLaB). He worked on materials research for future DRAM capacitors and finished his PhD in 2014. He used his expertise to establish processes for deposition of nanometer ferroelectric layers and worked as leading scientist for the integration of silicon nanowires in lithium ion batteries. Since 2019 he works at the electronic packaging lab at the TU Dresden in the startup project as expert for materials and process development. At MicroPack3D GmbH (iG), he is responsible for research and development operations.

Advanced Plasma Dicing for Manufacturing of 3D Stacked Devices

S. Okita
Process Equipment Development Department Manager
Panasonic Smart Factory Solutions Co., Ltd.,
Process Equipment Development Department,
Osaka, Japan

Abstract
In the field of advanced packaging technology, the adaptation of 2.5D and 3D stacking technology is expanding to increase the degree of packaging integration. Wafer thinning, wafer singulation and bonding technology have become more important and necessary in realizing these stacked packages. In order to stack packages in high density, it is necessary to stack thinner chips and/or wafers, and it is necessary to perform bonding through pads, bumps and micro bumps, or direct bonding between flat surfaces. In order to realize a higher-density stacked package structure, it is necessary to reduce the vertical direction of bonding distance. However, conventional dicing methods such as blade and laser dicing have the issue of particle and debris creation, which make it more difficult to reduce the vertical direction of bonding distance.

Panasonic established the Plasma Dicing Demonstration Center in 2016 and has continuously developed advanced Plasma Dicing technology. Total process integration of Plasma Dicing has been realized. Plasma Dicing is a promising singulation technology that dices wafers by plasma processing, mounted on metal ring frames. Furthermore, Plasma Dicing not only enables stronger chip strength, but also realizes particle-free and debris-free singulation, keeping the wafer surface and bonding surface clean. In this paper, Panasonic will introduce DAF (die attach film) plasma dicing technology which is required for 3D stacking technology, and the plasma dicing techniques necessary to suppress particles and surface contamination by using special protective films and the integration of such technology.

Biography
Shogo Okita is the manager of the Process Equipment Development Department at Panasonic Smart Factory Solutions, and is responsible for the development of plasma process equipment and respective processes, as well as the total process integration of Plasma Dicing.

In 1997, he joined Matsushita Electric Industrial Co., Ltd. (now Panasonic Co., Ltd.) as a process engineer. Since then, he has been engaged in R&D activity, product development and worked on the development of various plasma sources and processes for dry etching equipment in the field of Si & Compound semiconductors, MEMS and LCD devices. He is the author of many patents.

He received a B.S. degree in physics from Kwansei Gakuin University, Japan.

F. Kuechenmeister
PMTS
GLOBALFOUNDRIES, POSTFAB NPI & CPI, Dresden, Germany

Biography

Dr. Frank Kuechenmeister received a Master degree in Polymer Chemistry and a doctorate in Chemistry from the University of Technology in Dresden, Germany. He held post-doctoral appointments at the Departments of Polymer Science at the ETH Zuerich, Switzerland, the University of Massachusetts in Amherst, USA and the Department of Electrical Engineering and Micro Systems at the University of Technology in Dresden, Germany. He joined AMD in 1999, which converted to become GLOBALFOUNDRIES in 2008 as process engineer working the area of C4 bumping. He was promoted to principal member of technical staff in 2016. He currently leads the chip-packaging interaction team and coordinates all related efforts throughout all technology nodes at GLOBALFOUNDRIES.

Challenges for Heterogeneous Integration in Package – Applications Driving Materials and Processes towards Diversity

T. Meyer
Lead Principal Engineer
Infineon Technologies, Regensburg, Germany

Abstract
ABSTRACT

Challenges for Heterogeneous Integration in Package –
Applications driving Materials and Processes towards Diversity

by Thorsten Meyer and Klaus Pressel
Infineon Technologies AG, Regensburg

Heterogeneous Integration is a major technology driving force for microelectronic systems. More-than-Moore (MtM), System-in-Package (SiP), as well as 3D high-density integration technologies are a prerequisite for enabling the design of compact microelectronic devices. Heterogeneous Integration refers to the integration of separately manufactured components into a higher level of assembly, which is providing enhanced functionality and operating characteristics. In this definition, components should be taken to mean any unit, whether individual die, MEMS or sensor device, passive component and assembled package or sub-system, that are integrated into a single package (see e.g. Heterogeneous Integration Roadmap published for the first time October 2019).
The requirements for integration of the mentioned components are differing strongly depending on application. Integration of power devices requires thick copper with large area connections for thermal properties and current carrying capabilities, e.g. a solution for vertical current flow. For mm-wave applications, precise knowledge of material parameters and dimensions is required to fabricate leading edge devices like radar or LIDAR for future autonomous driving. Logic integration typically requests for many short interconnects, fine line spaces and tight pad pitches in a horizontal arrangement of the contacts. MEMS and sensor devices often require a special protection and are sensitive in handling during production. Packaging often is customized to the application. In addition, the integration of passives, e.g. resistors, inductors, capacitors, as well as shielding capabilities or antennas require special packaging building blocks for an application tailored integration. All these different constraints lead to an extreme diversity of package solutions very difficult to tackle.
In this presentation, we will discuss the challenges and introduce potential solutions for different integrated applications. We will highlight the importance of virtual prototyping, chip-package-board/system co-design as well as reliability prediction, which require detailed understanding of material properties and their interfaces. Especially, we will emphasize the increasing importance of knowledge on material physics. For example, investing into physics of advanced failure analysis is a major enabler for faster and more reliable development of innovative devices. We will show examples of building blocks for different areas of integration, which we must develop for the supply of integrated packages for future applications. Heterogeneous integration combined with miniaturization capability, i.e. more functionality in smaller volume, will drive us in future microelectronics.

Biography
Thorsten Meyer is Lead Principal Engineer Package Concept Engineering at Infineon Technologies in Regensburg, Germany, responsible for New Package concepts. Until March 2015 he was leading the Package Technology and Innovation department at Intel Mobile Communications (IMC) in Regensburg. Prior joining IMC, he was overall project leader for the development of Wafer Level Packaging Technologies at Infineon in Regensburg and earlier in Dresden.

Thorsten is author of multiple publications and holds more than 150 patents and patent applications in the area of advanced packaging.

Flip-Chip Scale Package(FCCSP) Process Characterization and Reliability of Coreless Thin Package with 7nm TSMC Si

E. De Mesa
Package Engineer
Intel Deutschland GmbH, Munich, Germany

Abstract
Advanced silicon nodes are continuously pushing the cutting edge of assembly technology for coreless thin packages used in mobile and electronic products to allow better power delivery, electrical performance, and higher routing capability. This results in a higher number of I/O and integration flexibilities. Furthermore, integration of a large die size in a smaller package with finer bump and ball pitches, increases the reliability risk. Also, typical mobile applications require stacking a memory die within the package without increasing the total package height. These combinations magnify the stress on back-end-of line (BEOL) stack and bump interconnection-especially on a thin coreless substrate which greatly influence extreme low-K dielectrics (ELK) fragility.

This paper describes the qualification of the 7nm silicon (Si) BEOL stability on thin coreless embedded trace substrate (ETS) with smaller solder ball pitch and a high die to package aspect ratio. In our previous experience, coreless material is generally prone to warpage due to absence of the core that supports the package rigidity. Therefore, controlling and minimizing warpage at room and elevated temperature is crucial, as the stress propagates into the BEOL, resulting in a significant impact on the chip reliability, especially for ELK structures. Simulation of thermal and mechanical stress in Finite Element Modeling (FEM) was completed to confirm warpage behavior. Shadow Moiré was documented under temperature loading and package coplanarity empirical data was collected.

Within the development phase, the package warpage was successfully reduced and coplanarity on thin coreless substrate was within specification. Significant improvement is attributed to mold compound higher coefficient of thermal expansion (CTE) and lower elastic modulus. Multiple reliability tests in accordance with JEDEC standard was conducted. Results confirmed the BEOL stack integrity and all related tests passed.

Biography
Eduardo De Mesa received B.S Mechanical Engineering from Mapua Institute of Technology, Manila, Philippines. Currently, working under Technology Enablement Group engaged in advanced package development at Intel Deutschland Gmbh.

Active Mold Packaging for Novel Antenna-in-Package Interconnection and Manufacturing

F. Roick
Business Development Active Mold Packaging
LPKF Laser & Electronics AG, Garbsen, Germany

Abstract
IC package designers wishing to benefit from space saving Antenna-in-Package (AiP) technologies rely on an intricate selection of materials and interconnect processes to produce a self-contained integrated module. This paper presents a new way to reduce the production complexities of AIP by introducing a novel homogeneous packaging technology: Active Mold Packaging (AMP).
Active Mold Packaging directly establishes electrical connections, such as patch antennas, signal vias, and Electro-Magnetic-Interference (EMI) shields for RF applications on the surface and in the volume of the encapsulating Epoxy Mold Compound (EMC). Advancing the development of multifunctional compact devices, AMP in essence transforms the passive and undeveloped real-estate of the EMC into an active carrier of package functionality.
A 2.5D interconnect technology to simplify AiP designs and EMI shielding will be presented. AMP integrates familiar process steps: molding of EMCs, Laser Direct Structuring and direct electro-less and galvanic plating. In combination the processing steps result in a robust scalable manufacturing solution, AMP. AMP is uniquely suited for the production of AiP but also a foundation design platform for other novel IC packages. Critical process attributes of AMP are discussed and used to propose a commercial AMP-AiP model. Measuring the influence of key design elements of an AMP fabricated EMC micro strip antenna and EMI shield within the 5G radio frequencies; sub-6GHZ, mm-wave, and beyond 5G (« B5G ») ISM bands yields strategies for implementing the AMP technology. Consideration is granted to the impact of the LDS activator, the laser structuring parameters, and electroless plating factors on the model devices. Lastly, the proposed commercialization of the AMP-AiP is modelled through a cost-model comparison.

Biography
M. Sc. Florian Roick, Business Development Manager Active Mold Packaging
Born in 1981. He holds a degree as Bachelor of Science in Applied Physics from Dublin Institute of Technology. And a degree as Master of Science in Electrical Engineering with focus on laser systems, laser physics and microsystems engineering from Hochschule Bremen.
Since 2006 employed at LPKF Laser & Electronics AG, until 2008 as application engineer for the StencilLaser business unit. Between 2008 and 2019 strategic product manager responsible for aligning the product portfolio with the needs and requirements of the PCB and SMT markets.
Since 2019 Business Development Manager for LPKF's Active Mold Packaging technology. That is to electrically functionalize the real-estate of the epoxy mold compound on the base of LPKF's patented Laser Direct Structuring (LDS) technology.
Co-inventor of the parametric stick-in and co-author of a variety of publications.

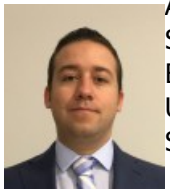
High Throughput & High Yield Heterogeneous Integration with Implemented Metrology for Collective D2W Bonding

E. Brandl
Business Development Manager
EVG, St Florian am Inn, Austria

Abstract
Heterogeneous integration offers several advantages in performance gain, functionality increase as well as yield enhancement. Depending on the device architecture and level of integration, several integration methods at different manufacturing levels can be used to create heterogeneous integrated systems. Processing on die level is often practiced, leading in some cases to throughput and yield considerations. Collective die to wafer bonding can enable several integration processes on wafer level via using a reconstituted transfer carrier approach. Especially in hybrid and fusion bonding this method enables heterogeneous integration as processes such as plasma activation are better performed on wafer level for high throughput.
As for all semiconductor processes, collective die to wafer bonding demands suited and optimized measurement solutions for process monitoring and yield optimization. Fitting metrology combined with a feedback loop for production equipment is essential to increase yield of the whole integration process and an important factor in successful heterogeneous integration. Regarding metrology implementation, two scenarios are generally possible. One is the implementation of metrology within the bond equipment, which allows a quick reaction and the process parameters can be directly adjusted. The consideration of such implementation demands throughput matching for high equipment efficiency. The other implementation method is an external metrology tool, where the feedback is delayed, but on the other hand one metrology tool can serve several production tools.
In the presentation the process flow of collective die to wafer bonding will be discussed in more detail as well as the advantages and disadvantages of the two metrology implementation scenarios.

Biography
Elisabeth Brandl received her master in technical physics from the Johannes Kepler University Linz, Austria in Semiconductor and Solid State Physics. Since 2014, she has been responsible for Product Marketing Management for temporary bonding and metrology at EVG.

Vertical Stacking of Controller IC on a Copper Clip Attached on MOSFET as a Space-saving Solution for High Current Switch e-fuse Applications



A. Attard
Sr. Technical Program Manager & Assembly Business Development
United Test and Assembly Center Ltd, Singapore, Singapore

Abstract
Recently there has been an increasing demand for high-performance computing, mainly driven by data centers, online storage, cloud-based servers, and online software services. These applications require high computing power which drives high energy consumption, so the power systems employed need to run at extremely high efficiency and have small form factors, whilst offering very high reliability and minimal thermal losses during their deployment. This can be achieved by improving both the power semiconductor device technology, as well as the power packaging technology, such that maximum power performance and reliability can be extracted from the PCB area available.

Power MOSFET technology has evolved to reduce switching losses and allow high frequency switching. Power modules have also been developed to integrate MOSFET dies together with a controller IC in a single package to offer a small form factor solution. From an interconnect perspective, copper clip bonding began to replace wire bonding technology due to the lower resistance and parasitic inductances it offers compared to wire bonding. Whereas most multi-die power module packages employ a side-by-side die configuration due to the wire bonding interconnect method, copper clip packages allow for vertical die stacking, which results in a smaller package for the same power rating.

In this paper, we propose a QFN power module package solution for an electronic fuse (e-fuse) device in high-performance computing applications, comprised of a controller IC vertically stacked onto the copper clip used to create the interconnect between the MOSFET die and the lead frame. This approach provides a vertically integrated power module solution, offering a significantly reduced form factor versus a side-by-side power module approach or the use of two separate QFN packages for each die. Typical e-fuse applications need two separate QFN packages, for example, a 3mm x 3mm QFN for the controller IC and a 5mm x 6mm QFN for the MOSFET die, occupying a total of 39mm^2 of PCB area. Comparatively, a vertically stacked power module can be packaged in a 5mm x 5mm QFN occupying a total PCB area of 25mm^2, resulting in 36% less PCB area usage. The vertically stacked power module also offers excellent thermal performance despite the increased power density of the package. Thermal simulations performed using a 5mm x 6mm e-fuse package structure with 4.1W of combined power dissipation show that a Theta Ja of 25.3 ^{o}C/W and maximum temperatures of around 128.8^{o}C for the IC and 123.9^{o}C for the MOSFET are achieved under still air conditions.

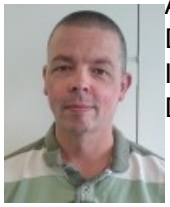
The assembly process flow will also be discussed in more detail, with focus on critical process steps such as vacuum reflow to ensure minimum voiding in the solder interconnects between MOSFET and lead frame, and copper clip and MOSFET. Examples of actual devices will also be shown. UTAC's outlook on more advanced power modules will also be shared, showing proposals for packages with increased complexity using three dies and copper clips in a vertically stacked configuration for smart power stage applications with reduced footprint requirements.

Biography
Alastair Attard is Senior Technical Program Manager and Assembly Business Development at UTAC Group. He has a Bachelor's degree in Mechanical Engineering and an Executive MBA from the University of Malta.

He has over 14 years of experience in the assembly & test of semiconductor devices.

Prior to joining UTAC, Alastair worked at STMicroelectronics Malta from 2006 until 2011, first as a Process Engineer on flip chip assembly for SiP and later as a Package Development Senior Engineer for SiP and MEMS packages. He later joined Besi in 2011, where he was Manager of the Process Development group until 2018.

At UTAC, he is responsible for Technical Program Management and Assembly Business Development in the European region, with main focus on Automotive, Industrial, SiP, Power and MEMS areas.



A. Miller
Department Director
IMEC, 3D and Si Photonics Technology Development, Leuven, Belgium

Biography
Andy Miller graduated from the University of Glasgow in 1995 with a Honours degree in Physics. He immediately started work as a process engineer at NEC Semiconductors (UK) Ltd in lithography. In 2000 he moved to Filtronic Compound Semiconductors Limited as lead lithography engineer. In 2008 he joined the Advanced Lithography program at IMEC, focused on alternative materials for Double Patterning.
In 2009 he became the Team Leader for More Than Moore lithography development at imec, quickly expanding the team to include wafer level bonding, die bonding and metrology. In 2012 he took up the position of Group Leader for technology development within the 3D Integration program. He is currently the Department Director for 3D and Si Photonics technology development at imec.

Test Methods for System-in-Package and Challenges to Testing Heterogeneously Integrated Systems

G. John
Senior Director, FCBGA Business Unit
Amkor Technology, Inc., Tempe, Arizona, United States

Abstract
Moore's law is not dead, nor is it dying – it is being reborn in the form of Heterogenous Integration (HI). HI is a powerful design innovation that improves manufacturing yield without sacrificing quality. HI creates semiconductor devices by connecting chiplets and dielets from various fabrication nodes. System-in-Package (SiP) designs employ HI in various forms to reduce product footprint, increase product functionality and lower costs. Prior methodologies consisted of building one large die containing most of the needed functionality for a product. As dies get larger, they have a higher probability of being impacted by inherent wafer defect density, and therefore, are prone to a lower yield. Realizing this phenomenon, integrated circuit (IC) designers split the functionality of the large die into small chiplets or dielets. Leveraging the advantages of HI, SiP designers build modules containing 5/7-nm silicon technology for high end ASICS, while lower complexity functions continue to be built using lower cost, larger, silicon nodes.
The switch to HI in SiP modules introduces unique testing challenges, where a test engineer needs to have a broad spectrum of expertise, covering the testing of: antennas, radio frequency (RF) devices, modulators and demodulators (modems), baseband, high-speed digital, serializer/deserializer (SerDes), photonics, power control and distribution, embedded actives/passives and interconnect technologies. This expertise must be applied to Wafer Probe Test, Partially Assembled Test (PAT), Final Test (FT) and System-Level Test (SLT).
As assembly techniques vary, so do the challenges of package-level testing. Therefore, the scope of this talk will be limited to one assembly technique but can be adapted to other assembly techniques. To add relevance, this talk will focus on test while building a hypothetical SiP - 5G Micro-Base Station (MBS) using HI. The 5G MBS will be built using four HI sub-modules, one for the processor, two RF sub-modules and one power, MEMS and accessories module, all of which will finally be assembled on a single motherboard.
The test methods for the processor module will cover high speed testing of reconstituted multichip AISC wafers, testing Through Silicon Via (TSV) interposer and testing the processor subassembly using PAT and SLT. The RF sub modules test describes SLT and antenna in package (AiP), including testing phased array antennas with Over-the-Air (OTA) Testing. The last module will cover SLT for the MEMS & DC subsystems. The final SiP assembly will be tested using SLT.
Through this talk, the attendees will gain an insight into the challenges of testing a complex HI SiP system.

Biography
Gerard joined Amkor in 2005, and currently manages the FCBGA product portfolio for customers in Europe, Israel and South Korea. He previously served as an advanced test technical expert for MEMS, 2.5D, WLFO, HDFO, fine pitch probe and optical devices, supporting customers in the US and Europe. Prior to joining Amkor, Gerard worked in various semiconductor test positions for Conexant Systems, Flarion Technologies (acquired by Qualcomm) and Motorola. He holds a BA degree in electronics and telecommunications engineering from Osmania University and an MBA from Gainey School of Business in Michigan and is pursuing a MSEE from the University of New Mexico.

New Solutions for Plasma Dicing, and New Solutions for Processing of SiC Wafers Ranging from Ingot Splitting, Grinding, Polishing to High Speed and Chipping Free Dicing

G. Klug
General Sales Manager
DISCO Hi-Tec Europe GmbH, Sales, Kirchheim b
Muenchen, Germany

DISCO
Kiru·Kezuru·Migaku Technologies

Abstract
Wafer thinning (Kezuru and Migaku) and dicing (Kiru) is essential for advanced packaging, for achieving narrow street widths and for making thin dies for 3D-packaging. New solutions on plasma dicing in combination with latest tapes and grinding technology enable the supply of perfect top side, back side and side wall quality on dies in thickness range from 20 – 150 µm.
Plasma dicing has various advantages comparing to the conventional dicing. However, during the plasma dicing process the sensitive wafer front can be at risk due to the surface being exposed to plasma gas. It is common to protect the wafer front surface by photoresist in the wafer fab, which increases the cost and the processing steps.
DISCO has developed a special surface protection film and a total new processing flow for plasma dicing to overcome these issues.

SiC is getting more and more important for the energy efficient devices. Since SiC is a very expensive material DISCO focuses on technologies for gaining as many as possible wafers and dies of outstanding quality out of it.
SiC ingot splitting by KABRA:
KABRA is a new method for SiC-ingot slicing by using a laser instead of a wire saw. In this process, a special layer is made inside of the ingot by laser irradiation and then the wafer is split from the ingot. 40% more wafers are obtained out of one ingot compared to conventional method.
SiC ingot and wafer grinding and polishing:
After splitting the wafer from the ingot, the ingot side and the wafer side need to be ground and polished. DISCO has developed grinding wheels and polishing pads (E Pad) suitable for wafer manufactures and device makers.
SiC wafer dicing by blade or laser:
To obtain more numbers of dies from a wafer, cutting streets can be reduced down to 50 µm and less. With our special technologies cutting speed and quality have been greatly improved, too.

Biography
Gerald Klug has studied business-engineering at the University of Siegen and graduated as Diplom-Engineer in 1998.
He started his carrier as a designer and project engineer of steel cutting lines at a globally leading German machine manufacturing company.
At the end of 2000, he joined DISCO as Sales Engineer. Meanwhile he has been working for DISCO for 19 years and is nowadays operating as General Sales Manager for the territory of Europe.

Virtual Prototyping for System-in-Package with Heterogeneous Integration - Enabler for faster Time-to-Market

G. Gadhiya
Research Associate
Fraunhofer ENAS, Chemnitz, Germany

Abstract
Heterogeneous Integration in System-in-Package (SiP) based on Fan-Out Wafer Level Technologies allows to meet various requirements such as improved performance, smaller form-factor, functional safety and low cost for upcoming new applications. Due to the thermo-mechanical stresses leading to device failure, the reliability risks must be assessed during the development of new products aiming for a design optimized for reliability. Virtual Prototyping (VP) based on Finite Element (FE) simulation allows the analysis of the thermo-mechanical situation during fabrication, tests and service within short time, allowing shorter development time. However, it requires parametric FE models, precise material and experimental data for validation. Because of this initial investment, it is advised to develop the VP schemes in a way that they are able to cover a wide variety of future products.
The talk will present a modular system of parametric FE models that enables virtual reliability assessments of various SiP products based on Fan-Out Technologies such as WLSiP, eWLB-PoP, RCP, InFO, FOPLP, WFOP, SiWLP and SWIFT-PoP [1][2]. By combination of common packaging components like die, mold, redistribution layers, solder balls, vias, integrated passives, and boards from the library of pre-calibrated parametric FE models in ANSYS, digital twins of a large number of individual package configurations can readily be generated, e.g. 2D, 2.5D and 3D/PoP. The talk highlights the flexibility of the modular system of parametric FE models by four very different industrial packages: Radar sensor, Silicon photomultiplier, Automotive inertial sensor and Camera module. The VP scheme for a new pad design of a multi-chip SiP sensor is demonstrated in detail to show the great support that virtual optimization and qualification schemes can provide. They can reduce Time-to-Market of new SiP products by 50%-75%.

References
[1] https://doi.org/10.1109/ESTC.2018.8546352
[2] https://doi.org/10.1115/1.4043341

Biography
Ghanshyam Gadhiya received his M.Sc. degree in Micro and Nano Systems, with a specialization in Finite element analysis of power module from Technical university of Chemnitz in 2013. Since 2014, he is working as a scientific researcher at the Micro materials center, Fraunhofer ENAS. His main research focus includes parametric finite element modelling, thermo-mechanical simulation and optimization of microelectronics packages using FE-program ANSYS. He has been also involved with several industrial projects for residual stress, humidity and vibrational analysis. His current research interests include fan-out wafer level packaging technology, system-in-package, virtual prototyping and micro-electronics failure analysis.

Innovative Packaging and Evaluation Approach for an Universal Sensor Platform

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Group Manager Sensor Nodes and Embedded Microsystems
Fraunhofer Institut für Zuverlässigkeit und Mikrointegration, RF& Smart Sensor Systems, Berlin, Germany

Abstract
This article presents an innovative packaging and evaluation approach for a newly developed Universal Sensor Platform (USEP) based on a system in package RISC-V integrated microcontroller with a top-level functionalized system in package design. Specific functions of the sensor platform are assigned to four different physical levels in the whole integration concept. The technical implementation of the functional requirements requires innovative, technological solutions in the packaging and interconnection technology (AVT) but also new approaches for testing methods and infrastructure across the different levels.
Starting from a bare die, inclusion of package co-design, new assembly and interconnection techniques, up to the provision of the evaluation and testing of the platform system, the increasing complexity of this research projects in microelectronics becomes apparent.

In the final step of finalizing the system in package solution, the sensors are applied to the functionalized package surface. This enables the system to directly measure various parameters such as temperature, humidity and pressure. The electrical connection of the components is done on a multilayer redistribution layer, which is applied to the mold material of the package and connected to the underlying system core with through package vias. For testing, a modular evaluation board is available, which allows the connection of an FPGA-based emulation environment. Furthermore, various test adapters can be connected to the data bus, thus significantly increasing the modular testability. A test socket detachable from the circuit board connects the manufactured modules with their 256-BGA footprint with all electrical operation and debug signals and plays a central role for the actual chip test because it enables short testing and configuration cycles.

Biography
Carsten Brockmann studied Technische Informatik at the Technical University of Berlin and received his diploma in 2008. He worked as a scientist at the Forschungsschwerpunkt Technologien der Mikroperipherik in the field of wireless sensor nodes until 2014 when he changed to Fraunhofer Institute for Reliability and Microintegration. In different national and international research projects he proceeded with his research work and became the group manager for sensor nodes and embedded microsystems in 2015.

P. Cockburn
Program Manager
Cohu, Inc., ISG, Verwood, United Kingdom

Biography
Peter Cockburn has worked in the ATE industry for over 30 years at Schlumberger, NPTest, Credence, LTX-Credence, Xcerra and now Cohu. He is currently responsible for several key interface projects including adding intelligence into test contactors to improve test cell efficiency and developing a range of high performance, low-cost interfaces for emerging 5G applications.
After developing realtime and GUI software for ATE systems, he moved into product marketing and launched several new SOC ATE systems and analog test options as well as providing marketing and sales support in USA, Asia and Europe.

As leader of the Test Cell Innovation team he was responsible for defining and delivering complete test cells to customers to reduce cost, increase uptime and improve quality when testing pressure and motion sensors, microphones and wafer-level packages.
He has an Engineering degree from the University of Southampton, UK.

Heterogeneous Integration - The New Driver of Innovation and Growth

R. Beica
Chief Sales Officer, Semiconductor Division
AT&S, Semiconductor Division, Leoben, Austria

Abstract
The explosive growth in data generated and computing needs, global network traffic and digital transformation are further driving the adoption of electronics and semiconductor devices. The need for more performing and smarter devices, with increased functionalities, that can address high bandwidth needs, faster speeds, parallel processing, with more efficient power consumption is driving the industry to further develop new and innovative technologies. While innovation in mobile devices continues, new emerging applications, such as IoT, Artificial Intelligence and 5G are expected to drive the next phase of innovation across the supply chain. The new driving forces are also shifting the importance in the industry from technology node scaling to system level integration.

This presentation will give an overview of the global market trends highlighting the major industry trends and applications, the increased need and growth of heterogeneous and system level integration and the solutions that AT&S is bringing to the market to address current and future market needs.

Biography
Rozalia Beica is currently the CSO of Semiconductor Division, focusing on semiconductor and module activities within AT&S. Prior to AT&S she had several executive and C-level roles with various organizations across the supply chain: electronic materials (Rohm and Haas Electronic Materials, Dow & DuPont), equipment (Semitool, Applied Materials and Lam Research), device manufacturing (Maxim IC) and market research & strategy consulting firm (Yole Developpement).

Rozalia is actively involved in various industry activities. Some of the current engagements include: Member of the Board of Governors for IEEE Electronics Packaging Society and Vice General Chair of 71th ECTC, Chair of the Heterogeneous Integration Roadmap WLP Technical Working Group, Chair of the Semi Strategic Materials Conference, Technical Chair of System in Package China Symposium, Advisory Board Member 3DinCites and IMPACT Taiwan. Past activities: IMAPS VP of Technology, General Chair IMAPS DPC, Program Director EMC3D Consortia, General Chair Global Semi & Electronics Forum, Technical Advisory Board Member SRC, several other memberships in industry committees. Rozalia has over 150 presentations & publications, including 3 book chapters on 3D Integration.

Rozalia has a M.Sc in Chemical Engineering (Romania), a M. Sc. In Management of Technology (USA) and a Global Executive MBA from IE Business School (Spain).

Enabling Assembly and Packaging Material Developments for Next Gen RF Devices, Antennas and Radars

R. de Wit
Business Development Manager EMEA
Henkel Belgium NV, Westerlo, Belgium

Abstract
Smart Electronics' market trends like 5G Telecom and Autonomous Driving are leading advanced semiconductor packaging innovations towards higher functionality, enhanced connectivity at higher frequencies, RF signal interference isolation (shielding), smaller form factors (miniaturization) and reduced power consumption. To meet these demands, semiconductor package designs continue to evolve towards MULTIPLE DIE using System-in-Package and Wafer Level architectures. Especially for next generation RF devices, antennas and radars, the thermo-mechanical, thermal resistance and (di)electric properties of the assembly and packaging materials play a key role as well as fast and low temperature processing/curing. This presentation will give an overview of the challenges and solutions from a semiconductor packaging material perspective based on recent customer experiences and ongoing developments to enable new designs. The focus will be on thermal performance of different die and lid attach assembly methods and thermal interface materials, EMI shielding effectiveness of thin silver layers, dielectric constant and loss factors of liquid wafer level encapsulants and underfills at 28-50 GHz and above, etc.

Biography
Ruud de Wit is responsible for managing Henkel's Semiconductor, Sensor & Consumer Electronics Assembly Materials business development within EMEA region. Ruud has a BSc degree in Mechanical Engineering followed by several polymer, sales and marketing courses. Ruud is working for Henkel since 1990 in multiple positions including technical customer support, quality assurance and engineering, and global semiconductor account and product management.

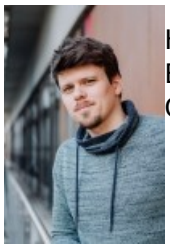
Development of a Foil based Flexible Interposer for Power Conditioning IC in Energy Autarkic Systems

E. Yacoub-George
Scientist
Fraunhofer EMFT, Flex, Munich, Germany

Abstract
The EU ECSEL project EnSO aims the development of autonomous micro energy sources (AMES) for innovative electronic devices that target key applications such as smart health, smart mobility and smart society. An AMES provides energy for sensors, data processing and data transmission and consists of micro storage element, energy harvester, smart charger and power conditioning IC. Smart integration of these building blocks to fabricate an AMES with an appropriate form factor was a key objective in the EnSO project.
Although in printed electronics, the PCB board is ususally fabricated with an innovative technology it is often still assembled with bulky and rigid SMD components. In such a case, some of the primary advantages such as conformability and flexibility that are commonly attributed to printed electronics are lost. In order to overcome this limitation, we developed a new package type called “flexible interposer”. It consists of a Cu wiring film fabricated in roll to roll, a thinned IC and a flexible polymeric mould cover. The interposer is designed with a QFN format and is characterized by a reduced thickness and some mechanical flexibility. The flexible interposer approach was developed and characterized for a daisychain chip and a commercial power conditioning IC of the latest generation from STMicroelectronics. The fabrication process was established with the daisychain chip to facilitate electrical characterization and reliability testing and was then adapted for the STBC15 IC. 30 interposer samples have been prepared and characterized. The obtained process yield indicates a robust fabrication process. Since all process steps are compatible with roll to roll production, we expect a high potential for up-scaling that offers the chance to close the gap between research and market.
The research results were obtained in the scope of EnSO project that has received funding from 1) EU under Grant Agreement no. 692482 and 2) BMBF with National Grant no. 16ESE0088.

Biography
Erwin Yacoub-George received his Ph. D in Chemistry (1994) at Technical University of Munich where he developed a production process for polysiloxane beads. Since 1994 he worked for the Fraunhofer Society in Munich. He started his research works on the development of optical biosensor systems. In 2002 he joined the flexible electronics team and developed self-assembly processes for thinned ICs as well as heterogeneous integration techniques for printed and large area electronics. He is currently working as a project manager on European and National research projects with a focus on thin chip integration in flexible foil substrates.

Holistic Thermal Material Characterization Approach for Thermal Performance Optimization of Electronic Packages



T. von Essen
Head Of Marketing
Berliner Nanotest und Design GmbH, Berlin, Germany

Abstract
Thermal management is a key component of electronic package design in general and heterogeneously integrated System-in-Package design in specific. Functionality, life expectancy and reliability of packages strongly depend on their thermal performance. The application of the right materials is most important to achieve the targets. Furthermore, numerical analysis for lifetime prediction requires correct material data for credible propositions.
As material properties strongly depend on use case and field scenario, but material datasheets, unfortunately, tend not to provide the details and accuracy required, it is crucial to acquire material data reliably using suitable methods.
The presentation will describe a systematic approach to identify the contribution of different materials in electronic packages to the overall thermal performance and which ones are potential bottlenecks. For the different material classes, different characterization methods are presented and discussed.
Thermal interface materials (TIMs) are centerpiece of the discussion, as they contribute with up to two thirds to the overall thermal junction to case resistance. The best approach to TIM characterization is following the ASTM D 5470 guideline, which does not only provide thermal conductivity as output but also the interface resistance, which is a crucial component of thermal interfaces with continuously shrinking gap width.
Second important group of materials in the list are metals and semiconductors in the package, all with rather high thermal conductivity and not possible to characterize using the ASTM D 5470 approach. However, a quite similar approach, moving from through-plane to in-plane measurement, will be presented. It allows the precise characterization of such materials and yields thermal conductivity and diffusivity as result, which is gratefully acknowledged input to numerical analysis. The same methodological approach enables the characterization of metal-based die attach materials such as solder and sintered material samples.
Eventually, a system-level evaluation method will be shown that can provide performance benchmarking of assembled prototypes and can greatly serve as validation beacon for numerical models.
In conclusion, an example of a typical electronic package will be shown, summarizing all presented methods and system-level test. The used complete off-the-shelve product family offering all the presented methods ready to use will be introduced.

Biography
Tobias von Essen studied Micro Systems Engineering and Systems Engineering at the University of Applied Sciences in Berlin, receiving his master’s degree in 2013, where he implemented a test stand for transient thermal characterization. Since 2011, he is part of the Nanotest team, first as student worker and, subsequent to his master’s thesis, as permanent employee. Tobias is responsible for marketing and sales activity at Nanotest, but also leads multiple software projects of Nanotest-proprietary characterization systems and partakes in method and system development. His scientific focus is steady-state thermal material characterization.