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Flip-Chip Scale Package(FCCSP) Process Characterization and Reliability of Coreless Thin Package with 7nm TSMC Si

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Abstract
Advanced silicon nodes are continuously pushing the cutting edge of assembly technology for coreless thin packages used in mobile and electronic products to allow better power delivery, electrical performance, and higher routing capability. This results in a higher number of I/O and integration flexibilities. Furthermore, integration of a large die size in a smaller package with finer bump and ball pitches, increases the reliability risk. Also, typical mobile applications require stacking a memory die within the package without increasing the total package height. These combinations magnify the stress on back-end-of line (BEOL) stack and bump interconnection-especially on a thin coreless substrate which greatly influence extreme low-K dielectrics (ELK) fragility.

This paper describes the qualification of the 7nm silicon (Si) BEOL stability on thin coreless embedded trace substrate (ETS) with smaller solder ball pitch and a high die to package aspect ratio. In our previous experience, coreless material is generally prone to warpage due to absence of the core that supports the package rigidity. Therefore, controlling and minimizing warpage at room and elevated temperature is crucial, as the stress propagates into the BEOL, resulting in a significant impact on the chip reliability, especially for ELK structures. Simulation of thermal and mechanical stress in Finite Element Modeling (FEM) was completed to confirm warpage behavior. Shadow Moiré was documented under temperature loading and package coplanarity empirical data was collected.

Within the development phase, the package warpage was successfully reduced and coplanarity on thin coreless substrate was within specification. Significant improvement is attributed to mold compound higher coefficient of thermal expansion (CTE) and lower elastic modulus. Multiple reliability tests in accordance with JEDEC standard was conducted. Results confirmed the BEOL stack integrity and all related tests passed.

Biography
Eduardo De Mesa received B.S Mechanical Engineering from Mapua Institute of Technology, Manila,

Philippines. Currently, working under Technology Enablement Group engaged in advanced package development at Intel Deutschland Gmbh.

Active Mold Packaging for novel Antenna-in-Package interconnection and manufacturing

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Abstract
IC package designers wishing to benefit from space saving Antenna-in-Package (AiP) technologies rely on an intricate selection of materials and interconnect processes to produce a self-contained integrated module. This paper presents a new way to reduce the production complexities of AIP by introducing a novel homogeneous packaging technology: Active Mold Packaging (AMP).
Active Mold Packaging directly establishes electrical connections, such as patch antennas, signal vias, and Electro-Magnetic-Interference (EMI) shields for RF applications on the surface and in the volume of the encapsulating Epoxy Mold Compound (EMC). Advancing the development of multifunctional compact devices, AMP in essence transforms the passive and undeveloped real-estate of the EMC into an active carrier of package functionality.
A 2.5D interconnect technology to simplify AiP designs and EMI shielding will be presented. AMP integrates familiar process steps: molding of EMCs, Laser Direct Structuring and direct electro-less and galvanic plating. In combination the processing steps result in a robust scalable manufacturing solution, AMP. AMP is uniquely suited for the production of AiP but also a foundation design platform for other novel IC packages. Critical process attributes of AMP are discussed and used to propose a commercial AMP-AiP model. Measuring the influence of key design elements of an AMP fabricated EMC micro strip antenna and EMI shield within the 5G radio frequencies; sub-6GHZ, mm-wave, and beyond 5G (« B5G ») ISM bands yields strategies for implementing the AMP technology. Consideration is granted to the impact of the LDS activator, the laser structuring parameters, and electroless plating factors on the model devices. Lastly, the proposed commercialization of the AMP-AiP is modelled through a cost-model comparison.

Biography
M. Sc. Florian Roick, Business Development Manager Active Mold Packaging
Born in 1981. He holds a degree as Bachelor of Science in Applied Physics from Dublin Institute of Technology. And a degree as Master of Science in Electrical Engineering with focus on laser systems, laser physics and microsystems engineering from Hochschule Bremen.
Since 2006 employed at LPKF Laser & Electronics AG, until 2008 as application engineer for the StencilLaser business unit. Between 2008 and 2019 strategic product manager responsible for aligning the product portfolio with the needs and requirements of the PCB and SMT markets.
Since 2019 Business Development Manager for LPKF's Active Mold Packaging technology. That is to electrically functionalize the real-estate of the epoxy mold compound on the base of LPKF's patented Laser Direct Structuring (LDS) technology.
Co-inventor of the parametric stick-in and co-author of a variety of publications.

High throughput & high yield heterogeneous integration with implemented metrology for collective D2W Bonding

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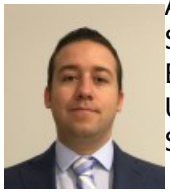
Abstract
Heterogeneous integration offers several advantages in performance gain, functionality increase as well as yield enhancement. Depending on the device architecture and level of integration, several integration methods at different manufacturing levels can be used to create heterogeneous integrated systems. Processing on die level is often practiced, leading in some cases to throughput and yield considerations. Collective die to wafer bonding can enable several integration processes on wafer level via using a reconstituted transfer carrier approach. Especially in hybrid and fusion bonding this method enables heterogeneous integration as processes such as plasma activation are better performed on wafer level for high throughput.
As for all semiconductor processes, collective die to wafer bonding demands suited and optimized measurement solutions for process monitoring and yield optimization. Fitting metrology combined with a feedback loop for production equipment is essential to increase yield of the whole integration process and an important factor in successful heterogeneous integration. Regarding metrology implementation, two scenarios are generally possible. One is the implementation of metrology within the bond equipment, which allows a quick reaction and the process parameters can be directly adjusted. The consideration of such implementation demands throughput matching for high equipment efficiency. The other implementation method is an external metrology tool, where the feedback is delayed, but on the other hand one metrology tool can serve several production tools.
In the presentation the process flow of collective die to wafer bonding will be discussed in more detail as well as the advantages and disadvantages of the two metrology implementation scenarios.

Biography
Elisabeth Brandl received her master in technical physics from the Johannes Kepler University Linz, Austria in Semiconductor and Solid State Physics. Since 2014, she has been responsible for Product Marketing Management for temporary bonding and metrology at EVG.

Vertical stacking of controller IC on a copper clip attached on MOSFET as a space-saving solution for high current switch e-fuse applications



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Abstract
Recently there has been an increasing demand for high-performance computing, mainly driven by data centers, online storage, cloud-based servers, and online software services. These applications require high computing power which drives high energy consumption, so the power systems employed need to run at extremely high efficiency and have small form factors, whilst offering very high reliability and minimal thermal losses during their deployment. This can be achieved by improving both the power semiconductor device technology, as well as the power packaging technology, such that maximum power performance and reliability can be extracted from the PCB area available.

Power MOSFET technology has evolved to reduce switching losses and allow high frequency switching. Power modules have also been developed to integrate MOSFET dies together with a controller IC in a single package to offer a small form factor solution. From an interconnect perspective, copper clip bonding began to replace wire bonding technology due to the lower resistance and parasitic inductances it offers compared to wire bonding. Whereas most multi-die power module packages employ a side-by-side die configuration due to the wire bonding interconnect method, copper clip packages allow for vertical die stacking, which results in a smaller package for the same power rating.

In this paper, we propose a QFN power module package solution for an electronic fuse (e-fuse) device in high-performance computing applications, comprised of a controller IC vertically stacked onto the copper clip used to create the interconnect between the MOSFET die and the lead frame. This approach provides a vertically integrated power module solution, offering a significantly reduced form factor versus a side-by-side power module approach or the use of two separate QFN packages for each die. Typical e-fuse applications need two separate QFN packages, for example, a 3mm x 3mm QFN for the controller IC and a 5mm x 6mm QFN for the MOSFET die, occupying a total of 39mm^2 of PCB area. Comparatively, a vertically stacked power module can be packaged in a 5mm x 5mm QFN occupying a total PCB area of 25mm^2, resulting in 36% less PCB area usage. The vertically stacked power module also offers excellent thermal performance despite the increased power density of the package. Thermal simulations performed using a 5mm x 6mm e-fuse package structure with 4.1W of combined power dissipation show that a Theta Ja of 25.3 ^{o}C/W and maximum temperatures of around 128.8^{o}C for the IC and 123.9^{o}C for the MOSFET are achieved under still air conditions.

The assembly process flow will also be discussed in more detail, with focus on critical process steps such as vacuum reflow to ensure minimum voiding in the solder interconnects between MOSFET and lead frame, and copper clip and MOSFET. Examples of actual devices will also be shown. UTAC's outlook on more advanced power modules will also be shared, showing proposals for packages with increased complexity using three dies and copper clips in a vertically stacked configuration for smart power stage applications with reduced footprint requirements.

Biography
Alastair Attard is Senior Technical Program Manager and Assembly Business Development at UTAC Group. He has a Bachelor's degree in Mechanical Engineering and an Executive MBA from the University of Malta.

He has over 14 years of experience in the assembly & test of semiconductor devices.

Prior to joining UTAC, Alastair worked at STMicroelectronics Malta from 2006 until 2011, first as a Process Engineer on flip chip assembly for SiP and later as a Package Development Senior Engineer for SiP and MEMS packages. He later joined Besi in 2011, where he was Manager of the Process Development group until 2018.

At UTAC, he is responsible for Technical Program Management and Assembly Business Development in the European region, with main focus on Automotive, Industrial, SiP, Power and MEMS areas.

New solutions for plasma dicing, and new solutions for processing of SiC wafers ranging from ingot splitting, grinding, polishing to high speed and chipping free dicing.

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DISCO
Kiru·Kezuru·Migaku Technologies

Abstract
Wafer thinning (Kezuru and Migaku) and dicing (Kiru) is essential for advanced packaging, for achieving narrow street widths and for making thin dies for 3D-packaging. New solutions on plasma dicing in combination with latest tapes and grinding technology enable the supply of perfect top side, back side and side wall quality on dies in thickness range from 20 – 150 µm.
Plasma dicing has various advantages comparing to the conventional dicing. However, during the plasma dicing process the sensitive wafer front can be at risk due to the surface being exposed to plasma gas. It is common to protect the wafer front surface by photoresist in the wafer fab, which increases the cost and the processing steps.
DISCO has developed a special surface protection film and a total new processing flow for plasma dicing to overcome these issues.

SiC is getting more and more important for the energy efficient devices. Since SiC is a very expensive material DISCO focuses on technologies for gaining as many as possible wafers and dies of outstanding quality out of it.
SiC ingot splitting by KABRA:
KABRA is a new method for SiC-ingot slicing by using a laser instead of a wire saw. In this process, a special layer is made inside of the ingot by laser irradiation and then the wafer is split from the ingot. 40% more wafers are obtained out of one ingot compared to conventional method.
SiC ingot and wafer grinding and polishing:
After splitting the wafer from the ingot, the ingot side and the wafer side need to be ground and polished. DISCO has developed grinding wheels and polishing pads (E Pad) suitable for wafer manufactures and device makers.
SiC wafer dicing by blade or laser:
To obtain more numbers of dies from a wafer, cutting streets can be reduced down to 50 µm and less. With our special technologies cutting speed and quality have been greatly improved, too.

Biography
Gerald Klug has studied business-engineering at the University of Siegen and graduated as Diplom-Engineer in 1998.
He started his carrier as a designer and project engineer of steel cutting lines at a globally leading German machine manufacturing company.
At the end of 2000, he joined DISCO as Sales Engineer. Meanwhile he has been working for DISCO for 19 years and is nowadays operating as General Sales Manager for the territory of Europe.

Virtual Prototyping for System-in-Package with Heterogeneous Integration - Enabler for faster Time-to-Market

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Abstract
Heterogeneous Integration in System-in-Package (SiP) based on Fan-Out Wafer Level Technologies allows to meet various requirements such as improved performance, smaller form-factor, functional safety and low cost for upcoming new applications. Due to the thermo-mechanical stresses leading to device failure, the reliability risks must be assessed during the development of new products aiming for a design optimized for reliability. Virtual Prototyping (VP) based on Finite Element (FE) simulation allows the analysis of the thermo-mechanical situation during fabrication, tests and service within short time, allowing shorter development time. However, it requires parametric FE models, precise material and experimental data for validation. Because of this initial investment, it is advised to develop the VP schemes in a way that they are able to cover a wide variety of future products.
The talk will present a modular system of parametric FE models that enables virtual reliability assessments of various SiP products based on Fan-Out Technologies such as WLSiP, eWLB-PoP, RCP, InFO, FOPLP, WFOP, SiWLP and SWIFT-PoP [1][2]. By combination of common packaging components like die, mold, redistribution layers, solder balls, vias, integrated passives, and boards from the library of pre-calibrated parametric FE models in ANSYS, digital twins of a large number of individual package configurations can readily be generated, e.g. 2D, 2.5D and 3D/PoP. The talk highlights the flexibility of the modular system of parametric FE models by four very different industrial packages: Radar sensor, Silicon photomultiplier, Automotive inertial sensor and Camera module. The VP scheme for a new pad design of a multi-chip SiP sensor is demonstrated in detail to show the great support that virtual optimization and qualification schemes can provide. They can reduce Time-to-Market of new SiP products by 50%-75%.

References
[1] https://doi.org/10.1109/ESTC.2018.8546352
[2] https://doi.org/10.1115/1.4043341

Biography
Ghanshyam Gadhiya received his M.Sc. degree in Micro and Nano Systems, with a specialization in Finite element analysis of power module from Technical university of Chemnitz in 2013. Since 2014, he is working as a scientific researcher at the Micro materials center, Fraunhofer ENAS. His main research focus includes parametric finite element modelling, thermo-mechanical simulation and optimization of microelectronics packages using FE-program ANSYS. He has been also involved with several industrial projects for residual stress, humidity and vibrational analysis. His current research interests include fan-out wafer level packaging technology, system-in-package, virtual prototyping and micro-electronics failure analysis.

Innovative Packaging and Evaluation Approach for an Universal Sensor Platform

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Abstract
This article presents an innovative packaging and evaluation approach for a newly developed Universal Sensor Platform (USEP) based on a system in package RISC-V integrated microcontroller with a top-level functionalized system in package design. Specific functions of the sensor platform are assigned to four different physical levels in the whole integration concept. The technical implementation of the functional requirements requires innovative, technological solutions in the packaging and interconnection technology (AVT) but also new approaches for testing methods and infrastructure across the different levels.
Starting from a bare die, inclusion of package co-design, new assembly and interconnection techniques, up to the provision of the evaluation and testing of the platform system, the increasing complexity of this research projects in microelectronics becomes apparent.

In the final step of finalizing the system in package solution, the sensors are applied to the functionalized package surface. This enables the system to directly measure various parameters such as temperature, humidity and pressure. The electrical connection of the components is done on a multilayer redistribution layer, which is applied to the mold material of the package and connected to the underlying system core with through package vias. For testing, a modular evaluation board is available, which allows the connection of an FPGA-based emulation environment. Furthermore, various test adapters can be connected to the data bus, thus significantly increasing the modular testability. A test socket detachable from the circuit board connects the manufactured modules with their 256-BGA footprint with all electrical operation and debug signals and plays a central role for the actual chip test because it enables short testing and configuration cycles.

Biography
Carsten Brockmann studied Technische Informatik at the Technical University of Berlin and received his diploma in 2008. He worked as a scientist at the Forschungsschwerpunkt Technologien der Mikroperipherik in the field of wireless sensor nodes until 2014 when he changed to Fraunhofer Institute for Reliability and Microintegration. In different national and international research projects he proceeded with his research work and became the group manager for sensor nodes and embedded microsystems in 2015.