Advanced Packaging Forum

S. Kroehnert
President and Founder
ESPAT-Consulting - Steffen Kroehnert, Dresden, Germany

Biography
Steffen Kroehnert is President & Founder of ESPAT-Consulting based in Dresden, Germany. He is providing a wide range of consulting services around Semiconductor Packaging, Assembly, and Test, mainly for customers in Europe. Until June 2019, he worked for more than 20 years in different R&D, engineering, and management positions at large IDMs and OSATs in Germany and Portugal, namely Siemens Semiconductors, Infineon Technologies, Qimonda, NANIUM and Amkor Technology, where he most recently served as Senior Director Technology Development. Since 2016 Steffen has chaired the European SEMI integrated Packaging, Assembly, and Test - Technology Community (ESiPAT-TC). Steffen has authored or co-authored 23 patent filings and many technical papers in the field of Packaging Technology. He also co-edited the book “Advances in Embedded and Fan-Out Wafer Level Packaging Technologies”. He is an active member of several technical and conference committees of IEEE EPS, IMAPS, SEMI Europe, and SMTA. Steffen holds an M.Sc. in Electrical Engineering and Microsystems Technologies from the Technical University of Chemnitz, Germany.

The Growing Momentum of Heterogeneous Integration

W. (. Chen
ASE Fellow & Sr. Technical Advisor
ASE Group, Tempe, United States

Abstract
coming soon

Biography
Dr. William (Bill) Chen is chief architect for technology strategy, lead mentor, and hands-on engineer for strategy implementation at ASE Group, blazing the trail for packaging innovators and innovation across the electronic industry ecosystem. His strategy portfolio includes SiP, copper wire-bond, 2.5D packaging, & fan-

out wafer-level packaging, all game changing technologies brought to high volume production to address new demands for emerging applications in IoT, cloud computing, autonomous automotive, AI and smart mobility.

Previously, Bill spent over thirty-five years at IBM, where he pioneered the concept and implementation of predictive verified modeling incorporating materials science, micromechanics and finite element for design and manufacturing benefiting generations of packaging products, from BGAs to mainframe systems.

Bill is a past president of the IEEE Electronics Packaging Society and was the co-chair of the Packaging & Assembly TWG at ITRS until its closure by SIA in 2016. He now chairs the Heterogeneous Integration Roadmap, co-sponsored by three IEEE Societies (EPS, EDS & Photonics) together with SEMI and ASME EPPD. He is the recipient of IEEE Electronics Packaging Technology Field Award and ASME InterPACK Award. Besides being ASE Fellow, he has also been elected IEEE Fellow and ASME Fellow.

Challenges for Heterogeneous Integration in Package – Applications Driving Materials and Processes towards Diversity

T. Meyer
Lead Principal Engineer
Infineon Technologies, Regensburg, Germany

Abstract
ABSTRACT

Challenges for Heterogeneous Integration in Package –
Applications driving Materials and Processes towards Diversity

by Thorsten Meyer and Klaus Pressel
Infineon Technologies AG, Regensburg

Heterogeneous Integration is a major technology driving force for microelectronic systems. More-than-Moore (MtM), System-in-Package (SiP), as well as 3D high-density integration technologies are a prerequisite for enabling the design of compact microelectronic devices. Heterogeneous Integration refers to the integration of separately manufactured components into a higher level of assembly, which is providing enhanced functionality and operating characteristics. In this definition, components should be taken to mean any unit, whether individual die, MEMS or sensor device, passive component and assembled package or sub-system, that are integrated into a single package (see e.g. Heterogeneous Integration Roadmap published for the first time October 2019).
The requirements for integration of the mentioned components are differing strongly depending on application. Integration of power devices requires thick copper with large area connections for thermal properties and current carrying capabilities, e.g. a solution for vertical current flow. For mm-wave applications, precise knowledge of material parameters and dimensions is required to fabricate leading edge devices like radar or LIDAR for future autonomous driving. Logic integration typically requests for many short interconnects, fine line spaces and tight pad pitches in a horizontal arrangement of the contacts. MEMS and sensor devices often require a special protection and are sensitive in handling during production. Packaging often is customized to the application. In addition, the integration of passives, e.g. resistors, inductors, capacitors, as well as shielding capabilities or antennas require special packaging building blocks for an application tailored integration. All these different constraints lead to an extreme diversity of package solutions very difficult to tackle.
In this presentation, we will discuss the challenges and introduce potential solutions for different integrated applications. We will highlight the importance of virtual prototyping, chip-package-board/system co-design as well as reliability prediction, which require detailed understanding of material properties and their interfaces. Especially, we will emphasize the increasing importance of knowledge on material physics. For example, investing into physics of advanced failure analysis is a major enabler for faster and more reliable development of innovative devices. We will show examples of building blocks for different areas of integration, which we must develop for the supply of integrated packages for future applications. Heterogeneous integration combined with miniaturization capability, i.e. more functionality in smaller volume, will drive us in future microelectronics.

Biography
Thorsten Meyer is Lead Principal Engineer Package Concept Engineering at Infineon Technologies in Regensburg, Germany, responsible for New Package concepts. Until March 2015 he was leading the Package Technology and Innovation department at Intel Mobile Communications (IMC) in Regensburg. Prior joining IMC, he was overall project leader for the development of Wafer Level Packaging Technologies at Infineon in Regensburg and earlier in Dresden.

Thorsten is author of multiple publications and holds more than 150 patents and patent applications in the area of advanced packaging.

Packaging in Europe - Micro Balling on Chips with a High Ball-count for Space Applications - an Extension of the Process Capabilities at AEMtec

D. Negrea
SVP New Technologies
AEMtec GmbH, Berlin, Germany

Abstract
Packaging in Europe – and not in Asia - seems a strange business model. But it is not, if you consider the technology IP aspects, the challenges, the drive of some European industries (mainly the space industry) towards emancipation from the dominance of the US and Asian providers.

AEMtec started the internalization of the Wafer Back End solder balling technologies for 4 years and increased permanently the portfolio of customers and products, mainly in the high sensitivity products, considered by our European customers and strategically critical to their business. The vision of a one-stop-shop for core technology products, for small and medium quantities became reality.

The requirements specific to the "New space" projects target in the first line the cost reduction of all components but without compromising on the required quality and performance.
The drive to miniaturization, considering the costs of the payload for satellites, leads to the use of chips with a high Ball count (whereby 5000 and more are rather the rule than the exception).
We like to focus in our presentation on the challenges, both from a technical as well as from a regulatory perspective for the use of the non-hermetic, soldered, flip chip technology for space applications on the technological, down-to-earth, explanations concerning the implementation of the wafer back end processes.

AEMtec actively participates in different projects and workgroups around ESA.
By qualifying in house processes, having extremely stringent requirements in terms of reliability, AEMtec can guarantee very high Cpk levels for all relevant processes, followed in the SPC.

The level of quality which needs to be achieved for the space applications, opens the way to multiple other types of applications, including high density large size chips for companies active in the detection technology, but also for applications in the automotive industry.

So far the achieved performances of the wafer back end solder bumping line, which comprises all the necessary stages of the process, from wafer inspection to balling, washing, dicing, and which has been validated on multiple tens of thousands of chips, allow the use of micro balls with a diameter of 50 µm, on chips with up to 12,000 connections.

Of course this miniature size of balls and the physical size of the chips cause a high unitary stress/strain on the balls, due to the difference in thermal coefficient in normal use - therefore the major importance of the cleanness and of the underfill processes. The tests performed for the qualification go far beyond the normal RTV cycles, thus guaranteeing a flawless quality.

Biography
For information purposes only

F. Kuechenmeister
PMTS

GLOBALFOUNDRIES, POSTFAB NPI & CPI,
Dresden, Germany

Biography

Dr. Frank Kuechenmeister received a Master degree in Polymer Chemistry and a doctorate in Chemistry from the University of Technology in Dresden, Germany. He held post-doctoral appointments at the Departments of Polymer Science at the ETH Zuerich, Switzerland, the University of Massachusetts in Amherst, USA and the Department of Electrical Engineering and Micro Systems at the University of Technology in Dresden, Germany. He joined AMD in 1999, which converted to become GLOBALFOUNDRIES in 2008 as process engineer working the area of C4 bumping. He was promoted to principal member of technical staff in 2016. He currently leads the chip-packaging interaction team and coordinates all related efforts throughout all technology nodes at GLOBALFOUNDRIES.

Flip-Chip Scale Package(FCCSP) Process Characterization and Reliability of Coreless Thin Package with 7nm TSMC Si

E. De Mesa
Package Engineer
Intel Deutschland GmbH, Munich, Germany

Abstract
Advanced silicon nodes are continuously pushing the cutting edge of assembly technology for coreless thin packages used in mobile and electronic products to allow better power delivery, electrical performance, and higher routing capability. This results in a higher number of I/O and integration flexibilities. Furthermore, integration of a large die size in a smaller package with finer bump and ball pitches, increases the reliability risk. Also, typical mobile applications require stacking a memory die within the package without increasing the total package height. These combinations magnify the stress on back-end-of line (BEOL) stack and bump interconnection-especially on a thin coreless substrate which greatly influence extreme low-K dielectrics (ELK) fragility.

This paper describes the qualification of the 7nm silicon (Si) BEOL stability on thin coreless embedded trace substrate (ETS) with smaller solder ball pitch and a high die to package aspect ratio. In our previous experience, coreless material is generally prone to warpage due to absence of the core that supports the package rigidity. Therefore, controlling and minimizing warpage at room and elevated temperature is crucial, as the stress propagates into the BEOL, resulting in a significant impact on the chip reliability, especially for ELK structures. Simulation of thermal and mechanical stress in Finite Element Modeling (FEM) was completed to confirm warpage behavior. Shadow Moiré was documented under temperature loading and package coplanarity empirical data was collected.

Within the development phase, the package warpage was successfully reduced and coplanarity on thin coreless substrate was within specification. Significant improvement is attributed to mold compound higher coefficient of thermal expansion (CTE) and lower elastic modulus. Multiple reliability tests in accordance with JEDEC standard was conducted. Results confirmed the BEOL stack integrity and all related tests passed.

Biography
Eduardo De Mesa received B.S Mechanical Engineering from Mapua Institute of Technology, Manila, Philippines. Currently, working under Technology Enablement Group engaged in advanced package development at Intel Deutschland Gmbh.

Active Mold Packaging for Novel Antenna-in-Package Interconnection and Manufacturing

F. Roick
Business Development Active Mold Packaging
LPKF Laser & Electronics AG, Garbsen, Germany

Abstract
IC package designers wishing to benefit from space saving Antenna-in-Package (AiP) technologies rely on an intricate selection of materials and interconnect processes to produce a self-contained integrated module. This paper presents a new way to reduce the production complexities of AIP by introducing a novel homogeneous packaging technology: Active Mold Packaging (AMP).
Active Mold Packaging directly establishes electrical connections, such as patch antennas, signal vias, and Electro-Magnetic-Interference (EMI) shields for RF applications on the surface and in the volume of the encapsulating Epoxy Mold Compound (EMC). Advancing the development of multifunctional compact devices, AMP in essence transforms the passive and undeveloped real-estate of the EMC into an active carrier of package functionality.
A 2.5D interconnect technology to simplify AiP designs and EMI shielding will be presented. AMP integrates familiar process steps: molding of EMCs, Laser Direct Structuring and direct electro-less and galvanic plating. In combination the processing steps result in a robust scalable manufacturing solution, AMP. AMP is uniquely suited for the production of AiP but also a foundation design platform for other novel IC packages.
This paper investigates the capabilities of Active Mold Packaging towards mmWave application. First the dielectric properties of three different AMP-EMCs are measured in the D-band. Second, the reflection coefficient S11, as well as the H- and E-plane radiation patterns are determined for a set of AMP manufactured 60 GHz bow-tie slot and dual dipole antennas. Where the measured results are compared to the design values and differences are discussed. And third, the D-band EMI shielding effectiveness of the electroless plated Cu/Ni/Au layer on the surface of three different AMP-EMCs is measured.
Lastly, AMP is proposed in a commercially available AiP, benefitting from increased manufacturing simplicity and lower cost.

Biography
M. Sc. Florian Roick, Business Development Manager Active Mold Packaging
Born in 1981. He holds a degree as Bachelor of Science in Applied Physics from Dublin Institute of Technology. And a degree as Master of Science in Electrical Engineering with focus on laser systems, laser physics and microsystems engineering from Hochschule Bremen.
Since 2006 employed at LPKF Laser & Electronics AG, until 2008 as application engineer for the StencilLaser business unit. Between 2008 and 2019 strategic product manager responsible for aligning the product portfolio with the needs and requirements of the PCB and SMT markets.
Since 2019 Business Development Manager for LPKF’s Active Mold Packaging technology. That is to electrically functionalize the real-estate of the epoxy mold compound on the base of LPKF’s patented Laser Direct Structuring (LDS) technology.
Co-inventor of the parametric stick-in and co-author of a variety of publications.

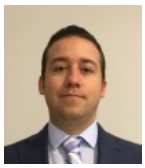
High Throughput & High Yield Heterogeneous Integration with Implemented Metrology for Collective D2W Bonding

E. Brandl
Business Development Manager
EVG, St Florian am Inn, Austria

Abstract
Heterogeneous integration offers several advantages in performance gain, functionality increase as well as yield enhancement. Depending on the device architecture and level of integration, several integration methods at different manufacturing levels can be used to create heterogeneous integrated systems. Processing on die level is often practiced, leading in some cases to throughput and yield considerations. Collective die to wafer bonding can enable several integration processes on wafer level via using a reconstituted transfer carrier approach. Especially in hybrid and fusion bonding this method enables heterogeneous integration as processes such as plasma activation are better performed on wafer level for high throughput.
As for all semiconductor processes, collective die to wafer bonding demands suited and optimized measurement solutions for process monitoring and yield optimization. Fitting metrology combined with a feedback loop for production equipment is essential to increase yield of the whole integration process and an important factor in successful heterogeneous integration. Regarding metrology implementation, two scenarios are generally possible. One is the implementation of metrology within the bond equipment, which allows a quick reaction and the process parameters can be directly adjusted. The consideration of such implementation demands throughput matching for high equipment efficiency. The other implementation method is an external metrology tool, where the feedback is delayed, but on the other hand one metrology tool can serve several production tools.
In the presentation the process flow of collective die to wafer bonding will be discussed in more detail as well as the advantages and disadvantages of the two metrology implementation scenarios.

Biography
Elisabeth Brandl received her master in technical physics from the Johannes Kepler University Linz, Austria in Semiconductor and Solid State Physics. Since 2014, she has been responsible for Product Marketing Management for temporary bonding and metrology at EVG.

Vertical Stacking of Controller IC on a Copper Clip Attached on MOSFET as a Space-saving Solution for High Current Switch e-fuse Applications



A. Attard
Sr. Technical Program Manager & Assembly Business Development
United Test and Assembly Center Ltd, Singapore, Singapore

Abstract
Recently there has been an increasing demand for high-performance computing, mainly driven by data centers, online storage, cloud-based servers, and online software services. These applications require high computing power which drives high energy consumption, so the power systems employed need to run at extremely high efficiency and have small form factors, whilst offering very high reliability and minimal thermal losses during their deployment. This can be achieved by improving both the power semiconductor device technology, as well as the power packaging technology, such that maximum power performance and reliability can be extracted from the PCB area available.

Power MOSFET technology has evolved to reduce switching losses and allow high frequency switching. Power modules have also been developed to integrate MOSFET dies together with a controller IC in a single package to offer a small form factor solution. From an interconnect perspective, copper clip bonding began to replace wire bonding technology due to the lower resistance and parasitic inductances it offers compared to wire bonding. Whereas most multi-die power module packages employ a side-by-side die configuration due to the wire bonding interconnect method, copper clip packages allow for vertical die stacking, which results in a smaller package for the same power rating.

In this paper, we propose a QFN power module package solution for an electronic fuse (e-fuse) device in high-performance computing applications, comprised of a controller IC vertically stacked onto the copper clip used to create the interconnect between the MOSFET die and the lead frame. This approach provides a vertically integrated power module solution, offering a significantly reduced form factor versus a side-by-side power module approach or the use of two separate QFN packages for each die. Typical e-fuse applications need two separate QFN packages, for example, a 3mm x 3mm QFN for the controller IC and a 5mm x 6mm QFN for the MOSFET die, occupying a total of 39mm^2 of PCB area. Comparatively, a vertically stacked power module can be packaged in a 5mm x 5mm QFN occupying a total PCB area of 25mm^2, resulting in 36% less PCB area usage. The vertically stacked power module also offers excellent thermal performance despite the increased power density of the package. Thermal simulations performed using a 5mm x 6mm e-fuse package structure with 4.1W of combined power dissipation show that a Theta Ja of 25.3 ^{o}C/W and maximum temperatures of around 128.8^{o}C for the IC and 123.9^{o}C for the MOSFET are achieved under still air conditions.

The assembly process flow will also be discussed in more detail, with focus on critical process steps such as vacuum reflow to ensure minimum voiding in the solder interconnects between MOSFET and lead frame, and copper clip and MOSFET. Examples of actual devices will also be shown. UTAC's outlook on more advanced power modules will also be shared, showing proposals for packages with increased complexity using three dies and copper clips in a vertically stacked configuration for smart power stage applications with reduced footprint requirements.

Biography
Alastair Attard is Senior Technical Program Manager and Assembly Business Development at UTAC Group.

He has a Bachelor's degree in Mechanical Engineering and an Executive MBA from the University of Malta. He has over 14 years of experience in the assembly & test of semiconductor devices.

Prior to joining UTAC, Alastair worked at STMicroelectronics Malta from 2006 until 2011, first as a Process Engineer on flip chip assembly for SiP and later as a Package Development Senior Engineer for SiP and MEMS packages. He later joined Besi in 2011, where he was Manager of the Process Development group until 2018.

At UTAC, he is responsible for Technical Program Management and Assembly Business Development in the European region, with main focus on Automotive, Industrial, SiP, Power and MEMS areas.

A. Miller
Department Director
IMEC, 3D and Si Photonics Technology Development, Leuven, Belgium

Biography

Andy Miller graduated from the University of Glasgow in 1995 with a Honours degree in Physics. He immediately started work as a process engineer at NEC Semiconductors (UK) Ltd in lithography. In 2000 he moved to Filtronic Compound Semiconductors Limited as lead lithography engineer. In 2008 he joined the Advanced Lithography program at IMEC, focused on alternative materials for Double Patterning.
In 2009 he became the Team Leader for More Than Moore lithography development at imec, quickly expanding the team to include wafer level bonding, die bonding and metrology. In 2012 he took up the position of Group Leader for technology development within the 3D Integration program. He is currently the Department Director for 3D and Si Photonics technology development at imec.

Heterogeneous Integration Test Impacts

V. Pancholi
Seniorr Director, Test Technology
Amkor Technology, Inc., Tempe, Arizona, United States

Abstract
Moore's law is not dead, nor is it dying – it is being reborn in the form of Heterogeneous Integration (HI). HI is a powerful design innovation that improves manufacturing yield without sacrificing quality. HI creates semiconductor devices by connecting chiplets and dielets from various fabrication nodes. System-in-Package (SiP) designs employ HI in various forms to reduce product footprint, increase product functionality and lower costs. Prior methodologies consisted of building one large die containing most of the needed functionality for a product. As dies get larger, they have a higher probability of being impacted by inherent wafer defect density, and therefore, are prone to a lower yield. Realizing this phenomenon, integrated circuit (IC) designers split the functionality of the large die into small chiplets or dielets. Leveraging the advantages of HI, SiP designers build modules containing 5/7-nm silicon technology for high end ASICS, while lower complexity functions continue to be built using lower cost, larger, silicon nodes.
The switch to HI in SiP modules introduces unique testing challenges, where a test engineer needs to have a broad spectrum of expertise, covering the testing of: antennas, radio frequency (RF) devices, modulators and demodulators (modems), baseband, high-speed digital, serializer/deserializer (SerDes), photonics, power control and distribution, embedded actives/passives and interconnect technologies. This expertise must be applied to Wafer Probe Test, Partially Assembled Test (PAT), Final Test (FT) and System-Level Test (SLT).
As assembly techniques vary, so do the challenges of package-level testing. Therefore, the scope of this talk will be limited to one assembly technique but can be adapted to other assembly techniques. To add relevance, this talk will focus on test while building a hypothetical SiP - 5G Micro-Base Station (MBS) using HI. The 5G MBS will be built using four HI sub-modules, one for the processor, two RF sub-modules and one power, MEMS and accessories module, all of which will finally be assembled on a single motherboard.
The test methods for the processor module will cover high speed testing of reconstituted multi-chip ASIC wafers, testing Through Silicon Via (TSV) interposer and testing the processor subassembly using PAT and SLT. The RF sub modules test describes SLT and antenna in package (AiP), including testing phased array antennas with Over-the-Air (OTA) Testing. The last module will cover SLT for the MEMS & DC subsystems. The final SiP assembly will be tested using SLT.
Through this talk, the attendees will gain an insight into the challenges of testing a complex HI SiP system.

Biography
Vineet joined Amkor in Jan. 2019 and currently leads test technology development for 5G RF and high-speed digital production test methodologies. Before joining Amkor, Vineet worked in test development at Microchip Technology. Prior, he spent 19 years at Intel in a variety of test roles, including tester supplier management, test technology development (burn-in, final and system level test) and RF tester architect. Vineet holds a patent on semiconductor device testers and has earned master's degrees in physics and electrical engineering from Arizona State University.

Fast, 100% 3D Bump Metrology and Inspection to Improve Yields of 3D System Integration

T. Skunes
VP R&D
CyberOptics Corporation, Minneapolis, United States

Abstract
Advanced Packaging (AP) and wafer level packaging (WLP) continue to be among the most dynamic and rapidly evolving areas of semiconductor development and manufacturing. Most of these new processes take advantage of the third dimension, going vertical to continue packing more computing power into less space while circumventing the difficulties posed by further reductions in two-dimensional size. Packaging stacks include various configuration of single or multiple chips, interposers, flip chips and substrates, but in almost all cases, they rely on some form of bump to make the vertical connections between these components. The bumps may be solder balls, a technology that has migrated down from board level assembly and surface mount technology (SMT) or copper pillars or microbumps, formed with processes that have migrated up from the front end. Horizontal connections within packages are made by redistribution lines, also fabricated with front-end like processes. The result has been the development of a process/size regime sometimes called the middle-end, populated by hybrid processes and feature sizes ranging from 10 microns to 100 microns.

As the processes and features they create have become smaller and more complex, manufacturers face an increasing need for high-precision inspection and measurement to detect defects and improve process control. This need is amplified by the fact that these processes use expensive known good die, making the cost of failure extremely high. Like middle-end fabrication process, metrology and process control technologies have also migrated up from the front-end and down from assembly. Bump metrology is fundamentally three-dimensional. Bump height is just as important as size and location. Controlling bump height, both absolute and relative to neighboring bumps (coplanarity), is critical to ensuring good, reliable connections between stacked components.

Phase shift profilometry (PSP) is widely used for 3D automated optical inspection (AOI) by electronics manufacturers assembling printed circuit boards (PCB) with surface mount technologies (SMT). PSP is also used for solder paste inspection (SPI) by PCB manufacturers, and for dimensional measurements typically performed by coordinate measurement machines (CMM) in a variety of applications. PSP measurements are highly accurate and can be orders of magnitude faster than alternative methods. However, conventional PSP measurements can be significantly degraded by inaccuracies caused by multiple reflections between shiny surfaces on the inspected object. Effective suppression of these reflections is critical for accurate measurements.

Multiple Reflection Suppression™ (MRS™) sensor technology addresses this challenge by comparing data from multiple perspectives and fringe frequencies to identify and reject these spurious signals. The MRS sensor's unique optical architecture and the system's proprietary image fusing and processing algorithms provide accurate 3D characterization that is several times faster than conventional PSP. The NanoResolution MRS sensor has been developed for advanced packaging processes control in what has been called the "middle-end" of the manufacturing process, where traditionally front-end and back-end processes overlap. The MRS sensor integrated into CyberOptics' WX3000™ system provides sub-micrometer accuracy on features as small as 25µm. And, while retaining its ability to reject spurious multiple reflections, it adds the ability to capture and analyze specular reflections from shiny surfaces of solder balls, bumps and pillars, thus allowing accurate inspection and 3D metrology of these critical packaging features.

The MRS sensor is 2-3X faster than alternative technologies. With data processing speeds in excess of 75 million 3D points per second, it delivers production-worthy throughput greater than 25 wafers (300mm) per hour. Complete 100% 3D/2D inspection can be accomplished at high speed for bump metrology, vs. the current practice of sampling approach. Both 3D/2D data is attained at the same time vs. time-consuming alternate methods that require separate scans for 3D and 2D.

Keywords: High-precision 3D sensors, Multiple Reflection Suppression (MRS) Sensors, 2D/3D Inspection and Measurement Sensors, Wafer-Level and Advanced Packaging Metrology and Inspection Systems, CyberOptics

Biography

Timothy Skunes is the VP R&D at CyberOptics Corporation. He holds a M.EE, Optics and Electrical Engineering from the University of Minnesota. Timothy has been involved with the design and development of advanced 3D sensors for over 30 years. He holds 22 U.S. patents for optical measurement systems, optical manufacturing, and fiber optics devices. Previously, he was the Director of Product Development for CyberOptics from 2003 to May 2010; Vice President, Systems Development, Avanti Optics Corporation from 1999-2003; and Research Manager, CyberOptics Corporation from 1997-1999.

Virtual Prototyping for System-in-Package with Heterogeneous Integration - Enabler for faster Time-to-Market

G. Gadhiya
Research Associate
Fraunhofer ENAS, Chemnitz, Germany

Abstract
Heterogeneous Integration in System-in-Package (SiP) based on Fan-Out Wafer Level Technologies allows to meet various requirements such as improved performance, smaller form-factor, functional safety and low cost for upcoming new applications. Due to the thermo-mechanical stresses leading to device failure, the reliability risks must be assessed during the development of new products aiming for a design optimized for reliability. Virtual Prototyping (VP) based on Finite Element (FE) simulation allows the analysis of the thermo-mechanical situation during fabrication, tests and service within short time, allowing shorter development time. However, it requires parametric FE models, precise material and experimental data for validation. Because of this initial investment, it is advised to develop the VP schemes in a way that they are able to cover a wide variety of future products.
The talk will present a modular system of parametric FE models that enables virtual reliability assessments of various SiP products based on Fan-Out Technologies such as WLSiP, eWLB-PoP, RCP, InFO, FOPLP, WFOP, SiWLP and SWIFT-PoP [1][2]. By combination of common packaging components like die, mold, redistribution layers, solder balls, vias, integrated passives, and boards from the library of pre-calibrated parametric FE models in ANSYS, digital twins of a large number of individual package configurations can readily be generated, e.g. 2D, 2.5D and 3D/PoP. The talk highlights the flexibility of the modular system of parametric FE models by four very different industrial packages: Radar sensor, Silicon photomultiplier, Automotive inertial sensor and Camera module. The VP scheme for a new pad design of a multi-chip SiP sensor is demonstrated in detail to show the great support that virtual optimization and qualification schemes can provide. They can reduce Time-to-Market of new SiP products by 50%-75%.

References
[1] https://doi.org/10.1109/ESTC.2018.8546352
[2] https://doi.org/10.1115/1.4043341

Biography
Ghanshyam Gadhiya received his M.Sc. degree in Micro and Nano Systems, with a specialization in Finite element analysis of power module from Technical university of Chemnitz in 2013. Since 2014, he is working as a scientific researcher at the Micro materials center, Fraunhofer ENAS. His main research focus includes parametric finite element modelling, thermo-mechanical simulation and optimization of microelectronics packages using FE-program ANSYS. He has been also involved with several industrial projects for residual stress, humidity and vibrational analysis. His current research interests include fan-out wafer level packaging technology, system-in-package, virtual prototyping and micro-electronics failure analysis.

Innovative Packaging and Evaluation Approach for an Universal Sensor Platform

C. Brockmann
Group Manager Sensor Nodes and Embedded Microsystems
Fraunhofer Institut für Zuverlässigkeit und Mikrointegration, RF& Smart Sensor Systems, Berlin, Germany

Abstract
This article presents an innovative packaging and evaluation approach for a newly developed Universal Sensor Platform (USEP) based on a system in package RISC-V integrated microcontroller with a top-level functionalized system in package design. Specific functions of the sensor platform are assigned to four different physical levels in the whole integration concept. The technical implementation of the functional requirements requires innovative, technological solutions in the packaging and interconnection technology (AVT) but also new approaches for testing methods and infrastructure across the different levels.
Starting from a bare die, inclusion of package co-design, new assembly and interconnection techniques, up to the provision of the evaluation and testing of the platform system, the increasing complexity of this research projects in microelectronics becomes apparent.

In the final step of finalizing the system in package solution, the sensors are applied to the functionalized package surface. This enables the system to directly measure various parameters such as temperature, humidity and pressure. The electrical connection of the components is done on a multilayer redistribution layer, which is applied to the mold material of the package and connected to the underlying system core with through package vias. For testing, a modular evaluation board is available, which allows the connection of an FPGA-based emulation environment. Furthermore, various test adapters can be connected to the data bus, thus significantly increasing the modular testability. A test socket detachable from the circuit board connects the manufactured modules with their 256-BGA footprint with all electrical operation and debug signals and plays a central role for the actual chip test because it enables short testing and configuration cycles.

Biography
Carsten Brockmann studied Technische Informatik at the Technical University of Berlin and received his diploma in 2008. He worked as a scientist at the Forschungsschwerpunkt Technologien der Mikroperipherik in the field of wireless sensor nodes until 2014 when he changed to Fraunhofer Institute for Reliability and Microintegration. In different national and international research projects he proceeded with his research work and became the group manager for sensor nodes and embedded microsystems in 2015.

P. Cockburn
Program Manager
Cohu, Inc., ISG, Verwood, United Kingdom

Biography
Peter Cockburn has worked in the ATE industry for over 30 years at Schlumberger, NPTest, Credence, LTX-Credence, Xcerra and now Cohu. He is currently responsible for several key interface projects including adding intelligence into test contactors to improve test cell efficiency and developing a range of high performance, low-cost interfaces for emerging 5G applications.
After developing realtime and GUI software for ATE systems, he moved into product marketing and launched several new SOC ATE systems and analog test options as well as providing marketing and sales support in USA, Asia and Europe.

As leader of the Test Cell Innovation team he was responsible for defining and delivering complete test cells to customers to reduce cost, increase uptime and improve quality when testing pressure and motion sensors, microphones and wafer-level packages.
He has an Engineering degree from the University of Southampton, UK.

Heterogeneous Integration - The New Driver of Innovation and Growth

R. Beica
Chief Sales Officer, Semiconductor Division
AT&S, Semiconductor Division, Leoben, Austria

Abstract
The explosive growth in data generated and computing needs, global network traffic and digital transformation are further driving the adoption of electronics and semiconductor devices. The need for more performing and smarter devices, with increased functionalities, that can address high bandwidth needs, faster speeds, parallel processing, with more efficient power consumption is driving the industry to further develop new and innovative technologies. While innovation in mobile devices continues, new emerging applications, such as IoT, Artificial Intelligence and 5G are expected to drive the next phase of innovation across the supply chain. The new driving forces are also shifting the importance in the industry from technology node scaling to system level integration.

This presentation will give an overview of the global market trends highlighting the major industry trends and applications, the increased need and growth of heterogeneous and system level integration and the solutions that AT&S is bringing to the market to address current and future market needs.

Biography
Rozalia Beica is currently the CSO of Semiconductor Division, focusing on semiconductor and module activities within AT&S. Prior to AT&S she had several executive and C-level roles with various organizations across the supply chain: electronic materials (Rohm and Haas Electronic Materials, Dow & DuPont), equipment (Semitool, Applied Materials and Lam Research), device manufacturing (Maxim IC) and market research & strategy consulting firm (Yole Developpement).

Rozalia is actively involved in various industry activities. Some of the current engagements include: Member of the Board of Governors for IEEE Electronics Packaging Society and Vice General Chair of 71th ECTC, Chair of the Heterogeneous Integration Roadmap WLP Technical Working Group, Chair of the Semi Strategic Materials Conference, Technical Chair of System in Package China Symposium, Advisory Board Member 3DinCites and IMPACT Taiwan. Past activities: IMAPS VP of Technology, General Chair IMAPS DPC, Program Director EMC3D Consortia, General Chair Global Semi & Electronics Forum, Technical Advisory Board Member SRC, several other memberships in industry committees. Rozalia has over 150 presentations & publications, including 3 book chapters on 3D Integration.

Rozalia has a M.Sc in Chemical Engineering (Romania), a M. Sc. In Management of Technology (USA) and a Global Executive MBA from IE Business School (Spain).

Coming soon

K. Hasegawa
General Manager Device Integration Materials Laboratory
JSR, Leuven, Belgium

Abstract
Coming soon

Biography
Koichi Hasegawa received Ph.D. degree in engineering from Osaka Prefecture University in 1999. His major at the university was inorganic materials science, especially focusing on sol-gel related materials. He has been working at Advanced Electronic Materials Laboratory in JSR Corporation Japan, and experienced various kinds of advanced electronic materials development like inorganic low-k dielectrics, plating photoresists, photo-sensitive dielectrics, temporary adhesives, LED related materials, CMP consumables, etc. During his carrier, he experienced a visiting scientist at University of Illinois at Urbana-Champaign (UIUC) for 2 years, for the research of self-alignment of inorganic spherical particles. From 2015, he has been assigned as a general manager of Device Integration Materials Laboratory in JSR Corporation. His current interests are in novel advanced packaging materials like photoresists for high density wiring and dielectrics for high frequency applications.

Enabling Assembly and Packaging Material Developments for Next Gen RF Devices, Antennas and Radars

R. de Wit
Business Development Manager EMEA
Henkel Belgium NV, Westerlo, Belgium

Abstract
Smart Electronics' market trends like 5G Telecom and Autonomous Driving are leading advanced semiconductor packaging innovations towards higher functionality, enhanced connectivity at higher frequencies, RF signal interference isolation (shielding), smaller form factors (miniaturization) and reduced power consumption. To meet these demands, semiconductor package designs continue to evolve towards MULTIPLE DIE using System-in-Package and Wafer Level architectures. Especially for next generation RF devices, antennas and radars, the thermo-mechanical, thermal resistance and (di)electric properties of the assembly and packaging materials play a key role as well as fast and low temperature processing/curing. This presentation will give an overview of the challenges and solutions from a semiconductor packaging material perspective based on recent customer experiences and ongoing developments to enable new designs. The focus will be on thermal performance of different die and lid attach assembly methods and thermal interface materials, EMI shielding effectiveness of thin silver layers, dielectric constant and loss factors of liquid wafer level encapsulants and underfills at 28-50 GHz and above, etc.

Biography
Ruud de Wit is responsible for managing Henkel's Semiconductor, Sensor & Consumer Electronics Assembly Materials business development within EMEA region. Ruud has a BSc degree in Mechanical Engineering followed by several polymer, sales and marketing courses. Ruud is working for Henkel since 1990 in multiple positions including technical customer support, quality assurance and engineering, and global semiconductor account and product management.

Development of a Foil based Flexible Interposer for Power Conditioning IC in Energy Autarkic Systems

E. Yacoub-George
Scientist
Fraunhofer EMFT, Flex, Munich, Germany

Abstract
The EU ECSEL project EnSO aims the development of autonomous micro energy sources (AMES) for innovative electronic devices that target key applications such as smart health, smart mobility and smart society. An AMES provides energy for sensors, data processing and data transmission and consists of micro storage element, energy harvester, smart charger and power conditioning IC. Smart integration of these building blocks to fabricate an AMES with an appropriate form factor was a key objective in the EnSO project.
Although in printed electronics, the PCB board is ususally fabricated with an innovative technology it is often still assembled with bulky and rigid SMD components. In such a case, some of the primary advantages such as conformability and flexibility that are commonly attributed to printed electronics are lost. In order to overcome this limitation, we developed a new package type called “flexible interposer”. It consists of a Cu wiring film fabricated in roll to roll, a thinned IC and a flexible polymeric mould cover. The interposer is designed with a QFN format and is characterized by a reduced thickness and some mechanical flexibility. The flexible interposer approach was developed and characterized for a daisychain chip and a commercial power conditioning IC of the latest generation from STMicroelectronics. The fabrication process was established with the daisychain chip to facilitate electrical characterization and reliability testing and was then adapted for the STBC15 IC. 30 interposer samples have been prepared and characterized. The obtained process yield indicates a robust fabrication process. Since all process steps are compatible with roll to roll production, we expect a high potential for up-scaling that offers the chance to close the gap between research and market.
The research results were obtained in the scope of EnSO project that has received funding from 1) EU under Grant Agreement no. 692482 and 2) BMBF with National Grant no. 16ESE0088.

Biography
Erwin Yacoub-George received his Ph. D in Chemistry (1994) at Technical University of Munich where he developed a production process for polysiloxane beads. Since 1994 he worked for the Fraunhofer Society in Munich. He started his research works on the development of optical biosensor systems. In 2002 he joined the flexible electronics team and developed self-assembly processes for thinned ICs as well as heterogeneous integration techniques for printed and large area electronics. He is currently working as a project manager on European and National research projects with a focus on thin chip integration in flexible foil substrates.