SMART Design

Welcome

B. Smith
Executive Director at Electronic System Design Alliance
Electronic System Design (ESD) Alliance a SEMI Strategic Association Partner, Milpitas, United States

Abstract

Biography

Robert (Bob) Smith is Executive Director of the Electronic System Design (ESD) Alliance a SEMI Strategic Association Partner. The ESD Alliance is an international trade association of companies providing goods and services throughout the semiconductor design ecosystem. Bob began his career as an analog design engineer at Hewlett-Packard working on disk drive technology. Since then, he has spent more than 30 years in various roles in executive management, marketing, and business development primarily working with startup and early stage companies in Electronic Design Automation (EDA) and semiconductor IP. These companies include IKOS Systems, Synopsys, LogicVision, Magma Design Automation and Uniquify. He was a member of the IPO teams that took Synopsys public in 1992 and Magma public in 2001. Bob received his BSEE from U.C. Davis and his MSEE from Stanford University.

Next Generation SoC Design: From Atoms to Systems

B. Taheri
CEO/CTO
Silvaco Inc, Santa Clara, United States

Abstract
Integrating the most advanced nanometer technologies such as FinFETs, Quantum Dots, MicroLEDs, MRAM, and ReRAM in IP and SoC designs, requires new simulation, optimization, and automation technologies. Physical models for new materials need to be captured to enable TCAD process and device simulation that extends from the atomic-level to the circuit-level. This simulation and modeling can then be promoted to a higher level for design and technology co-optimization (DTCO) from device to IP level, followed by system and technology co-optimization at the SoC level.

Silvaco TCAD software accurately simulates the manufacturing process, device characteristics and resulting circuity. In addition, Silvaco EDA tools take the results of TCAD analysis to simulate circuit behavior across a range of effects including process, voltage and temperature variability, and enable a cohesive DTCO flow for Smart Design. In this talk, I will describe the need for a toolset that can manipulate atoms in semiconductor structures, as well how a suite of tools can be tied together in a cohesive simulation environment to take full advantage of the performance and capabilities in the latest nanometer processes.

Biography
Babak Taheri is the CEO at Silvaco Inc., a leading provider of TCAD, EDA, and design IP software. He began his career at Silvaco as chief technical officer and executive vice-president of products. Previously, he was the CEO / president of IBT working with investors, private equity firms, and startups on M&A, technology, and business diligence.
While at IBT, he served on advisory boards of MEMS World Summit, Novasentis, AGCM, ALEA labs, Lion Point Capital, and Silver Lake. Prior to IBT, he was the VP & GM of the sensor solutions division at Freescale semiconductor (now NXP).
Babak was the recipient of ”the perfect project award” in 2003 while at Cypress; Twice recipient of the “Diamond Chip Award” in 2013 /14 while at Freescale; recipient of the MEMS & Sensors executive of the year award in 2014, and in 2015 was the recipient of the Distinguished Engineering Alumni Medal from UC. Davis College of Engineering, where he is on the advisory board to the college.
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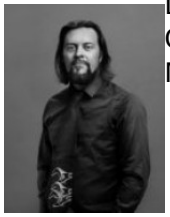
Near-Threshold Logic Benefits the Full Application Stack



L. Koskinen
CTO and Co-founder
Minima Processor, Oulu, Finland

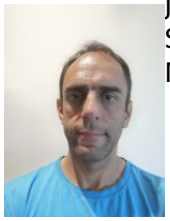
Minima

Abstract
Minima dynamic margining enables any processor or DSP core to operate at its minimum-energy point and achieve up to 15x energy savings. As energy is quadratically proportional to voltage, the energy savings are achieved with ultra-low-voltage operation. Minima enhanced logic operates down to 0.4V while still meeting user set performance requirements. Additionally, Minima margining enables ultra-wide DVFS that allows operation from ultra-low to nominal voltage.

Dynamic margining is a HW-SW solution that is grounded on netlist-level logic enhancements. Minima IP enables the processor to modify power usage in real time in response to performance needs, process variations, or environmental conditions. The enhancements are completely compliant with mainstream CAD. The Minima toolset includes application-level profiling that allows tuning for UW-DVFS in the whole vertical application.

Biography
Lauri brings broad design expertise to Minima ranging from ultra-low-power aspects of deep submicron transistors, up to the high-level realization of various systems (microcontrollers, deep learning, wireless biomedical sensors, audio and video coders). Lauri has 1 granted and 6 pending patents for the technology behind the Minima solution, and he is an author or co-author of 50+ papers in international conferences and journals. In his academic career, Lauri is an Adjunct Professor at the University of Turku, and he received a prestigious Fulbright Finland ASLA grant in the IC/Electronics field for a one year post-doctoral visit to the UC Berkeley Wireless Research Center.

Deep Learning for Electronics Manufacturing



J. Cabello
Senior Computer Vision Engineer
Mycronic AB, Täby, Sweden

Abstract
Deep learning is entering in the electronics manufacturing to further increase the reliability of its processes. In some cases, like in the operation of Pick & Place machines failures can only be afforded in a few cases per million operations.

The combination of this high reliability requirement, autonomous decision making without intervention of human operators and a huge ever-growing flora of components to inspect present challenges to deploy deep learning in production systems. Particularly deep learning limited explain ability when the algorithms fail and the need to reduce also human involvement in supervised training schemas make it harder for this technology to arrive to the factory line.

Biography
Javier Cabello holds a degree in Computer Science and Engineering from Heriot-Watt University at Edinburgh. He is Lead Engineer for the computer vision group at Mycronic AB in Stockholm. He has being involved in developing several generations of machines within Pick & Place and Jetting technologies for the electronics manufacturing industry.

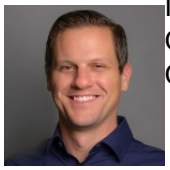
Cloud-Accelerated Innovation for Semiconductor Design and Verification

D. Pellerin
Head of WW Business Development,
Hitech/Semiconductor
Amazon Web Services, Seattle, United States

Abstract
An explosion in the number and variety of intelligent edge devices, combined with cloud computing, are driving a need for more rapid innovation in semiconductor products. This talk presents examples and best-practices for cloud-accelerated semiconductor design and verification, including use-cases and examples inside and outside of Amazon. The talk will include an overview of how the development of next-generation products is enhanced through the use of cloud for scalable, high-throughput EDA flows. The talk will cover performance optimizations for computing, storage, and EDA workload orchestration, as well as covering how cloud enables secure collaboration in the semiconductor and electronics supply chain.

Biography
David Pellerin serves as Head of Worldwide Business Development for Hitech/Semiconductor at Amazon Web Services. Prior to joining AWS, Mr. Pellerin had a career in electronic design automation and hardware-accelerated reconfigurable computing. He has experience with digital logic simulation and optimization, high-level synthesis, grid and cluster computing, and embedded systems for image, video, and network processing. He has published five Prentice Hall technical books on EDA-related topics.

Cloud Engineering Simulation: A Game Changer for Engineers



I. Campbell
CEO
OnScale, Redwood City, CA, United States

Abstract
Engineers are only as good as our tools. Engineers designed the first airplanes with slide rules and drafting tables. Engineers landed men on the moon with pocket calculators and early mainframe computers. Engineers in the modern era use desktop engineering simulation software to develop semiconductors, sensors, 5G RF base stations, biomedical devices – our modern world.

Now, we are entering a new era – the era of Cloud Engineering Simulation. Cloud Engineering Simulation combines highly scalable multiphysics solvers with cloud supercomputers to break cost and performance barriers for engineers pushing R&D boundaries.

With Cloud Engineering Simulation, engineers can now create Digital Prototypes – digital representations of physical devices that provide as much or even more engineering data than a set of engineering samples on a lab bench.

Learn how industry leaders are leveraging Cloud Engineering Simulation to massively reduce cost, risk, and time-to-market for new technology introductions in spaces like next-gen semiconductors, MEMS sensors, RF front-ends, biomedical devices, and driverless car systems.

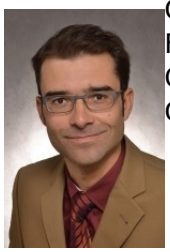
Biography
Ian Campbell is a twice venture-backed Silicon Valley CEO and expert in MEMS sensors, semiconductor technology, and engineering software.

Most recently, Ian co-founded OnScale, a Cloud Engineering Simulation startup backed by Intel Capital and Google's Gradient Ventures. OnScale is revolutionizing engineering by combining world-class multiphysics solvers with Cloud supercomputers, machine learning, and artificial intelligence.

Prior to co-founding OnScale, Campbell served as founder and CEO of NextInput, where he led the startup through multiple rounds of funding – totaling $12 million and an additional $4 million in research contracts with government and industry partners – and built a world-class team of engineers and scientists who developed 3D Touch and ForceTouch technologies for smartphones, wearables, industrial, and automotive interface applications. He also secured the first major smartphone OEM design wins in Asia.

Campbell earned his B.S. in mechanical engineering from Middle Tennessee State University, and his MSAE in aerospace engineering and MBA from Georgia Institute of Technology.

Addressing the "New-Space" Paradigm Shift in Development and Production of High Reliability, Space Grade Semiconductor Components



C. Sayer
Field Applications Engineer
Cobham Advanced Electronics Solutions, Cobham Gaisler, Gothenburg, Sweden

Abstract
Semiconductor devices used for space missions have for decades dominated as specialized, radiation hardened components, built to the highest standards of reliability. Developed and manufactured in small quantities, the cost of traditional HighRel devices can exceed their commercial counterparts by several orders of magnitude.

In recent years however, the number of smaller satellites, placed in lower orbits and designed for shorter operating lifetime, has increased. Especially the the concept of larger satellite constellations, with hundreds to thousands of spacecraft communicating with each other, covering the entire surface of the earth with a dense mesh of instruments or communication equipment for particular applications, have challenged the industry by their unconventional requirements. Cost of individual equipment becomes a primary factor for a mission involving a large number of spacecraft. New ways of designing for space need to be considered, questioning the traditional risk assessment.

From the perspective of a traditional HighRel component supplier, what is our strategy to follow this shift from the "best possible" to the "good enough"? Looking at what impact a harsh environment can have on semiconductor devices, and what makes a space grade component flight-worthy, the LeanREL™ concept and line of products is introduced. Aiming to combine traditional space pedigree with a manufacturing flow substantially reducing cost, the technology is an enabler for lower orbit, shorter lifetime, high volume space missions.

Biography
Christian Sayer is Field Applications Engineer for Cobham Gaisler and Cobham Advanced Electronic Solutions. His focus is on processor, memory, interface, mixed signal and power components. Prior to Cobham, he worked as design and applications engineer for companies in the fabless semiconductor and embedded domain. Christian studied electrical engineering in Berlin, Montpellier and Paris. He holds a MSc. (Dipl.-Ing.) in Electrical Engineering of the Technical University of Berlin.

J. Hogan
Executive Managing Partner
Vista Ventures, LLC, San Francisco Bay Area, United States

Biography
James H. Hogan, executive managing partner of Vista Ventures, LLC, is an experienced senior executive who has worked in the semiconductor design and manufacturing industry for more than 40 years. He serves as a member of the board of directors for electronic system design, intellectual property, semiconductor equipment, material science and IT companies.

Previously, Hogan was general partner at Telos Venture Partners and served as chief technology officer and senior vice president of business development at Cadence, and chief operating officer of Smart Machines, a semiconductor equipment automation company. Earlier, he worked for National Semiconductor and Philips where he established device physics laboratories globally and manufacturing yield improvement programs.

Hogan founded Heart of Technology (HOT), a philanthropic organization based in San Jose, Calif., to unite the semiconductor industry to aid charities in their fundraising efforts for the betterment of local communities and enrichment of lives.

He holds Bachelor of Arts and Math, Bachelor of Science and Computer Science and MBA degrees from San Jose State University.

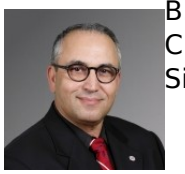
Pulini Gabriele

G. Pulini
Sr. Business Development Manager
Mentor Graphics, Wilsonville, United States

Biography

Gabriele Pulini joined Mentor in 1991 and has extensive engineering and marketing experience on the new technologies that changed over time the way new products are designed and brought to market. As part of the Emulation business unit within Mentor, a Siemens business, he is responsible for the new business opportunities, with today's focus on self-driving and artificial intelligence applications.

Taheri Babak



B. Taheri
CEO/CTO of Silvaco
Silvaco Inc, Santa Clara, United States

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Babak Taheri is the CEO at Silvaco Inc., a leading provider of TCAD, EDA, and design IP software. He began his career at Silvaco as chief technical officer and executive vice-president of products. Previously, he was the CEO / president of IBT working with investors, private equity firms, and startups on M&A, technology, and business diligence.

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Hamid Adnan

A. Hamid
Chief Executive Officer, Founder
Breker Verification Systems, San Jose, United States

Biography

Adnan is the founder CEO of Breker and the inventor of its core technology. Under his leadership, Breker has come to be a market leader in functional verification technologies. The Breker expertise in the automation of self-verifying testcases is setting the bar for the completeness of verification for system-on-chip (SoC) designs.

He has over 20 years of experience in functional verification automation. Prior to Breker, he managed AMD's System Logic Division, and also led their verification team to create the first test case generator providing 100% coverage for an x86-class microprocessor. In addition, Adnan spent several years at Cadence Design Systems and served as the subject matter expert in system-level verification, developing solutions for Texas Instruments, Siemens/Infineon, Motorola/Freescale, and General Motors.

Adnan holds twelve patents in test case generation and synthesis. He received BS degrees in Electrical Engineering and Computer Science from Princeton University, and an MBA from the University of Texas at Austin.

Cunningham Paul

P. Cunningham
Corporate Vice president and General Manager of the System Verification Group
Cadence Design Systems, Inc., San Hose, United States

Biography

Paul Cunningham is corporate vice president and general manager of the system verification group at Cadence Design Systems. His product responsibilities include logic simulation, emulation, prototyping, formal, VIP, and debug. Prior to this, he was responsible for Cadence's frontend digital design tools including logic synthesis and design-for-test. Paul joined Cadence in 2011 through the acquisition of Azuro, a startup developing concurrent physical optimization and useful skew clock tree synthesis technologies, where he was a co-founder and CEO. Paul holds a Master's Degree and a Ph.D. in Computer Science from the University of Cambridge, UK.

Brinkmann Raik

R. Brinkmann
President and CEO
OneSpin Solutions, Munich, Germany

Biography

Dr. Raik Brinkmann is the president and CEO of OneSpin Solutions. His innovative vision for advanced formal technology lead to co-founding OneSpin Solutions in 2005. Since his tenure as president and CEO in 2012, Brinkmann has led the company to significant growth including an unprecedented 52% CAGR over the past four years. Dr. Brinkmann holds a Diplom Informatiker (equivalent to a master's degree in computer science) from the Clausthal Technical University, Germany and a Dr.-Ing. (equivalent to a Ph.D. degree) from the Department of Electrical Engineering at the University of Kaiserslautern, Germany. He is also currently on the board of directors for the Electronic System Design Alliance, an organization responsible for the advancement of electronic design automation within the semiconductor industry.