Challenges of Moores Law

Challenges for the end of Moore Law

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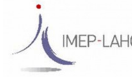

Abstract
The historical trend in micro/nano-electronics over the last 50 years has been to increase both speed and density by scaling down the size of electronic devices, together with reduced energy dissipation per binary transition, and to develop many novel functionalities for future electronic systems. We are facing today dramatic challenges for More Moore and More than Moore applications: substantial increase of energy consumption and heating which can jeopardize future IC integration and performance, reduced performance due to limitation in traditional high conductivity metal/low k dielectric interconnects, limit of optical lithography, heterogeneous integration of new functionalities for future nanosystems, etc. Therefore many breakthroughs, disruptive technologies, novel materials, and innovative devices are needed in the next two decades.
With respect to the substantial reduction of the static and dynamic power of future high performance/ultra low power terascale integration and autonomous nanosystems, new materials, ultimate processing technologies and novel CMOS or Beyond-CMOS device architectures (FDSOI, FinFET, Nanowire FET, Nanosheet devices, Carbon Nanotube FET, Tunnel FET or Ferroelectric Gate FET with Negative Capacitance, Non-charge-based Memories –e.g. PCRAM, ReRAM, MRAM, FeRAM- 3D integration, etc.) are mandatory for different applications, as well as new circuit design techniques, architectures and embedded software.
This presentation will focus on the main trends, challenges, limits and possible solutions for future high performance and ultralow power nanoscale devices for the end of Moore’s Law.

Biography
BALESTRA Francis, CNRS Research Director at IMEP-LAHC, has been Director of several Laboratories, IMEP and LPCS, for a total of 10 years and Director of the European Sinano Institute during 6 years. Within FP6, FP7 and H2020, he coordinated several European Projects (SINANO, NANOSIL, NANOFUNCTION, NEREID) that have represented unprecedented collaborations in Europe in the field of Nanoelectronics. He is member of the AENEAS Scientific Council, of the European Academy of Sciences, of the Advisory Committee of several International Journals and of European Working Groups for Roadmapping activities. He founded (ULIS, WOLTE, INC) or organized many international Conferences, and has co-authored a large number of books and publications. He is currently Vice President of Grenoble INP, in charge of European activities.

EU consortia joining forces to tackle challenges of advanced technology nodes

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Abstract
Moore's Law has powered more than 50 years of advances in the microelectronics industry. In recent years this law is under pressure, because the continued geometrical miniaturization led to device performance degradation, device variability issues.

Since 2015, with financial support from the EU, material compagnies, equipment companies, design houses, universities and research institutes have joined forces to tackle the challenges related to CMOS scaling. The first project, SeNaTe, targeted the 7nm node, subsequent projects respectively tackled the 5nm node (TAKE5 and TAKEMI5) and the 3nm node (TAPES3 and Pin3S) challenges. Recently, May 2019, the IT2 project targeting IC Technology for 2nm node was submitted for funding by EU.

An overview will be presented of the technical solutions which have been explored to provide solutions for 7nm, 5nm, 3nm technology node to keep pace with Moore's scaling law.
The following topics will be addressed: multi-patternng solutions for area scaling, self-aligned patterning and area selective deposition solutions for Edge Placement Error (EPE) mitigation, material innovation, hybrid damascene and air gap integration for advanced BEOL, innovative device architectures transitioning from planar to FinFET, Gate All Around nanowire/nanosheet (GAA NW/NS) device, for improved device performance. Other topic which will be addressed are track height scaling and device booster integration through Design Technology Co-Optimization. Device boosters which will be covered comprise: fully-Self Aligned Contact, Self-Aligned Gate Contact, Self-Aligned Block, Buried Power Rail (BPR), Super Via (SV).

Final part of the presentation will cover System Technology Co-Optimization (STCO). STCO, the next level of design and technology optimization, this time approached from a system/application perspective, for manufacturing of future node devices and applications meeting 2nn node PPAC specifications.

Biography
Werner Boullart received a PhD in Chemistry in 1991 at the Catholic University of Leuven. Till 1995 he worked at the university as a researcher in the domain of atmospheric chemistry.
In 1995, he joined imec as a process engineer responsible for the development of plasma etch processes. From 2001 till 2012, he was manager of the Plasma Etch group. Since 2012 he worked as staff engineer of the Unit Process and Module department responsible for strengthening the collaboration between the different unit process step groups. In this function he was also managing Joint Development Projects with key semiconductor equipment suppliers.
Since 2015, he took up the role of work package project manager for imec in the EU funded projects. In this role he is also responsible for defining the the imec contribution for future projects related to advanced CMOS scaling.