Strategic Materials Conference

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Fujifilm Electronic Materials, FFEM, Europe,
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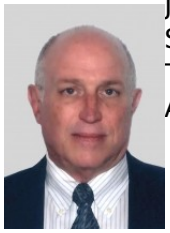
Biography
Stefan Vanclooster is Global Business Director Polyimides at FujiFilm Electronic Materials (FFEM), located in Belgium. Stefan manages the global business unit of polyimide materials for the semiconductor industry within FFEM. Stefan received a Master's degree in chemical engineering at the University of Ghent and a Master's degree in Polymer and Composite Materials at the University of Leuven. He also obtained a postgraduate in business economics and finance at the University of Leuven

Innovations in Fan Out for Heterogeneous Integration



J. Hunt
Senior Director, Engineering Marketing &
Technical Promotion
ASE Group, Tempe, United States

Abstract
For today's electronic applications, including all levels of Mobile and High Performance, the increased device complexity and performance requirements have driven the need for heterogeneous interconnectivity. At the same time, Fan Out technology has evolved from a simple, single die packaging solution into a variety of high-density solutions enabling multi-die 2D and 3D connectivity.
During this presentation, we will review how the integration of a wide variety of packaging technologies, including wafer level processing, substrate evolution and Flip Chip packaging structures have come together to enable complex Fan Out packages. We will further explore the different levels of integration and sophistication which use Fan Out as a basic manufacturing technology, describing the evolving functionality achieved by combining low cost materials and innovative process flows. By using these combinations of tools and processes, the resulting packages have been continually evolving in complexity and functionality, limited only by our imagination and creativity.

Biography
John is Senior Director Engineering, Marketing & Technical Promotion at ASE Group, and provides technical support for the Introduction, Engineering, Marketing, and Business Development activities for Advanced Wafer Level and Fan Out Packaging Technologies at ASE.

John has more than 45 years of experience in various areas of manufacturing, assembly and testing of electronic components and systems, with emphasis on the development of new technologies and processes. He has a B.S. from Rutgers and an M.S. from the University of Central Florida.

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Polymeric materials for Advanced packaging

A. Pizzagalli
Technology & Market Analyst,Equipment & Materials - Semiconductor Manufacturing
Yole Développement, Villeurbanne, France

Abstract
Driven by movements towards further miniaturization and higher functionalities, megatrend applications like artificial intelligence (AI), 5G, and augmented reality (AR)/virtual reality (VR) are creating huge business opportunities and contributing to the growth of AP applications. Indeed, these megatrend applications are fueling the next generation of AP platforms (high-density FOWLP, 3D stacked TSV memory, WLCSP, and flip-chip), which have reached a new level of complexity and now demand higher integration-level requirements. These lofty standards will strongly influence the increasing demand for advanced materials with new technical specifications, in order to achieve better performance.
Polymeric materials are primarily used to protect printed wiring boards (PWB) from moisture, handling, and environmental influences. However, over the last few years polymeric materials have attracted significant interest in the microelectronics field, and have already found integration in major process steps: RDL, bump/UBM, through-silicon vias (TSV), and assembly levels, as well as at the bonding interface.

This presentation will provide a comprehensive analysis of the different existing polymeric materials used for Advanced Packaging as well as their status. In addition, key technical trends, requirements and challenges regarding the polymeric materials applied at each advanced packaging process step will be addressed. A technology roadmap showing the future steps for these polymeric materials solutions as well as market forecast, competitive landscape of the major material suppliers will be covered.

Biography
Amandine Pizzagalli is a Technology & Market Analyst, Equipment & Materials - Semiconductor Manufacturing, at Yole Développement (Yole). Amandine is part of the development of the Semiconductor & Software division of Yole with the production of reports and custom consulting projects. She is in charge of comprehensive analyses focused on semiconductor equipment, materials and manufacturing processes. Previously, Amandine worked as Process engineer on CVD and ALD processes for semiconductor applications at Air Liquide. Amandine was based in Japan during one year to manage these projects. Amandine graduated from the engineering school, CPE Lyon (France), with a technical expertise in Semiconductor & Nano-Electronics and holds an electronics engineering degree followed by a master's in semiconductor manufacturing technology from KTH Royal institute of technology (Sweden).
She has spoken in numerous international conferences and has authored or co-authored more than 10 papers.

Innovative Interconnect and Encapsulation Developments for Wafer Level Packaging

R. de Wit
EIMEA SU Head Semiconductors
Henkel Electronic Materials, Semiconductor Assembly Materials, Westerlo, Belgium

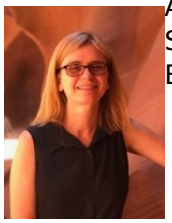
Abstract
Smart Electronics' trends like Big Data, Artificial Intelligence, Autonomous Driving and 5G continue to drive advanced semiconductor innovation towards higher functionality with smaller form factors and reduced power consumption. To meet these future demands, semiconductor package designs continue to evolve towards WAFER scale assembly using 3D Stacking and System-in-Package (SiP) type of architectures. Through Silicon Via (TSV) is enabling 3D die stacking for High Bandwidth Memory (HBM) allowing for finer pitch. Wafer Level Packaging (WLP) for both Fan-In and Fan-Out are also gaining momentum rapidly and same for Panel Level Packaging (PLP) showing significant progress. With this move towards SiP, increasing data demands, faster processing speeds and the emergence of 5G, traditional wafer fabrication companies are getting more in the driver's seat of Semiconductor Packaging.

New finer pitch interconnect and low warpage encapsulation developments are essential for such high-density and challenging 2.5/3D device manufacturing processes, stress management for larger devices and increasing long-term reliability requirements. Next to this, increasing heat generation and dissipation, Fan-In and Fan-Out process compatibility (adhesion, die shift) and further need for miniaturization (Keep-out-Zone) are key challenges for Semiconductor Packaging material suppliers.
< div >This presentation will give a technical overview of the advanced wafer level packaging material developments to enable next gen 2.5D and 3D chip designs :
< div >- "Wafer Applied Underfill Films" for 3D Stacking of thin TSV wafers with increasing thermal performance and faster processing
- Low shrinkage and ultra-low warpage wafer encapsulants and coatings for Fan-In and Fan-Out applications

These developments are aimed to meet the market's sustainability, miniaturization and high reliability requirements with providing reliable, scalable and environmental-friendly adhesive and encapsulation solutions.

Biography
Ruud de Wit is responsible for managing Henkel's Semiconductor Packaging Materials business development within EIMEA region. Ruud has a BSc degree in Mechanical Engineering followed by several polymer, sales and marketing courses. Ruud is working for Henkel since 1990 in multiple positions including technical customer service, quality assurance and engineering, and global semiconductor account and product management.

Temporary Bonding Materials: The Future Beyond Temporary Thin Wafer Handling



A. Guerrero
Senior Applications Engineer
Brewer Science, Inc, Leuven, Belgium

Abstract
Processes using temporary bonding materials (TBMs) are now frequently integrated into advanced packaging processes that require thin wafer handling. Initially, materials and processes were developed for silicon to enable through-silicon vias (TSVs) as interconnect for 3D stacking. However, the need to handle highly warped and stressed substrates such as reconstructed epoxy mold compound (EMC) wafers or thin alternative metal substrates has further broadened the utility of TBMs.

This presentation will highlight how materials developed for temporary thin wafer handling are evolving and being adapted to diverse applications. The first example will review processes in chip-first fan-out wafer-level packaging (FO-WLP) where TBMs are used for temporary die placement. In general, RDL processing and the density of I/O connections after mold is limited due to issues with die shift during mold processing. However, by selecting a TBM with the right properties and coupling it with the right EMC, one can achieve <2 µm shift with bow <200 µm. This fine control of die placement in a reconstructed wafer can further drive RDL interconnect to tighter pitches. From a TBM perspective, the material serves both as a substrate for collective die placement as well as to facilitate mold wafer thinning.

A second example, in yet a different area of electronics manufacturing, is the transfer of ultrathin 2D layers from a growth substrate to a device substrate using temporary bond-debond technologies. To maintain the pace for future node devices, novel 2D materials that support CMOS circuits will be a key element enabling transistor scaling. The challenge is to grow and transfer these 2D materials in a manner that maintains its key electrical properties at 300 mm scale. In collaboration with imec, an example of transferring a 7-Å-thick WS2 2D layer from a 300 mm wafer will be discussed.

Biography
Alice Guerrero is a senior applications engineer with Brewer Science, Inc. She is currently a resident scientist for Brewer Science at imec in Leuven, Belgium in partnership with the 3D System Integration Program.

She received her undergraduate degree in chemistry from Union College, in Lincoln, NE and completed her PhD in Analytical Chemistry at the University of Illinois in Champaign-Urbana.

Alice has worked for Brewer Science for 21 years in both the Semiconductor Materials and Advanced Packaging business divisions in technical and project management roles. Her current focus is developing processes for emerging temporary bond and debond applications.

Ultra-Low Stress Silicone Die-Attach Film For Stress Sensitive, SiP and Stacked Dies Assembly

T. Seldrum
TS&D Scientist
DOW Silicones Belgium, Seneffe, Belgium

Abstract
Silicones are inorganic based materials with remarkable properties such as broad temperature range stability, low modulus and possibility to be loaded with multiple fillers to tune the thermal, optical and mechanical properties.

The microelectronics technology trends towards smaller form factors, increased integration of multiple devices within the same package (SiP) or stacking of dies architecture lead DOW to develop a unique die-attach film technology to be used as laminated film at wafer-level or large component level. The die-attach film consists in a pre-cured film laminated between two liners and designed to be used in mass production environment. The technology developed can be supplied with a thickness between 25µm and 300µm depending on the device requirements. Independent of this thickness, the film has a stable and low storage modulus below 1MPa over a temperature range from -40°C to 220°C. The coefficient of thermal expansion (CTE) is also stable across the same temperature range, at 290ppm/K. This combination of extremely low stress and reasonable CTE ensures that the total stress during thermo-mechanical fatigue of the device will remain remarkably low compared to organic materials such as epoxies or acrylics that have a modulus significantly higher (~1000 times higher than silicones). In addition, using a pre-cured film will ensure that the bond line thickness (BLT) is precisely controlled and that no adhesive fillet will rise along sidewalls of the chip during the assembly process, making it possible to bond thinned dies without contamination risk.

This unique solution completes an already existing broad portfolio of liquid-based silicone solutions used as adhesives for die-attach, lid-seal and grounding applications, together with thermally conductive silicone materials used as thermal interface material between the chip and package to improve the heat spreading.

Biography
Dr. Thomas Seldrum holds a PhD in Solid State Physics and is working as a Technical Development Scientist within the DOW Chemical Company. In his assignment, Dr. Seldrum is responsible for the application development of silicone-based solutions used in Automotive and Microelectronics applications. He started his career within DOW with the development of wafer-level silicone solutions for wafer passivation and manufacturing of transparent silicone membrane for optical applications. He is mostly today focusing on the application development of silicone die-attach film technologies, electrically conductive adhesives and thermally conductive materials used in the assembly of sensors and actuators.

D. Guerrero
Senior Technologist
Brewer Science, Inc., Semiconductor Business Unit, Rolla, United States

Biography

Douglas Guerrero received a PhD in Organic Chemistry from the University of Oklahoma and completed Post-doctoral work at the University of Texas-Dallas in the field of conducting polymers. He joined Brewer Science in 1995 and has served in a number of positions within the R&D organization. He is currently a Senior Technologist in the Semiconductor Materials Business Unit. Dr. Guerrero is a Senior Member of SPIE and serves in Semicon EU Strategic Material Conference, SPIE Advances in Patterning Materials and Processes and the International Symposium on DSA committees. He has been on assignment at imec in Leuven, Belgium since 2008 where he is developing processes for future nodes.

SiGeSn – A new (old) building block for nano- and optoelectronic devices

J. Schulze
Full Professor and Head of Institute
University of Stuttgart, Institute of Semiconductor Engineering (IHT), Department of Electrical Engineering & Information Technology, Stuttgart, Germany

Abstract
Recent years have seen a lot of experimental effort directed towards integrating photonics with electronics. The Group-IV elements Si and Ge are the dominating materials of semiconductor electronics. However, their application to optoelectronics is limited due to their indirect bandgap and the concomitant low efficiency in optoelectronic applications. Recent experiments have therefore focused on the investigation of GeSn and SiGeSn alloys that could potentially be used as direct bandgap Group-IV-materials for an efficient on-chip integration of photonics and electronics. The relaxed alloy Ge(1-y)Sn(y) has been predicted to become a direct bandgap material for y > 0.073, while pseudomorphic Ge(1-y)Sn(y) is predicted to have a direct bandgap for y > 0.19. A number of experimental studies have been performed to fabricate and characterize Ge(1-y)Sn(y) bulk and quantum well photodetector devices. Because of the large lattice mismatch between Ge and Sn (14 %), the growth of Ge(1-y)Sn(y) alloys with a large percentage of Sn is difficult to achieve on Si and Ge substrates. The ternary alloy SiGeSn allows one to decouple bandgap and lattice constant [8] and is, therefore, a particularly interesting candidate for optoelectronic applications. Several groups have reported the successful fabrication of SiGeSn alloys by Chemical Vapor Deposition and Molecular Beam Epitaxy; bulk SiGeSn-photodiodes have been fabricated and analyzed. Furthermore, a number of proposals concerning photonic devices such as light-emitting diodes or modulators with Multi-Quantum-Well structures in their active regions have been made. For those devices, additional advantages such as a lower intensity of Auger processes have been predicted. The talk presents results on the growth and characterization of SiGeSn alloys integrated on Si substrates and their use in optoelectronic devices.

Biography
Jörg Schulze studied experimental physics at the TU of Braunschweig, Germany. In 2000 he received his PhD in Electrical Engineering from the Electrical Engineering & Information Technology Faculty of the University of the German Federal Armed Forces Munich with a dissertation on Boron surface phases and Esaki-like tunneling transistors. From the same faculty he received in 2004 his post-doctoral degree (Habilitation) in Semiconductor Physics and Microelectronics. He was active as Senior Consultant for Technical Risk Management and as Head of Competence Field “Robust Design Optimization” in Siemens Corporate Technology (2005-2008). Since 2008 he has been working at the University of Stuttgart, Germany, as Professor of Electrical Engineering and Head of the Institute of Semiconductor Engineering. He authored more than 200 peer reviewed articles, two book chapters and two books.

New Prospects for Temperature and Current Sensing for Wide Bandgap Semiconductors

J. Winkler
Robert Bosch GmbH, Reutlingen, Germany

Abstract
In typical high voltage applications, such as traction inverters, silicon IGBTs or SiC MOSFETs are implemented. Within such applications the power semiconductors are accompanied by current and temperature sensing devices to drive a certain load, e.g. an electric motor. Commonly, these sensing elements must be added to the system but there are various approaches to utilize appropriate current or temperature sensitive parameters of the semiconductor device.
To promote future power electronic applications it is essential to tap the full potential of the power semiconductor device, especially with regard to current and temperature sensing. Power electronic applications could benefit from a commonly unappreciated and unused advantage: Light emission. It occurs in every forward biased p-n junction and exhibits an approximately proportional intensity-current characteristic. This behavior is known from operation of usual light emitting diodes and it is also applicable to p-n junctions in power semiconductor devices.
The basic suitability of electroluminescence from power semiconductor devices for the purpose of current sensing or deadtime control is demonstrated in the authors' previous work [1,2]. The current work of the authors focus on the transient measurement of the light emission from SiC Power MOSFETs for the purpose of current sensing [3] and for the purpose of junction temperature sensing.

[1] Winkler et al., “Utilization of Parasitic Luminescence from Power Semiconductor Devices for Current Sensing”, PCIM Europe 2018, 2018
[2] Winkler et al., “Electroluminescence in Power Electronic Applications: Utilization of p-n Junctions in Power Semiconductors as unintentional Light Emitting Diodes for Current and Temperature Sensing”, EVS31 & EVTeC 2018, 2018
[3] Winkler et al., “Study on Transient Light Emission of SiC Power MOSFETs Regarding the Sensing of Source-Drain Currents in Hard-Switched Power Electronic Applications”. PCIM Europe 2019, 2019

Biography
Jonathan Winkler received the Bachelor of Engineering degree in mechatronics & electrical engineering from University of Applied Science Esslingen in 2014. He continued his studies at the Robert Bosch Center for Power Electronics and received the Master of Science degree in power- & microelectronics from Reutlingen University in 2016. Afterwards, he joined a PhD program of Robert Bosch GmbH and the University of Stuttgart. The focus of his research is on the electroluminescence of power semiconductor devices and its utilization.

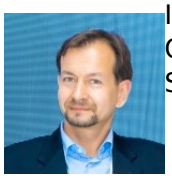
Germanium as an emerging strategic material for next-generation devices and applications

R. R. Sumathi
Head Semiconductors
Leibniz-Institute for Crystal Growth (IKZ),
Semiconductors, Berlin, Germany

Abstract
CMOS scaling is continuously being pushed to go beyond sub-10nm level. There is a quest to overcome the ultimate “bulk-Silicon(Si)” limits and the size-scaling by adding new materials and structures for devices. Among alternate new materials, Germanium (Ge) looks to be promising because of favourable properties like low effective electron mass, higher carrier mobilities for high-mobility channel material and p-MOSFET with simple material design and compatible processing in a Si-fab. Ge as substrate for solar cells in space and light emitting sources are well known and have already been demonstrated. From our vast experience in the growth of volume single crystalline boules of Si, Gallium Arsenide (GaAs), Indium Phosphide (InP), we have successfully grown Ge single crystals of size 2-inch diameter. Both high purity (net carrier concentration ≈ 10^{11} cm^{-3}) and high p-, n-doping (mid 10^{18} cm^{-3}) wafers with a EPD of 5000 cm^{-2} for device applications in CMOS, detectors, plasmonics/sensors could be prepared out of the grown crystals. Additionally, the development of 3-inch dia crystalline boules are being completed and the wafers will be soon available. In this talk, the Ge growth technology and its related processes, developed in-house at IKZ, will be presented, after discussing the growth challenges of this new material. The remaining associated problems with Ge and envisaged solutions will be highlighted before concluding this presentation.

Biography
Dr. R. Radhakrishnan Sumathi is a Vice-head of volume crystals department at Leibniz-Institute for Crystal Growth (IKZ), Berlin. She is leading and responsible for the semiconductor section, which focuses its niche research and development in elemental and compound semiconductor materials (Si, Ge, III-Vs, II-VIs). IKZ is a well-known institute within Europe for developing crystalline materials and also one of the world leading institute with a wealth of expertise covering narrow and wide bandgap materials, which includes nitrides (AlN), carbides (SiC), oxides (Ga_2O_3), etc.
Dr. Sumathi holds a Ph.D degree (Anna University, Chennai/Madras, India) and also obtained a “*habilitation*” title from Ludwig-Maximilians-University (LMU, Munich, Germany), where she is also a faculty at Materials Science and Crystallography institute. She has about 25 years of expertise and good experience in semiconductor materials and devices. She is very active in many professional societies of crystal growth / materials sciences and has received many awards, the recent one being, Young Achiever Award by Indian Science and Technology Association in 2018. She has over 75 papers in international journals and/or conferences and has given invited talks in 25 meetings.

Quality control in sapphire production: From automated defect detection to big data approach.



I. Orlov
CEO
Scientific Visual, Lausanne, Switzerland

Abstract
High thermal conductivity, low reactivity, and appropriate unit cell size makes sapphire an ideal material for a wide range of electronic substrates such as LEDs and silicon on sapphire for CMOS. However, internal flaws, such as cracks, bubbles and dislocations, in sapphire substantially affect performance and reliability of such devices [1,2]. Flaws are usually identified only after costly wafering and polishing steps, because rough surface of raw crystals prevents detection of the defects. Most of manufacturers evaluate crystal defectiveness only at the wafer substrate stage, where up to 20% of processed material is rejected.

This contribution shows advanced technology to visualise defects in semiconductor crystal *prior to processing*, as well as defect statistics we have collected over 5 years of grading sapphire from key suppliers in Europe and Asia[1].

With automated systems that can accurately determine locations, density and types of sapphire defects and 'big data' approach, we will illustrate trends in sapphire defectiveness, compare growth methods and derive the best combination of process parameters to increase yield.

We will demonstrate:

- 3D variation of defect morphology, size and quality zoning in a typical crystal grown by Kyropolous and HEM[2] methods
- Correlation of defects at crystal level with specific parameters of crystallisation
- Revealing long-time trends in production quality by accumulating defect statistics over time
- Applying *big data* and artificial intelligence to trace structural defects back to crystallisation issues.

This work illustrates how *Industry 4.0* approach in quality control can benefit both sapphire producers and end device manufacturers in terms of production yield.

[1] Anonymised data
[2] Heat Exchange Method (HEM)

[1] T.Person, R.Howland. The Gleam of Well-Polished Sapphire, Solid State Technology, Jan 2013
[2] O.Bunoiu et al. Gas bubbles in shaped sapphire. Progress in Crystal Growth and Characterisation of Materials 2010; 56(3–4),123

Biography
Dr. Ivan Orlov obtained PhD in Crystallography from Federal University of Technology in Switzerland and MSc in Solid-State Physics in Moscow, Russia. Ivan co-founded Scientific Visual in 2010 to answer the challenge of synthetic crystals industry struggling with high defect yield. Prior to it he worked in a company

specialised in diamond optics. His career includes 10+ years of progressive experience in R&D with the focus on optical materials, industrial crystals and non-destructive quality control technologies.
Dr. Orlov was SEMI Task Force member for sapphire standard development in China, and collaborates with ISO committee in Switzerland to establish industry-wide sapphire quality standard.

Recent advancements in tailor-made silicon substrate manufacturing

P. Sievilä
Customer Support Engineer
Okmetic Oy, Customers and Markets, Vantaa, Finland

Abstract
There is a constant drive towards increased reliability, quality, and performance of silicon-based devices. To respond to this demand, we present the manufacturing process platform for value-added Si substrates with fully customized material properties and design, including embedded patterns and SOI layers with high layer thickness precision. These wafers, acting as a partially built component, not only enhance the profitability of user's further processing but also improve the long-term reliability due to the state-of-the art fusion bonding quality.

We demonstrate the achievements in recently started industrial scale manufacturing. The fully in-house solution, designed to fit for volume production, combines the expertise in bonded-SOI processing with patterning and DRIE etching technologies. Thanks to our own crystal growth capability, the starting silicon properties such as orientation, resistivity and dopants can be freely adjusted. As a further advantage, integrated process scheduling enables reasonable cycle times as the approach decreases handling and transportations between foundries and critical process steps.

A special attention has been paid to end user's quality requirements in tool and process selection, as well as in associated measurements, inspections and control. The defectivity of the embedded patterned surface is compared between in-house and service-contractor manufacturing, showing clear improvement with the substrate-integrated process done in-house.

The substrate tailoring has potential in various MEMS, sensor and photonics applications requiring buried cavities, poly-Si filled TSV structures, or patterned multi-layer SOI design.

Biography
Dr. Päivi Sievilä is a professional in the field of silicon and SOI wafers with extensive experience in research, industrial process engineering and development. Currently she works as Customer Support Engineer in Okmetic's global technical customer support. Her field of responsibility covers collaboration with European customers. She received her PhD from the Department of Micro- and Nanosciences, Aalto University in 2013. Her thesis focused on microfabrication technologies for silicon-based sensors.

H. Pairitsch
Infineon, Villach, Austria

Biography
Dr. Herbert Pairitsch holds a degree in electrical engineering from the Graz University of Technology, from

where he graduated in the year 1985. In 1986 he started his career at Infineon Technologies Austria AG (former Siemens Semiconductors) and held leading positions at various manufacturing and development departments. Since 2014 he serves as divisional Head of R&D Funding PMM (Power Management & Multimarket). His responsibilities include the coordination of national and international research projects in the context of energy efficient electronics (e.g.: LED-Lighting, renewable energy, e-mobility, Smart Grids) and new materials (e.g.: Silicon-Carbide, Gallium-Nitride).

Challenges for Cu-Metallization in More than Moore Applications

W. Robl
Senior Principal Metallization
Infineon Technologies AG, Regensburg, Germany

Abstract

Copper metallization is widely used in More than Moore applications for interconnects. Through silicon vias (TSV), copper pillars and redistribution layers are used for chip stacking or in system in package applications. Thick copper metallization for power devices increases the performance of smart power devices or MOSFETs. For all these applications, copper is mainly deposited by electroplating. The advantage of electroplating is that the growth mechanism of the copper film can be tailored for each application by adding the right organic additives to the electrolyte.

In this paper, we present how different additive packages influence the solderability and the mechanical properties of the deposited Cu films. Using additive package A (electrolyte A, film A) a more conformal deposition at high deposition rates is achieved compared to additive package B (electrolyte B, film B). However, films deposited with electrolyte A show increased incorporation of sulfur and chlorine compared to electrolyte B. This indicates that more additives are incorporated into films deposited with electrolyte A. This contamination lowers the interface energy between Cu and SnAg balls [1] for flip chip or Cu pillar applications and therefore more voids are induced at the Cu-SnAg interface after thermal storage compared to electrolyte B.

The mechanical properties of Cu films A and B were determined by micro tension tests of freestanding Cu films. The test equipment is heatable and was installed into a SEM to visualize the fracture mechanism [2]. Whereas Cu films A show very small grains after annealing the grains of film B are in the order of the sample geometry. Cu films A show therefore a higher yield stress compared to films B at room temperature; however the fracture mechanism changes with increasing temperature to brittle for film A as a result of segregation of sulfur and chlorine to the grain boundaries [3].

Biography

Werner Robl received his PhD in Physics from the University of Regensburg in 1994. After his degree he joined Infineon (former Siemens Semiconductors). Since then he has been working on development of new metallization schemes in Regensburg and Munich, Germany and East Fishkill, USA. Currently he is working as senior principal on new metallization schemes for semiconductors.

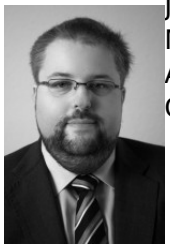
References:

[1] J.Y. Kim, J. Yu, (2008), Effects of residual impurities in electroplated Cu on the Kirkendall void formation during soldering, Appl. Phys. Lett 92, 92

[2] M. Smolka, et. al., (2012), Novel temperature dependent tensile test of freestanding copper thin film structures, Review of Scientific Instruments 83, 064702

[3] A. Wimmer, et. al., (2014), Temperature dependent transition of intragranular plastic to intergranular brittle failure in electrodeposited Cu micro-tensile samples, Materials Science and Engineering A, Volume 618, 398

Influence of Chemical Copper Surface Treatments on the Mechanical Reliability and Failure Modes in Heterogeneous Integration Packages



J. M. Knaup
Manager R&D - Group R&D
Atotech Deutschland GmbH, Group R&D, Berlin, Germany

Abstract
The reliability of Cu conductor lines is one of the major challenges in heterogeneous integration, where individually manufactured components are integrated into a single package to create highly functional devices. These conductors and their embedding in dielectric compounds are key elements to the functioning of packaging technologies such as fan out wafer level packaging (FOWLP). Shrinking the lines and spaces is central to achieving smaller form factors, reduced cost, higher performance and accommodating higher I/O counts.
In order to withstand mechanical and thermal stresses during subsequent manufacturing steps and operation, Cu lines in redistribution layers (RDL) need to be mechanically resilient. With Cu line width approaching the 1 µm scale, the toughness and ductility of the metal itself become limited by size effects. Therefore not only the properties of the individual materials need to be optimized, but the whole system must act synergistically as a composite material. The synergistic effect of a composite material depends crucially upon the transmission of forces between its constituents, i.e. the adhesion between the different materials. We show that different chemical surface treatments can improve the mechanical reliability of the conductor/dielectric composite. Detailed analyses of the materials interfaces and the failure modes of the composites provide deep insight into the underlying mechanisms and lays the foundation for knowledge based design of improved materials systems.

Biography
Jan M. Knaup studied physics at the University of Paderborn and defended his PhD in theoretical physics in 2008. After post-doctoral studies at Harvard, the EPFL and the Bremen Center for Computational Materials Science, he joined the Atotech group in 2014. Since 2017 he is R&D manager of the Group R&D team at Atotech Berlin.

Expanding the engineered substrates era

C. Maleville
EVP & CTO
SOITEC, BERNIN, France

Abstract
Users are requesting always more functionalities form their systems: information access everywhere, faster data processing, longer battery life, longer autonomy, low latency, ... To be competitive, systems must then benefit from semiconductor devices delivering more advanced performance. But performance doesn't mean only speed any more, not even speed/power only. More advanced functionalities are needed, stressing even more lack of ROI on advanced logic development, and requiring new materials and advanced integration with increased importance of More than Moore modules.
Engineered substrates are playing a critical role in enabling and accelerating integration and More Than Moore applications. By offering for example, integration platform where all components are isolated but close to each other, by decoupling active layer from passive layers requirements, by allowing integration of larger band gap or piezo electronics materials into silicon.
5G connectivity, electrical vehicles, micro LED are ramping or emerging application domains that are clearly boosted by selecting right engineered substrate and design. these examples will be described with expected impact in terms of performance, supply chain but also cost of ownership to enable HVM adoption.

Biography
Christophe Maleville has been appointed CTO in 2019.
He joined Soitec in 1993 and was a driving force behind the company's joint research activities with CEA-Leti. For several years, he led new SOI process development, oversaw SOI technology transfer from R&D to production, and managed customer certifications. He also served as vice president, SOI Products Platform at Soitec, working closely with key customers worldwide and as Executive VP of Soitec's Digital Electronics BU from 2010 to 2018, leading develeopment and deployment of FDSOI substrates as well as Imager and Photonics engineered substrates.
Maleville has authored or co-authored more than 30 papers and also holds some 30 patents. He has a PhD in microelectronics from Grenoble Institute of Technology and obtained an executive MBA from INSEAD.

I. Buchanan
Versum Materials, Utrecht, Netherlands

Biography
Iain Buchana is Strategic Marketing Manager at Versum Materials. In the past he worked for Air Product, FSAI International and Metron technology

EUV lithography insertion for future nodes in imec

P. Leray
Leti, Leuven, Belgium

Abstract
The development of EUV lithography was a long journey, but its adoption as a solution for the industry in the coming node is now clear. But still some challenges are in front of us: Resist and Infrastructure.
In this paper, after an overview of the landscape of the patterning development sustaining the Moore's law, we will show the most recent results obtained in imec with our NXE3400. After the description of the hypothesis of physical/chemical mechanisms that seem to drive the stochastic problem, we will list all the initiative currently ongoing in imec to reduce the number of stochastic counts (resist, source, track process). We will describe our Attosecond laboratory initiative to investigate the fundamentals of stochastic defects creation. We will show the latest results about EUV mask impact on defectivity and the development of CarboNanoTubes pellicle (CNT). Finally, we will summarize by discussing the remaining challenges and what could be the role of High NA lithography to support the scaling roadmap tomorrow

Biography
Philippe Leray joined imec in 2001, after being metrology group leader in imec until May 2018, he became the director of advanced patterning. This department is composed of 100 engineers and is in charge of EUV lithography, Etch and FAB metrology and inspection development for imec advanced nodes (iN7, iN5, iN3). He is also the technical owner of supplier hub with few key companies (ASML, KLA, HHT, NOVA). During the 12 first years in imec, Dr Leray has been responsible of evaluation of overlay emerging techniques (DBO and multi-layer target). He developed scatterometry models for IMEC processes (Fins, Gate and BEOL after CMP). He studied immersion defectivity issues when first immersion hoods were implemented. He contributed to more than 60 publications in SPIE.

Prior to joining imec, Dr Leray spent 4 years in plasma characterization in JRC-Ispra (Italy)
Philippe Leray obtained his PhD in 1997 at university Paris XI (France) studying the fundamentals of a plasma thruster for space applications.

The use of chemicals in the Semi conductor industry and the regulatory requirements or concerns

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JSRmicro N.V., Regulatory Affairs, Leuven, Belgium

Abstract
The Semi conductor industry has to use a lot of chemicals in his processes.
The use of chemical products in the EU is regulated by REACH and CLP .
Chemicals have to be assessed for their hazardous properties and classified according to CLP
Chemicals of very high concerned are considered for RMOA(risk management options) so that risk for man and environment is minimized

It should be good to have a look on these different

This short presentation will handle following topics
- classification according to CLP
- what are substances of very high concern
- which kind of RMOA are being considered by the European Authorities
- what is the role of the industry in those different actions
- perfluorinated chemicals : what is the concern ? what about the future ?

Biography
Name Catherine Jakus
Education PhD in polymer chemistry and in photoimaging processes in polymermatrices (K.U.Leuven)
Certificate in toxicology (UCL Louvain la neuve)
Experience
1983-1986 R&D in emulsion polymerization UVB Drogenbos
1986-1988 R&D Radcure and synthesis of liquid crystals
Synthesis of plasmask
1988-1999 Regulatory affais at UCB
Actively involved at Essenscia and CEFIC in the process of white paper for REACH regulation and CLP
Food contact
World wide regulation ; US , Australia, Korea
1999- Regulatory affairs at JSR micro nv responsible for
Hazard assessment of chemicals
Coordination of (eco) toxicological tests
Classification for GHS and CLP
Registration of chemicals for REACH
Follow up of restriction , authorisation and SVHC issues
Registration for BPR – biocidal products
Elaboration of SDS

Temperature-dependent thermal properties of nm-thin Nb2O5 using a novel thermal impedance approach

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Abstract
Nanosecond – and Picosecond laserflash equipment using aTime Domain Thermoreflectance method(TDTR) was used to investigate a 166 nm thick amorphous Niobium pentoxide layer (Nb2O5) on a silicon substrate at ambient temperatures from 25°C to 500°C.Thermal transients are obtained in sub-nanoseconds time resolution exploiting a pump laser technique. The thermal transients were analysed (i) using established analytical solutions of the fourier equation for the heat ransport in layered material stacks and (ii) by a novel numerical approach transferring thermal impedance (TI) –concepts into the nano- and pico second time regime. The analytical approach showed a thermal diffusivity and thermal conductivity from 0.43 mm²/s to 0.74 mm²/s and from 1.0 W/mK to 2.3 W/mK, respectively to temperature. The used numerical method eploited a thermal impedance appoach for the generation of structure functions to map the measured heat path in terms of a RthCth-network. The structure function showed a decrease of Rth with increasing temperature according to the increasing thermal conductivity of Nb2O5.
The combination of both, the PicoTR and NanoTR, enables to investigate the complete heat path of Nb2O5 films, from ps to µs time regime. The numerical analysis, the structure function, visualizes the Nb2O5 temperature-dependent heat path. The structure function of the PicoTR measurements showed the heat path of the Pt layer, in the ps time regime, and the Nb2O5 film in ns time regime. The NanoTR structure function, displayed the heat path of the Nb2O5 and its substrate. The temperature dependency of the structure functions is in accordance with the analytical solutions of the thermal conductivity and exhibits the indirect proportionality between thermal conductivity of the analytical solutions.

Biography
Stefan Defregger received his master's degree and PhD in Technical Physics from the Technical University of Graz, Austria. The PhD thesis was focused on piezosensor development in cooperation with AVL GmbH. Stefan has over 20 years' experience in the semiconductor industry. In his current position at MCL he is a project manager and senior semiconductor technology expert with focus on semiconductor process technologies and materials for 3D/TSV and sensors. Previously Stefan has held assignments with the solar cell maker BlueChip Energy as Head of Engineering as well as with NXP as a test development manager for RFID. Earlier assignments include leading a Unit Process Engineering group (CVD, PVD, plasma etching, CMP, metrology) at ams AG (2001-2005) and Siemens (EPCOS-TDK) from 1990-2001 working on process development for ceramic discretes.

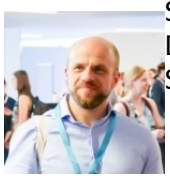
Nanopatterning for Reduced Template Hetero-Epitaxy of Low Defect Density Semiconductors

G. Feuillet
CEA-Leti, Grenoble, France

Abstract
Most optical and electronic devices rely on a specific stack of semiconducting epilayers grown onto a specific substrate. For some semiconductors such as nitrides, there are no large area substrates at affordable prices, then one has to resort to epitaxy on foreign substrates i.e. heteroepitaxy. But growing epitaxial layers on foreign substrates is at the cost of detrimental strain in the epilayers and of defect generation, the most common being dislocations that account for the different lattice parameters and thermo-elastic properties of epilayers and substrate.
We will focus on the recent development of methods for preparing the substrates in order to alleviate, if not completely, at least partially the generation of defects at the heteroepitaxial / substrate interface. Most methods rely on patterning the substrates in order to promote localized growth of the epitaxial layers. We will mainly take the example of nitride compounds and show how reducing the dimension of the pattern, hence reducing the localized growth surface, allows to critically decrease the density of dislocations threading within the epilayers up to the active region of the device to be.Two cases will be considered whether nanowires or 2 dimensional (2D) layers are considered.
Localized growth on patterned substrates allows for a strong reduction of threading dislocations but, in the case where 2D layer are envisaged, always induce defects originating from the coalescence of the slightly misaligned neighbouring crystallites. We will detail an original method based on the use of nano-patterned SOI substrates: designing SOI nano-pillars, which may deform by creep at the growth temperature, allows the GaN crystallites grown locally on top of them to align crystallographically with respect to each other. This sort of compliance results in the decrease of the grain boundaries dislocations between adjacent crystallites. We will give examples of dedicated applications based on the method.

Biography
Guy FEUILLET, 62, Research director at LETI from CEA in Grenoble, France. His past and present activities are related to compound semiconductor materials , II-VIs and III-Vs, for various applications in the field of optoelectronics and now for power electronics as well. Has an extensive expertise in semiconductor related fields such as epitaxy (including nanostructures), device physics and technologies, structural and optical characterizations.
Has lead a number of basic research or R&D teams and initiated R&D programs (ZnO French network, GaN nanostructures, CdTe based X-ray detectors for medical imaging, Solid State Lighting…) during his work at CEA. Has scientifically coordinated many of these programs, whether of fundamental or industrial character. Has also started and followed collaborative work with many partners external to CEA, at national and european levels. Used to be a member of the Selection Committee for the French National Research Agency.
Has published about a 120+papers in refereed journals, has supervised 14 thesis to date plus post-docs, has 15 patents.

More novelty and less risk with materials modelling for the semiconductor roadmap



S. Elliott
Director
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Abstract
Bringing genuine innovation into the R&D process, while managing risk, is frequently identified as a challenge for the semiconductor industry. Materials modelling is growing in importance as a reliable, flexible and cost-effective way to explore new options and reduce risk [1]. We give state-of-the-art examples of how atomic-scale modelling is impacting the semiconductor industry [2].
We show briefly how new fluorescent molecules for OLED displays can be discovered either through explicit simulation of their photophysics, or by applying machine learning to large datasets. A second example concerns semiconductor packaging, where simulations reveal the effect of UV curing on the glass transition temperature of epoxy acrylates.
In the third example, computational screening of precursors for chemical vapor deposition (CVD) and atomic layer deposition (ALD) is described in more detail. Heteroleptic precursors (such as the ZyALD™ precursor for DRAM from Air Liquide) can allow conflicting chemical requirements to be accommodated in a single molecule. However combining multiple ligands opens up a vast chemical space, much too large to explore with experiment alone. Computational screening can narrow down the search and de-risk the innovation process [3].
Here we screen metal precursors against a crucial property: thermal stability. We first enumerate over a small ligand library to produce ~100 plausible metal complexes for optimization with density functional theory (DFT). We then enumerate over the ~1000 different bonds that can be broken in these complexes and compute DFT-level bond dissociation energies as a measure of thermal stability. The least stable complexes are found to be amides with bidentate spectator ligands, which would therefore be good CVD precursors. By contrast, using cyano groups as spectator ligands is predicted to be a way to extend the ALD window to higher temperatures.

Biography
Dr Simon Elliott is Director of atomic level process simulation at scientific software company Schrödinger. From 2001-2018 he was a researcher at Tyndall National Institute, Ireland, and led the Materials Modelling for Devices group. He studied chemistry in Trinity College Dublin (B. A. Mod., 1995) and in Karlsruhe Institute of Technology (Dr. rer. nat., 1999), and carried out postdoctoral research in Trinity College (1999-2001). He has over 80 publications and is regularly invited to speak at international conferences on how modelling can address problems in materials science. He is also active in communicating science to wider audiences on TV, radio, stage and online and is a trainer in the Connect2Communicate Academy. He is a Fellow of the Royal Society of Chemistry and has qualified as a Project Management Professional. He was co-chair of the 16th International Conference on Atomic Layer Deposition (2016) and chair of a 175-member European network on the same topic (2014-2018).