Semiconductor Technology Conference (STC)

M. Pfeffer
Group Manager
Fraunhofer IISB, Erlangen, Germany

Biography
Dr. Markus Pfeffer- Group Manager Fraunhofer IISB Dr. Markus Pfeffer holds a diploma in Electrical Engineering and a PhD (Dr.-Ing.) with specialization in manufacturing optimization both from the University of Erlangen- Nuremberg. Since 2002 he is with Fraunhofer IISB in the department Semiconductor Manufacturing Equipment and Methods. He leads the group Manufacturing Control and is responsible for the analysis laboratory for micro and nano technology at the IISB. He has been engaged in the fields of equipment control, advanced process control, manufacturing optimization, analytical methods, equipment assessment and especially discrete event simulation. He was/is involved in several national and international cooperative R&D projects, e. g. FLYING WAFER, IMPROVE, EEMI450, EEM450PR, SEA-NET, SEAL and SEA4KET in different functions also as coordinator. He is member of the Steering Committee of the 450mm Equipment & Materials Initiative EEMI450 and since 2012 a member of the Factory Integration Group and Yield Enhancement Group of the ITRS.

How G450C Activities are Driving Productivity in the Industry

P. Farrar
General Manager of G450C
SUNY Polytechnic Institute, Albany, United States

Abstract
The talk will focus on productivity gains that are being advanced by work being lead by G450C. Initiatives such as Notchless wafers , 1.5mm exclusion zone, advances in metrology and process capabilities will be highlighted. In addition, 450mm process data and tool performance metrics will be discussed.

Biography
As General Manager of the Global 450mm Consortium (G450C), Paul Farrar oversees the coordination, administration and management of G450C's strategic, operational and financial missions, including external collaborations with international partner companies, program staffing, and interactions with the G450C Management Council. In addition, he serves as CNSE Vice President for Manufacturing Innovation, where he is responsible for the expansion of CNSE's intellectual know-how and state-of-the-art programs to convert longterm prospective innovations into business opportunities and economic development programs across New York. In this role, he also collaborates with educational organizations throughout New York State to implement educational programs and training opportunities in nanoscale and green energy manufacturing. Farrar joined CNSE with more than 36 years of experience in the semiconductor industry. He most recently served as IBM Vice President for Albany Expansion and Strategic Initiatives, where he was responsible for joint development alliances, the growth of the Albany ecosystem, and IBM's collaborative model, as well as

management of the capital budget for the Microelectronics Division.
During Farrar's tenure at IBM, he managed 700 IBM and partner research and development engineers and scientists, and as Vice President for Semiconductor Process Development, was responsible for unit process, lithography and characterization. Additionally, he held numerous positions in manufacturing and development, led IBM's semiconductor fab in Burlington, Vermont, managed IBM's SRAM and DRAM businesses, spent seven years in process development, and negotiated numerous strategic alliances with semiconductor equipment manufacturers and IDMs.
Farrar received a bachelor's degree and a master's degree in Materials Engineering from Rensselaer Polytechnic Institute.

Where Might Future Semiconductor Productivity Enhancements Come From?

M. Liehr
Executive VP for Innovation & Technology
SUNY Polytechnic Institute, Albany, United States

Abstract
The nanoelectronics industry has enjoyed decades of productivity gains driven by lithographic scaling. However, scaling slowed due to delays in the introduction of extreme ultraviolet (EUV). However, to maintain the pace of die-level cost reduction, a different set of approaches are needed in addition to using EUV.

The advantages of time to market of any productivity enhancement require a model that assures rapid transfer of novel concepts from a lab environment to the fab. Improvements in time to market in the CNSE model will be described. The significant investments required for the development of future scaled technology favor a collaborative government-industry co-investment model. Recent additions to the SUNY Poly technology portfolio will also be discussed.

Specific productivity enhancement for future semiconductor technologies will be elaborated: the performance of the first generation of EUV production scanners, system-level improvements incorporating photonic components and new device materials.

Biography
As CNSE Executive Vice President of Innovation and Technology, Michael Liehr focuses on the creation of new business opportunities and manages integrated industry-university consortia and public-private partnerships. He is also responsible for the effective and efficient operation of the CNSE core strategic CMOS and SiC power semiconductor and packaging partnership engagements, including the IBM, GLOBALFOUNDRIES, General Electric, SEMATECH, AMAT, TEL, and LAM partnerships.

Prior to this assignment, he led the Global 450mm Consortium through the start-up phase as the General Manager. Dr. Liehr is further the Vice President for Research at the College of Nanoscale Science and Engineering in Albany, NY. In this role, he leads the State University of New York's Network of Excellence in Materials and Manufacturing. Prior to joining CNSE, Dr. Liehr served as an IBM executive responsible for Worldwide Semiconductor Manufacturing Strategic Production Alliances for leading-edge semiconductor products.

EU Industrial Electronic Strategy - Where do we stand?

W. van Puymbroeck
Head of Unit A4 Components
European Commission, Brussels, Belgium

Abstract
T B A

Biography
Willy holds a Ph.D in physics from the Universitaire Instelling Antwerpen. He joined the European Commission in the late 80's and throughout his twenty-five year career he has been responsible for research initiatives under different European Framework Programmes. He is the author of several articles in the domain of physics, information technology and integrated manufacturing. Since mid-2011 he is Head of Unit in DG INFSO Nanoelectronics. His responsibilities include Horizon 2020 preparation and stakeholder engagement in the field of electronic components, and the technical, scientific, financial and administrative monitoring of projects.

B. Capraro
Research Manager, Silicon Technology
Intel Ireland Ltd, F24 Research, Leixlip, Ireland

Biography

Bernie received a Masters Degree in Engineering (MEng) from Newcastle upon Tyne Polytechnic (with Distinction) and has been working at Intel for the past 18 years holding various Engineering and Management roles across the wafer fabrication facilities. Bernie is currently responsible for all silicon nanotechnology research involving Intel Ireland, helping to deliver potential solutions to Corporate Intel for materials, devices, equipment and processing techniques required for the future technology nodes in collaboration with Research Centres, Academia and Industry across Ireland and Europe. Bernie's semiconductor career spans 28 years, with other Process and Equipment Engineering positions held at Telefunken GmbH (Ge), Nortel/Bell Northern Research (UK/Canada), Applied Materials (UK) and Newport Wafer Fab (UK).

Lithography roadmap to enable cost effective shrink for future technology nodes

P. Jenkins
Vice President Marketing
ASML, Veldhoven, Netherlands

Abstract
Lithography has been a key enabler of Moore's law through continued progression to shorter wavelengths, higher NA optics and increased productivity.

This presentation will address ASML roadmap for continued productivity scaling, HVM introduction status of the next wavelength, 13.5nm EUV, together with the opportunity for extension to higher NA, and resulting outlook for continued scaling of cost/function per Moore's law.

Biography
Peter Jenkins joined ASML in 1991 where he has held various product and commercial management positions including international assignments to South Korea in 1996 and Hong Kong in 1999. Mr. Jenkins returned to The Netherlands as Vice President of Marketing in 2005.

Prior to joining ASML, Mr. Jenkins gained extensive experience in Lithography and Semiconductor processing at LSI Logic and Plessey Research in the United Kingdom. Peter studied BSc Economics at Bath University, England.

450mm plasma etch module

M. Cooke
CTO - OIPT
Oxford Instruments, Plasma Technology, Bristol, United Kingdom

Abstract
Plasma etching is one technique that offers direct productivity increase by scaling to a larger wafer size. We describe the development of a plasma etch module for 450mm wafers, within the ENIAC project EEM450PR.

The requirement for uniform processing over a larger area triggered two significant changes in approach. At 300mm, a static table was used, with a wafer loading slot above the table. This chamber asymmetry was noticeable at 300mm, but acceptable. At 450mm, it could no longer be tolerated and forced a change to a vertically movable table, so that the wafer loading chamber opening was below the table during processing. Secondly, a tubular ICP plasma source was used at 300mm. The skin depth for power coupling into this plasma is of order 50 - 100mm, so that power is principally coupled into an annulus around the chamber edge. At 450 mm, this tended to starve the centre of the wafer of active species to drive etching, so the induction coupling geometry was changed to a planar form. A mechanical change for improved chamber access was also necessary, because the previous tilted lid method was not practical at the larger scale. Plasma simulation has advanced to the point that it was possible to examine alternative geometries, and even to perform sensitivity analysis, at least to the point of identifying the most critical dimensions, before design the first prototype hardware. We outline briefly an approach to simulation, and its usefulness to the design process.
We present characterisation of the chamber and an etch process, together with an estimation of the cost of ownership compared to the equivalent 300mm tool.
This is offered as a short presentation, intended to be joined to other partner contributions from the project EEM450PR
M Cooke, G Hassall

Biography
Mike Cooke is CTO at Oxford Instruments Plasma Technology (OIPT), responsible for technical developments which have included plasma sources for etching and deposition, plasma-enhanced atomic layer deposition, and ion beam processing tools

Geoff Hassall is Principal Development Scientist at OIPT, and developed the 450mm plasma etch module, with a novel large area plasma source.

450mm module readiness and direct benefit for 300mm yield improvements

A. JARRE
CEO
RECIF Technologies, BLAGNAC, France

Abstract
"450mm module readiness and direct benefit for 300mm yield improvements"

A challenge of the 450 mm introduction is to demonstrate (after prototyping stage) the rationale which allows productivity increase for an IC manufacturer, with economics making business sense also for the Supplier.

Notchless has been standardized taking the opportunity of the 450mm transition to enhance productivity. Recif, as leader in automation, had the opportunity to be involved from the standardization stage up to field trial using "Sorter/EFEM 450mm" installed at imec.

Productivity enhancement is also possible at the R&D stage, through the cross-collaborative concept, the Recif tool installed at imec is evaluated using the "Demonstration Test Methodology" (DTM) in place at G450C and therefore considered as an offsite tool for G450C.

Beyond this 450mm achievement, RECIF will also demonstrate how it was possible to retrofit some of the learning to their latest 300mm wafer handling prototype. It was recently installed at imec within a new collaborative work to demonstrate how it can benefit to the N7 pilot/production lines.

Biography
Alain has over 25 years of international experience in high tech industry (Semi-conductor, Telecom & Smartcard).

Alain started his career with Schlumberger, where he held several technical positions. He then moved to STMicroelectronics for 10 years including 3 years in Japan. Prior to join Recif Technologies in July 2008, he was Deputy General Manager of the Mobile Product Line at Oberthur Card Systems.
Alain holds a Master of Science in Electronic and Computer Sciences Degree and a MBA.

Enhanced Equipment and New Processes as Enabler for Power Technologies on 300mm Substrates

M. Engelhardt
Senior Principal Plasma Etch
Infineon Technologies Austria AG, Villach, Austria

Abstract
Transferring power technologies from 200mm silicon substrates to 300mm provides challenges with regard to substrate materials, process equipment, and unit processes in addition to a similar transfer of standard CMOS. Tight furnace temperature uniformities across the wafers within large wafer batches required severe simulation support. Wafers with polysilicon films on the backside for impurity gettering are so far only available on 200mm. Such films were deposited and analytically assessed. Extremely high doped wafer substrates for manufacturing power devices were not available yet in both sufficient quality and quantity to start 300mm power semiconductor activities and had to be manufactured by epitaxial growth. In addition to severe modifications of the reactors and the provision of the complete infrastructure unit process development is very challenging. Simultaneous achievements of both supreme uniformity of thick epitaxial layers and of the dopant distribution therein is key to allow perfect pattern generation and transfer and hence identical electrical device performance across the wafer until the very wafer edge to take full advantage of the productivity plus.
For IGBTs a 5-wafer epi batch tool was used on 200mm to transfer all the tool and process learning for building a 300mm tool. Hereby the main focus was on the reduction of sliplines resulting from non-uniform thermal substrate-susceptor coupling. While critical CDs in high end products differ by almost an order of magnitude between power semiconductors and standard CD driven CMOS technologies, the tolerated CD uniformities are rather comparable. This finally requires plasma etch equipment with all the "knobs" to address wafer center and wafer periphery individually regarding etch rate, profile shape, and CD to achieve lowest center-edge non-uniformities.
The work has been performed in the project EPT300, co-funded by grants from Austria, Germany, Italy, The Netherlands and the ENIAC Joint Undertaking.

Biography
Manfred holds a PhD in Solid State Physics from 1984 from the University of Regensburg, Germany. He is a 30-year semiconductor industry veteran. In processing of electronic materials he held several positions at Siemens Semiconductors, Infineon Corporate Research, Infineon Memory Products, and Qimonda on the various frontend sites. In his current position with Infineon Austria he is owner of both the equipment and process roadmaps for plasma etch processes for Infineon worldwide. He has pioneered plasma etching of high-aspect-ratio structures and plasma damage assessment methodologies. He has authored and co-authored more than 150 peer-reviewed papers and 90 invention disclosures with more than 50 patents and delivered about 100 presentations on international conferences. Manfred is member-at-large and Fellow of the Electrochemical Society Inc. (ECS) and co-organizer of the bi-annual Plasma Processing Symposium of the Society.

Plasma Dicing 4 Thin Wafers

R. Windemuth
Sales Director Microelectronics Europe
Panasonic Automotive & Industrial Sales Europe GmbH, PFSE, Microelectronics, Haar, Germany

Abstract
Recently many issues came up when using conventional dicing methods. Such conventional methods are mechanical sawing (blade dicing) or laser dicing or stealth dicing. Relevant applications are thin wafers, brittle materials and wafer singulation for very small devices or LED or discretes. Plasma dicing is a recommended method to overcome many challenges of wafer separation. Damage free, water free, particle free and high throughput dicing can be realized by using plasma trench etch (dry etch) technology for dicing. Several technical and equipment aspects will be presented and discussed accordingly. Plasma dicing technology can provide solutions for high rate dicing, beautiful chip shape without any chipping and high bonding strength.
Cost aspects:
The throughput of a plasma chamber depends mainly on wafer thickness and is quite independent from wafer size or chip size. By using plasma for dicing the throughput can achieve more than 4 or 5 wafers per hour. Such cannot be achieved by any line-by-line dicing method as long as small chips are required. Significant cost savings can be expected.
Advantages of plasma dicing are described in detail such as
a. Damage Free / Chipping Free.
b. Increase quantity of chips per wafer
c. Water Free process
d. Flexible Chip Shape
e. Etching speed and characterisation
f. Total Dicing Process Flow
New materials for semiconductor devices are recently coming up on the market. Such as SiC base material and GaN-on-Silicon for power devices and discretes. Future challenges such as SiC dicing or GaN-on-Silicon dicing will be discussed.
Typical topics on Plasma Dicing equipment are explained

Biography
Degree of Diplom-Ingenieur in Process Engineering on Technical University in Munich / Germany in 1988. Since then Project Management & Sales for different kinds of Industy, mainly in chemical Industry. Since 1998 Sales & Project management in Microelectronics & Semiconductor Industry for F&K Delvotec, Wirebonding and Diebonding Technology. Profund experience in handling packaging projects in both Semiconductor and Device-Manufacturing Industry. Since 2006 Sales Director for Microelectronics Equipment at Panasonic Factory Solutions Europe (PFSE). Main target is to establish new PFSE business fields in the Backend and Frontend Industry in Europe: Dieattach, Flipchip, Plasma Cleaning and Plasma Etch Technolgies.

M. Shoval
chairman
Metro450, , Israel

Biography

Menachem Shoval is holding an Electronic Engineering degree since 1973 specializing on Industrial Control Systems. After 10 years of working in different companies and research organizations in Israel Menachem joint Intel to start the first Fab in Israel in 1984.

Menachem spent 28 years in Intel, working in F8, PTD, F18 and TME, fulfilling different engineering tasks, technological tasks and managerial positions. In his last position Menachem was in-charge of introducing Intel with new/ relevant technologies available in Israel and the region, focusing mainly on Lithography and Metrology.

In 2012 Menachem left Intel to start leading the Israeli 'Metro450' consortium as the Chairman of Board.

Wafer Metrology in the 300 - 450 mm / sub 10 era

R. Naftali
CTO
Applied Materials, Kiryat Gat, Israel

Abstract
Wafer inspection tools are used to detect the location of defects on silicon wafers during process development, ramp and high volume manufacturing. The goal of this inspection is to control process stability and improve yield. A significant area of the wafer is scanned by an imaging system which may be based on optical (DUV) or electron (E beam) technology. These systems are characterized by their sensitivity to defect detection, driven by resolution, and by their productivity, driven by throughput.

The drive for high productivity process and process control equipment (e.g. 450 mm silicon wafer diameter) drives the development for high throughput wafer inspection tools. At the same time the required defect detection resolution has decreased towards the sub 10 nm device manufacturing node. The presentation will discuss the challenges associated with high throughput and nanometers scale resolution requirements for next generation wafer inspection tools. Some of the challenges include: a faster motion system; smarter sampling methods; a rapid computing platform and new imaging methods.

Biography
Ron Naftali, chief technology officer of Applied Materials Process Diagnostics and Control Group holds a bachelor of science degree with honors in electrical engineering, a bachelor of arts degree in physics and a master of science degree in electrical engineering from the Technion-Israel Institute of Technology. Ron is an Applied Materials Fellow, a title he has earned for his multiple breakthrough product developments. He holds 58 active patents and patent applications worldwide, including 29 U.S. patents.

Dimensional & Material metrology to meet industry growing needs

S. Wolfling
CTO
Nova Measuring Instruments, Rehovot, Israel

Abstract
Dimensional & Material metrology to meet industry growing needs

Biography
Dr. Shay Wolfling is Nova's Chief Technology Officer, since 2011.
Prior to joining Nova, Dr. Wolfling was an R&D manager at KLA-Tencor-Belgium (formerly ICOS Vision Systems), and a founder and VP R&D of Nano-Or-Technologies (a start-up company for 3D optical measurements).
Shay holds a B.Sc. in physics and mathematics from the Hebrew University of Jerusalem, a M.Sc. in physics from Tel-Aviv University, and a PhD in physics from the Hebrew University of Jerusalem.

Wafer Handling Challenges

N. Karasikov
Senior Vice President & Vice President of Research & Development
NANOMOTION, YOKNEAM, Israel

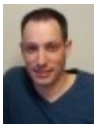
Abstract
The MAGNET Metro450 consortium WP1 is addressing the wafer handling challenges of the evolving Semicon market., including increased throughput, accuracy and cleanliness. The challenge is further manifested by the increase in wafer dimension to 450 mm. Inherently the stage mass increases according to diameter squared or cubed and can reach a moving mass of 100 kg or more. Achieving a high natural frequency, typically required for a precision motion system is becoming practically impossible and advanced solutions of perturbation suppression are being developed. Flatness and Cleanliness are also key factors and the requirements are setting sub-micron flatness and 1 particle contamination for 1000 wafers.
The consortium is addressing these challenges by a set of innovative multi disciplinary motion solution developments for ambient and vacuum environment,.
Advanced solutions are described for contact less acoustic levitation chuck, super flat stage and chuck, XYZT fast stage, fast tracking focus mechanism and Z stage, advanced nonlinear control algorithms to facilitate fast convergence to nanometer accuracy, vibration modeling, passive damping and suppression, piezo-based vibration suppression and advanced composite material structures to yield high stiffness in lower mass.
Actual designs, prototypes and results are presented and discussed.

The consortium is now in its 4th year out of 5. Basic technologies are being developed. Novel building blocks were already demonstrated and the ultimate objective is to integrate the innovative development into a combined demonstrator that will be the base for the next generation motion platform for the 300 and 450 mm wafers, compatible with 10nm nodes.

Biography
Dr. Nir Karasikov - Nanomotion Senior Vice President & Vice President of Research & Development

Dr. Nir Karasikov is Nanomotion's senior Vice President, and Vice President of Research and Development. Dr. Karasikov joined Nanomotion in 1997. Prior to joining Nanomotion, Dr. Karasikov was involved for many years in various hi tech industries, leading the development of infrared systems, electro-optic systems, laser based metrology systems, security systems, image analysis systems and precision mechanical systems for microscopy. Dr. Karasikov has vast experience in developing and introducing new pioneering technologies into the market and in collaboration with major worldwide corporations. Since achieving his Doctorate in Material Science and Solid State Physics from the Technion, Dr. Karasikov has authored over 20 articles in his field, and has invented and patented applications in electro-optics, inspection and piezoelectric related fields.
In the Metro450 consortium Dr. Karasikov manages WP1 and is a member of the consortium Scientific Committee

Sampling Optimization For 450mm Wafers



I. Kaizerman
Machine Vision Group Manager
Applied Materials, Rehovot, Israel

Abstract
The challenge of the inspection companies is to maintain roughly the same per-wafer inspection or defect review time for 450mm wafers as for 300mm wafers. Since the only reason for 450mm conversion is reducing manufacturing cost, if wafer review time will increase with the wafer size - the 'cost reduction' challenge will not be achieved.
One of the obvious solutions is simply trying to speed-up review time. This solution however almost always requires sacrificing other parameters, such as repeatability and sensitivity, in exchange for speed. However, previous trends in this industry showed that in order to achieve sensitive process control, repeatability and sensitivity must improve, not worsen.
One can think of additional methods for maintaining the current time for defect review; Optimization of the sampling plan (explained below) is the most appealing one, as no additional investment in hardware is needed.
Somewhere along the process chain, some of the wafers may be delivered temporarily to an inspection or review unit. This unit reviews defects and sends the data to the host. Usually, this unit has no function in wafer processing; it is there merely to ensure that the process is working correctly. Process control is based on sampling, there is no need to review every defect to maintain control. Today the sampling plans (e.g., how many review locations represent a wafer and how many wafers represent a lot) are fixed, and are set off-line according to the worst case process step sensitivity.
By exploiting the fact that these units already collect data by themselves, sometimes a great deal more than is needed by the host, they may have the ability on their own to decide how frequently sampling should be performed, by introducing a sampling optimizer module inside the defect review unit itself.
The goal of this work group is to demonstrate, by incorporating statistical algorithms into review tools, a smart in-tool sampling mechanism which will improve overall throughput.

Biography
Idan Kaizerman is the manager of machine vision algorithms group in Applied Materials Process Diagnostics and Control business unit. Idan, who holds a M.Sc. in Electrical Engineering from Ben-Gurion University, joined Applied Materials in 2007 and filled a number of key roles in the development of various detection and classification algorithms for wafer inspection and defect review tools. Idan is now managing the group responsible for development of computer vision algorithms combining state of the art procedures for image processing and machine learning.

Analysis and In-Line Monitoring of Non-Visual Crystalline Defects (cNVDs) in Silicon Wafers to Identify Wafers at Risk from breakage

Abstract

Silicon wafers break during different processing within a Si manufacturing fab. Beside the yield-losses, due to lost material and tool availability during cleaning and requalification, each wafer breakage event is accompanied by conventional failure analysis methods that consume much effort, cost and time. In this presentation, we report on recent advance in our research aiming at developing a methodology to identify wafers with an increased risk of breakage during processing.

We used X-ray diffraction imagining (XRDI) technology to map the strain fields in silicon wafers after applying defined impact forces at the wafer bevel, similar to those applied in fab environment by mechanical handlers. We show that slight misalignments in the handers might cause unexpected crystalline damage to the wafer bevel and thus to significantly decrease the wafer's residual strength. To understand the nature of the crystalline damage we used optical microscopy, AFM and SEM and performed finite element analysis. We show that the crystalline damage is dictated by the magnitude of the impact force, indenter (material and geometry) and damage location at the wafer bevel. Controlling these parameters has allowed to generate specific defect shapes and sizes and to generate sub-surface crystalline damage, which might affect the fracture toughness but are not detected by conventional optical surface inspection tools or by SEM. We refer to these defects as crystalline non-visual defects (cNVD).

Recent developments in XRDI allow automatic, fast, precise and accurate inspection of the crystalline damage in silicon wafers within the fab and not just limited to the FA labs. XRDI defects maps are analyzed to identify and classify crystalline defects. We suggest that monitoring the crystalline defects at the wafer edge by XRDI accompanied with actions that keep the tools within specific envelope of mechanical force may reduce wafer breakage ratio.

Biography

Dr. Fouad Atrash received his PhD degree in materials engineering from the Technion in 2010 in the field of fracture dynamics of brittle crystals.

He then served as a researcher and lecturer at the Technion, his main research interest was solving fundamental inquiries in fracture dynamics of brittle single crystals using multi-scale computational methods.

Dr. Fouad joined Jordan Valley semiconductors in 2012 as a Senior physicist. He is leading the development of XRF technology algorithms and projects linking wafer breakage and XRDI technology.

B. van Nooten
Founder
Semi Consulting, Utrecht, Netherlands

Biography

Sebastiaan (Bas) van Nooten graduated with a Master's degree from the Technical University Delft in 1971. After his military service he was involved in processing and design of integrated circuits till 1981 at Telefunken, Germany. After his return to Holland he went to an IC design house as group leader. In 1985 he moved to the semiconductor equipment industry in several positions, mainly as European product specialist for several equipment types. He joined ASM in 1989, first heading the German office in Munich, later as Sales Manager Europe in the Dutch head office. In 2007 he was appointed as Director of European Cooperative Programs, where he was engaged in several European cluster programs, like the Steering Group Technology of Catrene and as project coordinator for ENIAC projects and two 450mm related FP7 Support Actions. Since last year he is an independent consultant to the semiconductor and semiconductor equipment industry. He is the current spokesman of the Steering Committee of the 450mm Equipment & Materials Initiative EEMI450. He has several patents on his name.

Integrating critical sub-fab equipment into future adaptive maintenance methods.

M. Czerniak
Environmental Solutions Business Development Manager
Edwards Ltd, Crawley, United Kingdom

Abstract
As a substantive contributor to fab utility consumption, vacuum and abatement systems provide a focal point for cost reduction. The common themes of "green-mode" and reduction of the threshold barriers to implementation are developed. The pathway to a managed solution is vital and splits into two distinct areas. First formation of knowledge base for green mode actions based on process risk mitigation. Secondly, standardised approaches to distributing that knowledge throughout the broader fab.
In EEM450PR models were constructed to simulate the impact of green modes, at various levels of wafer fab utilisation, initially for 300mm, and then extended for a hypothetical 450mm fab. It was also noted that additional savings would be possible in the facility. The model was then validated by looking at data from a representative high volume manufacturing 300mm fab, simulating the impact of green modes (without actually implementing them), and also live green mode implementation on pumps and abatement at a R+D lab in Europe.
In G450C, Edwards' emphasis has been the risk mitigation elements and to capture sub-fab data analytics as a solid foundation for implementation of green modes in 450mm. / advanced node high volume manufacturing. Through incorporating vacuum as a key variable during the process qualification of the installed tools and then monitoring changes in this captured data, the basis for methodologies for risk mitigation are being designed for advanced vacuum systems..
Underpinning the data analytics is the requirement to ensure that data capture is robust & easily and precisely disseminated across the future fab wide information topologies. Central to this is the provision of standardised and agnostic interfaces and within this approach, a clear and strong focus on tool-centricity.
The aim is to provide the material conditions for the progressive (fab and sub-fab synchronised) introduction of adaptive / condition-based maintenance modalities.

Biography
Following obtaining his doctorate in Electrical engineering from Manchester University in 1982, Mike started full-time work at Philips' UK R+D labs in Redhill, UK, working on the MOCVD growth of II-V materials, followed by 2 years in Holland transferring a III-V MOCVD process into the Nijmegen fab.
Mike returned to the UK with Cambridge Instruments, a MOCVD OEM as a Product Specialist, before working at Courtaulds Advanced Materials in Business Development roles. He moved to UHV OEM VSW, then joined VG Semicon as Product Manager for MBE UHV systems. He joined Edwards 19 years ago, working through a number of roles before starting his current job this year as Environmental Solutions Business development Manager.

Fully Automated Vendor Lot Start

S. Puelm
MTS Program Management
GLOBALFOUNDRIES Dresden Module One Limited Liability Company & Co. KG, FICS DEVELOPMENT, Dresden, Germany

Abstract
Following the Industry 4.0 approach, GLOBALFOUNDRIES has implemented a fully automated vendor lot start process, covering the entire wafer material supply chain.
In the new process, each raw wafer that is delivered to GLOBALFOUNDRIES has its certification automatically checked, is registered in all manufacturing IT systems and is transferred to sorters and FOUPs (Front-Opening Unified Pod), which are the containers in which wafers are transported through the manufacturing process. This automated handling replaces five manual steps, and integrates several former lot start processes.
This solution is an important step for fully automated FAB logistics and wafer start. It covers:
* Automation of wafer material registration at Lot start
* Automated synchronization of supplier data with incoming physical wafers
* Certificate release procedure
* Automated transfer from FOSB to FOUP
* Automated vendor lot start in MES
The presentation will show the implanted (consider grafted?) business process, and will highlight implementation details, such as Supplier involvement and standardized COA data transfer, as well as the FOSB recognition hardware preconditions.

Biography
Stephan Puelm:
After studying physics with areas of concentration in fields surface science and semiconductor physics, Stephan Puelm worked as a software engineer at Sympatec GmbH (particle size analysis system vendor). In 1999, he transferred over to GSM GmbH as branch lead (software and project management consultant). Since 2006, he has worked in the semiconductor industry. He worked at Qimonda from 2006 to 2010, then transferred over to GLOBALFOUNDRIES as a project lead for automation projects.

Tony Genenncher:
Mr. Genenncher is currently working as project lead and application engineer for Logistics at GLOBALFOUNDRIES. In 2000, he started an apprenticeship in micro-technology in cooperation with AMD and the Bildungszentrum für Hochtechnologie GmbH. As a member of the Production Control Department, he was involved in the ramp-up of AMD's then new Fab36 in 2005. After he completed his studies in mechatronics in 2011, he began work for Fab Logistics Support at GLOBALFOUNDRIES, where he continues to make significant contributions.

Advanced Semiconductor Manufacturing Fabs: A View from a Gas and Material Supplier

J.-C. Cigal
Programme Manager
Linde AG, Pullach, Germany

Abstract
With the implementation of advanced technology nodes below 20nm, semiconductor companies are facing a dramatic increase of manufacturing costs. Furthermore, the consolidation of the industry into few leading edge manufacturers is inevitably leading to the emergence of larger fabs. Gas companies are preparing themselves for this rapid metamorphosis of the industry landscape.

Whether or not the transition to 450nm happens, economies of scale need to be addressed, as the demand for gases is drastically increasing. The consequences for bulk gases delivery (nitrogen, argon, and hydrogen) need to be assessed and delivery strategies must be developed and implemented. In many cases, the standard truck delivery scheme is to be replaced by on-site production.

The logistics of cylinders needs to be revamped as well. The materials supply chain has become truly globalized and material companies are facing new challenges to avoid any interruption of product delivery.

At the same time, material quality requirements are reaching levels never observed in the industry before. New and innovative material quality controls are required all along the supply chain. New analytic methods also need to be developed to challenge the current detection limits.

Finally, limited natural resources need to be addressed. Innovative solutions like materials recycling can be a useful tool in reducing environmental impact.

Biography
Jean-Charles Cigal is currently Programme Manager at Linde Electronics. In his role, Jean-Charles helps customers and equipment manufacturers with technical support to achieve their roadmap with the introduction of new processes and materials. He joined Linde as principal technologist in 2009, where he was technology consultant for the semiconductor and the photovoltaic industry.

Prior joining the Linde Group, Jean-Charles worked several years as senior process engineer in the semiconductor industry.

He owns a M.Sc. in Applied Physics from Pierre et Marie Curie University, Paris, France, and a PhD in Applied Physics from Eindhoven University of Technology, the Netherlands.