17th European Manufacturing Test Conference (EMTC)

R. Segers
chairman
ReSeCo, XXXX, Netherlands

Biography
After getting his degree from the University in Eindhoven, Rene Segers started his professional career at Philips. Rene held technical and managerial positions in various divisions from Philips, including Research, Consumer Electronics, the Centre for Manufacturing Technology and Philips Semiconductors which later became NXP. Technically, over the years the focus has broadened from just DfT in the first couple of years, towards Test and Product Engineering, Diagnosis, DfX and supply chain management. The last couple of years of his career at NXP, Rene was responsible for the Test and DfX strategy as well as for its implementation in the global NXP.
Rene left NXP in 2009 and is since then active as an independent consultant, supporting mainly start-ups and smaller companies in developing their business. Rene maintains many contacts in the industry in Europe, Asia and the USA.
Rene plays a key role in 2 European conferences, the EMTC and the ETS2.
Between 1988 and 2004, Rene was also as a (part-time) professor at the University of Eindhoven, teaching DfT and Testing of electronic circuitry.

Silicon, Interconnect, Packaging and Test Challenges from a Foundry Viewpoint

M. Bonkass
Director Bump Test Facility
GLOBALFOUNDRIES Dresden, Dresden, Germany

Abstract
Beyond the complex wafer fabrication processes starts a very challenging world of silicon interconnect, packaging and test. Many aspects of leading edge fab processes drive for smaller and dense die-to-die interconnects as well as next technology stage packing and test challenges. The cost of silicon scaling effects rapidly increases. New packaging solutions have to balance the performance, power and cost. Chip-Package-Interaction (CPI) at leading edge technology nodes become a very complex system containing different types of material which require new ways of controlling mechanical and electrical stress. While new bump technologies allow reducing cost with the introduction of new materials the overall test cost trend increases.
The key note speech will highlight the industry trends, technical challenges and potential solutions addressing those areas. The foundry point of view offers a summary for the various trends seen in the industry.

Biography
Matthias was a member of the Dresden startup teams for AMD Fab30 (200mm) in 1997 and AMD Fab36 (300mm) in 2004.

He started his career as a CMP/Plating process engineering back in 1997 with long term assignments in AMD Sunnyvale/California. After holding several operation management positions in the 200mm and 300mm lines he became a Module Manager in CMP/Plating in Fab1 in 2007. In 2012 he became the Module Manager for GLOBALFOUNDRIES Fab1 Thin Films. Since 2013 he has been the Director of the Bump Test Facility (BTF) in GLOBALFOUNDRIES Fab1.
Matthias holds a degree of electrical engineering of University of Applied Science Lausitz.

P. van Ulsen
CEO
Salland Engineering (Europe) BV, Zwolle, Netherlands

Biography

Paul van Ulsen Chief Executive Officer and President
Paul is responsible for all aspects of corporate governance for Salland Engineering worldwide. Paul joined Salland in 1993 as a test applications engineer. He became Manager of the Test Applications business unit and soon demonstrated his sales skills as Managing Director for Salland Europe. Investors and managers recognized that Paul had a vision to build Salland into a major player in the market for semiconductor test and he was appointed CEO in 2001. His leadership has guided Salland to becoming one of the largest suppliers of test productivity products and services in the world. Prior to Salland, Paul worked for Rood Testhouse International as a mixed-signal applications engineering. He is a graduate of Windesheim Technical University in electronics and computer engineering.

Small is Beautiful - Time-to-Market Estimates with 'Smart' Data Analyses

G. Karner
Director
optimiSE, Karlsruhe, Germany

Abstract
Statistical Data Analysis is recognised as a method for extracting knowledge from large data sets. The latest example is 'Big Data', which claims to explain 'everything'.

In semiconductor production, however, the application of this doctrine runs into a serious obstacle:

(i) The crucial phase in the semiconductor life-cycle is the ramp-up period, characterised by the quest for maximal quality in minimal time-to-market. Naturally, during this span the amount of analysable test data is (rather) limited.

(ii) Once the roll-out is achieved, the data volume grows rapidly. Yet, the coercion for test optimisation declines proportionally to the number of STDF logs and data graveyards sprawl while the engineer's mind is already set onto the next product.

Thus, when the talk is about New Product Introduction (NPI) in the semicon industry, the order of the day is 'Smart' rather than 'Big' Data!

The present note introduces a new approach to the analysis of test data collected during the NPI phase.

The backbone of that algorithm is Trend Estimation, a statistical technique allowing the construction of a model independent of 'anything' known about the underlying process. Trend Estimation employs the Ordinary Least Square Estimator as the best linear unbiased estimator, if the requirements of the Gauss-Markov Theorem are met.

Therefore, the first part of the analysis demonstrates that the specific Trend Model indeed represents the NPI test set-up. Thereafter, the NPI tests are qualified with respect to their temporal and spatial coherence into stationary and non-stationary entities by means of a Time Series analysis.

To accelerate improvement of non-stationary tests, a drill-down feature relates jumps in sublot autocorrelations to local quality issues on the wafer. It acts as a precursor to root-cause analyses done by specialists.

At last, based on the analysis of current data, a prediction on the time remaining to reach stationarity is presented for each test.

Biography
Born 1959, Austrian Nationality, married

PhD in Mathematical Physics from the University of Graz, Austria

Research and Teaching in Germany, France and the US

Founder of optimiSE GmbH in 2001 (as spin-off from the University of Karlsruhe, Germany)

Executive Director of optimiSE ever since

Knowledge in mathematical modelling and evaluation of non-linear processes (such as testing of semiconductors)

The Quest for Quality and Yield Improvement for High Speed Serial Interfaces in Vehicles

N. Leblond
Senior Application Engineer
Galaxy Semiconductor, Applications, Grenoble, France

Abstract
Inova Semiconductors GmbH is a fabless semiconductor manufacturer headquartered in Munich, Germany, which specializes in the development of products for Gigabit/s serial data communication. As vehicle manufacturers deploy intelligent driver assistance systems and eventually even self-driving cars, the need for high speed serial interfaces between cameras, displays and video units is skyrocketing. Because of the mission -critical nature of these automotive applications, Inova has demonstrated a strong focus on quality and reliability, while also keeping costs under control.
In this paper we will describe the advanced test techniques that we have put in place, including Part Average Test (PAT) and Statistical Yield Analysis (SYA) to eliminate outliers and maverick lots. We will also describe our analysis of field returns using a die traceability capability that helps us recreate the wafer map from which the failing die originate and looking for systematic process problems. We will provide specific examples that illustrate how the combination of advanced test techniques and detailed failure analysis has helped us improve the manufacturing process to achieve better quality and yield at the same time.
This paper is coauthored with Lothar Doni Director Quality Assurance at Inova Semiconductors GmbH and Nicolas Leblond Senior Application Engineer at Galaxy

Biography
Nicolas Leblond holds an Engineering degree from INP Grenoble and specialized in Microelectronics. He has been working for more than 10 years in the software and semiconductor industries, in startups as well as in larger companies like Xilinx. He is now Senior Application Engineer at Galaxy Semiconductor and provides technical support for customers in Europe, Asia and USA.
Lothar Doni is currently Head of quality assurance at Inova Semiconductors. He worked as unit process engineer and team leader at Infineon in Villach and in development alliance for 45/65nm in Fishkill, as process engineer at Steag Microtec and studied micro system technology at university of applied science in Regensburg

P. Cockburn
Senior Product Manager
Xcerra, xxxx, United Kingdom

Biography

Peter Cockburn has worked in the ATE industry for over 25 years at Schlumberger, NPTest, Credence, LTXCredence and now Xcerra. He has developed real-time and GUI software for ATE systems, managed the launch of several SOC ATE systems and new analog test options and provided marketing and sales support in USA, Asia and Europe. As Product Manager in the Test Cell Innovation team, he is now defining new ways to reduce cost, increase uptime and improve quality when testing semiconductors. He has an Engineering degree from the University of Southampton, UK.

Electrical Overstress (EOS) of Semiconductors (SC) in Automotive Applications, Root Causes, and Conclusions

C. Thienel
Head of Department
Robert Bosch GmbH, AE/EIQ, Reutlingen, Germany

Abstract
In automotive business customers urgently want to get solutions in case of damaged parts. Thus a short, simple, consistent description of EOS is mandatory. Today there are many diversifications of EOS. We try to describe the EOS phenomenon from customers` point of view by a simple and universal, but consistent approach. So, we are striving for congruence of real electrical stress levels in applications and the amount of stress the device is able to withstand, the resilience.

Our sole reference is the SC device specification. It is the exclusive interface between customer and supplier and it contains the entire information we need to know for judging about EOS. Electrical Overstress is every electrical stress situation for a SC beyond Absolute Maximum Rating (AMR).

There are two kinds of destroyed SC devices: Weak parts (defect inside) are failing being operated under specified conditions and on the other hand parts being damaged by out of specification operation mode. In the first case supplier needs to improve his process (reduction of defect density) and in second case customers` processes must be investigated for EOS root causes.
Electrostatic Discharge (ESD) is a normal electrical stress and is one part of our EOS definition. According to specification there is also a limit for ESD operation, which is not allowed to be exceeded.
This understanding of EOS and ESD is very successful for our business.
We will show several clusters of root causes we found and will conclude for all involved levels of automotive industry from supplier to final customer.
We want to contribute to a better understanding and global avoidance of EOS.

Biography
1956 born in Bamberg, Bavaria
1984 diploma in physics from Friedrich-Alexander-University in Erlangen, Bavaria
since 1984 with Robert Bosch GmbH in Reutlingen

Experience in design, test, qualification, release, and analysis of SC for more than 25 years in SC area of Robert Bosch GmbH, Reutlingen.
Therefrom 10 years intensive work in global EOS area.
100 linewalks worldwide in assembly lines of car manufacturers.
Chairman of working group "first-mate-last-break" of German Electric and Electronic Manufacturers` Association, ZVEI, and edition of a whitepaper "Introduction of FMLB contacts in automotive industry", www.zvei.org/first-mate-last-break.

An Intelligent Temperature Sensing Application Circuit in Eradicating Temperature Induced Variance on Performance Board Hemispheres

L.C. Landicho
Test Development Engineer/ Professor-Lecturer
AMS-Asia / De La Salle University Manila, Test Development Engineering / Electronics Engineering, Calamba, Philippines

Abstract

This paper presents a circuit application of a temperature transducer. An application circuit used to sense the variance of temperature level between performance board hemispheres. The temperature level is linearly converted into micro-amperes (uA). Moreover, the circuit design has the capability of sensing the variance between hemispheres where different test sites were mapped. A site to site variance was observed due to heating of performance board used in 150 degree Celsius testing. This event was solved with the aid of equipoise temperature sensing between performance board hemispheres. The application circuit provide the most precise feedback through its 1uA/K linearity, and display the most accurate result to be used in monitoring parametric readings. This application will use an on-the-fly performance board temperature calibration. A threshold temperature was set to greater than 80 degrees Celsius. Once this threshold temperature is exceeded, the application should execute an on the fly temperature calibration to define a site-specific correction factor. A performance board checker also performs a thermal equilibrium check of about less than 0.1% before proceeding with 150 degrees Celsius testing. Through implementing the application circuit, performance board is being stabilized.

Biography

During Design for Manufacturability (DFM) consideration, temperature consistency is considered on performance board designs. This consideration is limited only up to certain temperature level due to characterized performance of the materials and components used during hardware design. However, due to uncontrolled heat transfer the resistivity levels of board design could be affected. The said resistivity level has a direct relationship on the current and differential voltage level during the manufacturing run. A deviation on parametric measurement was seen, when a certain Device-Under-Test (DUT) is exposed and soaked from a boiling point temperature up to 150 degrees Celsius. A drift on digital levels was observed and yield loss becomes gross. This causes an unexpected fall on unit per hour (UPH), which can be converted into a negative cost. On the other hand, the solution made on the said event was to have a precise and real-time feedback on board hemispheres temperature. Dictate the system on the hardware condition drift due to rise on board hemispheres temperature. Provide a stop and deliver a signal that would restore the equipoise ambient temperature expected on both hemisphere of the board.

A proposal for full test line automation at package level of SoC, under the very high test time paradigm

L. Moriconi
Test Application Division Manager
ELES Semiconductor Equipment Spa, Todi, Italy

Abstract
The present paper proposes an innovative automation solution that allows to overcome the high test time paradigm achieving a cost of test and complexity reduction with respect to the current approach based only low parallelism test architecture. This can be achieved by partitioning the test between a Massively parallel Low cost Tester and a standard ATE integrated with a low handling parallelism in a fully automated test line. In addition to that, the solution is able to perform adaptive test and embed reliability stress tests that can be analysed and used to guarantee maximum quality.
Semiconductor products are becoming more and more complex and the expectations in terms of quality and reliability are growing especially in the automotive market, thus requiring the need for new test strategies: i.e.

Application Specific tests, Re-configurability and Repair, Subtle defect screening. In this scenario the test time is going to increase from few seconds to probably minutes.
The traditional approach - i.e. Pick&Place Handlers - that focuses on increasing the handling parallelism does not seem to be the most efficient answer. Complexity and cost would go dramatically up. ITRS Roadmap for Multisite Test at package level of MCU low power indicates that para 32 will be probably the limit for next years. As a consequence, new test arrangements need to be considered for a more cost effective solution.
The aim of this paper is to propose an innovative Test Cell, fully automated, that bypasses the need of a high

handling parallelism to manage the growing complexity. This solution is a fully integrated Test Cell in which N

different Test stations are connected and different test insertions are managed within the same automated line; the device handling, loading/unloading for all the test insertions is fully automated as well.

Biography
Luca Moriconi holds a degree in Electronic Engineering from the University of Perugia, Italy.

Luca joined ELES Semiconductor Equipment in 1999 and worked in the semiconductor reliability and testing industry as Senior application engineer and Test Application Division Manager.
Luca in 2015 became Head of Technology and Solutions at Eles supporting the definition of the technical roadmap for the different solutions and the business development activities.

C. PORTELLI-HALE
Operational Programs Director
ST Microelectronics, SPA Front-End Manufacturing & Technology R&D, Rousset, France

Biography

Chris Portelli-Hale holds the post of Operational Programs Director in the Manufacturing Execution Excellence team within the Front-End Manufacturing & Technology R&D organization of ST Microelectronics, based in Rousset France.

He holds a degree in Electronics Engineering from the University of Malta and joined ST in 1989 where he has held various positions is Test Engineering and Test Operations

Management within different organizations and locations of the company in Malta, France and Singapore.

Chris is Chairman of CAST the Collaborative Alliance of Semiconductor Test group which brings together several actors within the test arena from IDMs, Fabless and Equipment vendors.

Ainslie Stuart

S. Ainslie
Director Business Development
Advantest Europe GmbH, Munich, Germany

Biography

With over 25 years experience in the semiconductor industry Stuart Ainslie has been with Advantest for 19 years and is currently Director of the business development group located in Munich.

In Advantest Stuart worked as an applications engineer before joining the marketing group in 2000. Stuart originally studied Electronics and Electrical Engineering in his native Fife Scotland and in 2008 was awarded an MBA from the Open University (UK).

Stuart is married with two children and lives in Munich.

Final Test Solution of WLCSP

A. Nagy
Senior Director Marketing Handler & TCI
Xcerra, Rosenheim, Germany

Abstract
Wafer Level Chip Scale Package (WLCSP) devices are used because they offer low cost, small footprint packages to be directly mounted into smartphones, tablet PC's and other mobile devices. They are even used in automotive applications. The manufacturers of these mobile and automotive application devices are demanding lower defect parts per million (DPPM) from their suppliers of WLCSP devices.

Today, the backend process flow for mobile WLCSP devices is a single insertion test at wafer probe. With this flow, test is only performed prior to device singulation (wafer saw). The reason for this flow is that there has been no cost effective way to handle singulated WLCSP devices in a high volume manufacturing (HVM) environment.

Xcerra's proposal is using InCarrier (device carrier) technology to solve this market requirement. InCarrier technology was designed to secure up to hundreds of singulated devices in an array similar in format to a device strip. By placing the singulated devices into an InCarrier, the InStrip device handler can then be used to provide Final Tri-temp Test of WLCSP devices.

This paper will explore some of the key attributes and technical challenges in testing singulated WLCSP devices. Topics to be explored include:

- Backend process flow and machinery required
- Device handling, alignment and retention of delicate WLCSP devices
- Device placement accuracy required for multi-site test of WLCSP and impact on yield
- Methodology to retain data for wafer map even though wafer sort test is not done
- Test cell efficiency gain enabled by InCarrier

InStrip / InCarrier WLCSP solution is in development now and is planned to be evaluated in a HVM environment before the Semicon Penang conference.

Biography
Dipl. Ing. Andreas Nagy is Senior Director Marketing for Xcerra's Handler Group and TCI (Test Cell Innovation). He holds a degree in Mechanical Engineering from the Technical University of Munich. After graduation, Nagy spent two years in the semiconductor industry as a design engineer prior to his six year tenure in the printing industry. Upon his return to the semiconductor business, Nagy became Multitest's Business Unit Manager for Engineering Driven Business. With the foundation of Xcerra in 2014 Andreas Nagy took over the responsibility for Marketing with the Handler and TCI Group.

Vock Stefan

Biography

Stefan Vock Biography Stefan Vock is holding a Diplom-Ingenieur (FH) degree from the University of Applied Science Augsburg and a Master degree in Electronic Systems with distinction from the University of Ulster. He received the designation of European Engineer (EUR ING) in 2009. Mr. Vock has been in the Automated Test Equipment (ATE) industry for more than 20 years delivering professional services to: ATE vendors like credence and Teradyne, and to design houses as well as to integrated device manufactures (IDM), and today to Infineon in the area test technology and innovation. Further he is currently a Ph.D. candidate at the University of Ulster with the research focus on semiconductor test engineering.

R. Richter
President
Ebara Precision Machinery GmbH, Hanau, Germany

Biography
Reinhart Richter has recently been appointed President of EBARA Precision Machinery Europe GmbH.

Previously he has worked for over 13 years at Multitest as Vice President sales and marketing and later President successfully promoting the company's transition to a leading edge solution supplier for advanced test handlers, test sockets and DUT boards. After the acquisition of Multitest by LTX-Credence he served the newly formed Xcerra Corp. as Chief Technology Officer. Prior to Multitest he held various positions at KLA-Tencor Corp., BBN Inc., and IABG.

Reinhart Richter holds a M.Sc. and Ph.D. in Solid State Physics from McGill University, Montreal, Canada, and has authored over a dozen peer reviewed scientific papers.

Architecture of an Efficient MEMS Final Test System

M. Brucke
Head of R&D Department
SPEKTRA Schwingungstechnik und Akustik GmbH Dresden, Dresden, Germany

Abstract
MEMS final test systems face various requirements. On the one hand consumer MEMS require a short time to market and thus an early test qualification for a fast production ramp up as well as the capability to allow large volume production. On the other hand automotive or niche MEMS require an excellent scalability of the test system in order to adapt to the production volume in different product life cycles. This paper suggests a test hardware and software architecture that can be scaled from a two channel desktop system to a several hundred channel multisite production test system. Since the scalability allows the use of the same hardware platform at reasonable low costs in the development department as well as in the mass production, the setup and qualification of tests can already start in development phase and thus shorten the time to market. Furthermore it can be configured very flexibly to adapt to the requirements of new MEMS generations easily while still supporting older generations at the end of their life cycle.
By focusing on technical parameters that are typically required for the final test of MEMS devices, all required functions like device power supply, digital interfaces and analog measurement capabilities are integrated on one board allowing an excellent scalability at lowest possible investment. By means of an onboard FPGA digital interfaces like I^2C, SPI, SENT, JTAG, PSI5, CAN and others can be easily and flexibly configured on hardware level reducing the software coding effort. Additionally a microcontroller with real-time kernel on each board allows a parallel operation on a variable number of test channels without a high overhead in the communication between host and test system. The coding, qualification and deployment of tests is handled efficiently by a software framework that fits to the system and supports small development systems as well as complete production sites.

Biography
Dr. Martin Brucke received his PhD in Mechanical Engineering from the Technical University Braunschweig, Germany. He works since ten years as head of the SPEKTRA R&D department.

Multi-site Probing of Magnetic Sensors at 175 deg C

G. Gouwy
Process Owner Probing
Melexis, Process, Ieper, Belgium

Abstract
The rapidly-growing sensor market for automotive and other industries is driving innovations in semiconductor wafer test. Stringent safety and reliability standards requires extreme tests, including tests at high/low temperatures, which is notoriously difficult to achieve at the wafer level, due to uncontrolled movements of the various parts of the test-cell (probe card, prober components and probe-card interface, etc..), which affect yields, pad damage, bonding reliability, and test through-put. In addition, sensors require stimuli (pressure, magnetic fields, light, etc.) in addition to electrical tests. As such stimuli are difficult or impossible to apply during wafer test, sensors are often tested in special handlers, individually, and after device packaging. The cost of this method is very high because more test systems are required, and bad devices are packaged along with good ones. So, unless device volumes are very low, wafer-level test of multiple devices in parallel is usually desirable. However, achieving this is not easy.

The stimulus requires equipment that often interferes with the tester/prober interface. Often the probe card is a physical barrier, preventing access to the device. This presentation will describe how Melexis successfully implemented multi-site (x8) testing of magnetic devices at temperatures up to 175 deg. C, while applying a uniform magnetic field to all devices. The key elements included in the presentation will be:

- The challenges and requirements of probing of magnetic sensors in parallel and over a wide temperature range
- The development of the probing hardware (magnetic source, prober interface, probe card)
- The test results which validated the probing hardware
- Best practices for probing at high/low temperatures

Biography
Melexis
- Geert Gouwy,
- Olivier Dubrulle
- Lindsey Ameele
- Frederic Plancke
- Filip Beyens
- Peter Schops

Melexis Internship
- Ruth Verheyen

JEM
- Joe Mai
- Christopher Mackanic
- Sebastien Perino

J. Mai
Managing Director
JEM Europe, Montbonnot-Saint-Martin, France

Biography

Joe Mai is founder and managing director of the European subsidiary of Japan Electronic Materials (JEM), a leader in wafer-probing technologies, for whom he's worked for over 20 years, playing both technical and business-development roles in the US, Europe and Asia. His technical experience includes product R&D, PCB design, automation, and applications engineering. During these past two decades, he has worked closely with many customers to improve their test capabilities and develop JEM's technologies.

Presto! A test element driven test program Generator for Test Probe

U. Schiessl
Production Test Engineer
Texas Instruments Deutschland Gmbh, FTEST, Freising, Germany

Abstract
New technologies in semiconductor industries in the last 10 years trend to grow more and more complex. State of the art technologies today are supporting > 70 flows and > 100 technology elements. Those elements can be technology design components (MOS/Bipolar transistors, diodes, resistors etc.) or Fab control structures like Vias, contacts, GOI etc. Whereas Scribe Line test programs for wafer test probe in the past, consisted of ~100 tests, today the generation of several thousand tests per program is necessary to provide support for all the requirements specified in a Process Control Document. Utilizing adaptive test in combination with component based test is a modern strategy in wafer test probe to handle multiple flow and component technologies. This reduces the sustaining effort by maintaining only one test program per technology. Latest trends in Scribe line layout start to implement strategies, which no longer place all the Scribe Line modules of a given technology on each device, but limit the module placement to those, supporting only technology elements, which are crucial for device layout and functionality. This trend, however, increases the sustaining effort for the supporting test engineer considerably - he must now support multiple programs for a given technology. To allow a test engineer to still handle such requirements, new tools need to be provided.
The authors are presenting Presto! an innovative element driven test program generator for test probe. It can cut down development times of several days to several hours. Presto associates to each technology element a parameterized test sequence with one/more variable groups (Patent TI-74851). Additional concepts like multiple sub element support, as well as Inter/ Intra Dut/module provide a flexibility to 100 % port mature manually generated programs to an automated test platform. Once generated, test sequences can be easily reused in a building block manner or ported to other technologies.

Biography
Uwe Schiessl joined TI in 2000 as a characterization engineer in the parametric test group. He is a Member Group Technical Staff since 2015 and has a physics diploma from the University of Heidelberg.
Istvan Bauer joined TI in 2011 as a Product Engineer in the TSDS group working on multiple parametric test optimization projects. He has a MS EE diploma from University of Texas at Dallas.
Shannon Wilmes joined TI as a co-op in 1994 and currently works as a software design engineer. He has primarily worked on automation solutions related to physical design, final test program generation and parametric test program generation. He has a BS degrees in Electrical Engineering and Mathematics from Southern Methodist University in Dallas, TX.

Probe Card Identification via RFID

M. Sapienza
EWS Europe - Advanced Automation team leader
STMicroelectronics, Catania, Italy

Abstract
At Electrical Wafer Sort (EWS), the probe card represents a fundamental and mandatory component of the test cell and hence a key entity for the process. Exactly like tester and prober, the probe card must be unequivocally and automatically identified for performing EWS testing as for any other usage. Once identified, it is possible to verify if it is the correct one for the intended operation.
However, when the probe card is manufactured, it is not supplied with a solution for identifying itself automatically.
To address this need, a low cost solution, called "Probe Card Identification via RFID", has been identified and implemented at ST EWS: Probe card identification task is achieved through Radio Frequency Identification, RFID. The choice of applying RFID derives from the need of finding a solution not embedded into the test cell, with minimum hardware impact and not introducing any limitation into the regular test cell operability. Likewise, RFID technology offers the big advantage that the reading operation requires neither any physical contact between receiver and transmitter nor line of sight.
Probe card name acquisition carries other benefits:
- securing the process integrity as automation is able to perform accurate probe card data validation avoiding misprocessing
- yield improvement through probe card status monitoring as well as reduction of retests due to probe card issues
- ensuring full probe card traceability as probe card relevant events throughout its lifetime can be traced and associated to the correct probe card
- strengthening process traceability through touchdowns tracking allowing both to perform scheduled maintenance operations and continuous benchmarking for all suppliers
- quality improvement by reducing squashes on final passivation and preventing any exposure of underlying PAD layers
This paper describes the RFID Probe Card Identification solution design and development, field results and its implementation in the EWS test manufacturing process

Biography
Massimo Sapienza holds a master degree in Electronic Engineering from the University of Catania, Italy. He joined STMicroelectronics in 1999 where he worked for 10 years in Electrical Wafer Sort department in Catania holding several roles linked to Automation and System and data administration. In 2009, he joined Front-End Manufacturing and Technology EWS Europe & EWS Technology - Test Engineering R&D and Automation leading the team of Advanced Automation & Process Flow Standardization Project Management.