Lithography Session

Full wafer scale NanoImprint and Mask Less Lithography status and synergies for advanced manufacturing and pre prototyping at LETI

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Abstract
In the lithography landscape, extreme-UV (EUV) lithography technology is now implemented in manufacturing lines. Meanwhile, 193nm immersion lithography, with multiple-patterning strategies, is still widely supporting the industry requirements for advanced-node develop¬ments, despite the tremendous effort required for process controls. Although these two options are suitable for high volume manufacturing, more affordable technologies are still needed for R&D evaluations, pre-prototyping and small scale productions.
In such landscape, lithography alternatives maintain promise because they may present competitive compromises for the industry. Massively parallel electron-beam and nano-imprint lithography techniques remain highly attractive, as they can provide noteworthy cost-of-ownership benefits. In addition, directed self-assembly (DSA) lithog¬raphy shows promising resolution capabilities and appears to be an option to reduce multi-patterning strategies, and therefore the associated mask-set budgets. Even if large amount of efforts are dedicated to overcome the lithography side issues of these new patterning solutions, they introduce also new challenges and opportunities for the integration schemes.
Through three collaborative R&D programs, IDEAL for Directed Self-Assembly Lithography, IMAGINE for Massively Parallel Electron Beam Lithography and INSPIRE for NanoImprint Lithography, CEA-Leti is currently assessing and boosting the development of these alternative technologies through strategic partnerships and innovative mix of them. In this paper, we will present how the development of the Massively Parallel Electron Beam Lithography may contribute to strengthen the supply chain of the NanoImprint Lithography through master manufacturing capabilities. We will review both Massively Parallel Electron Beam and NanoImprint Lithography technology status at CEA-LETI and then show some realizations.

Biography
Stefan LANDIS, Senior Scientist, received his Master's Degree in Engineering in Physics and Solid State Physics, from the INPG Grenoble Engineering School and his Master of Science (MSc) in Quantum & Statistical Physics from Grenoble University. After a PhD thesis in patterned magnetic media for ultra-high density recording, he joined in 2001 the Lithography Laboratory of CEA-LETI to develop high resolution Ebeam lithography processes for CMOS devices. Then he has been in charge of the NanoImprint lithography activity for 14 years and recently managed the Multi Electron Beam Lithography Project at LETI for the development and qualification of the Mapper Lithography solution. He is now working on business development for patterning activities and services available at LETI.

Author or co-author of more than 70 papers and 30 patents, Stefan Landis has edited two books Nanolithography and Lithography (ISTE-Wiley, 2011) and contributed to Plasma Etching for CMOS Device Realization book (ISTE Press- Elsevier, 2017).

Direct Imaging Solutions for Advanced Fan-Out Wafer-Level and Panel-Level Packaging

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Abstract

In recent years, the increasing use of smartphones and other mobile devices has created a demand for even higher integration, speed and miniaturization of devices. As scaling according to Moore´s Law is slowing down, the industry is focusing to boost device performance by advancing in 3D integration and packaging. This trend has motivated SCREEN to develop an entire line-up of direct imaging systems for both application spaces - Wafer-Level and Panel-Level Packaging.

This talk will outline the specific challenges an exposure tool has to cope with in the packaging arena. A unique method of image creation by using a proprietary spatial light modulator will be presented as well as image correction functions, that automatically adjust exposure data to prevent alignment errors. This feature resolves the previously challenging issue of positional deviation when rearranging the individual dies for fan-out processing.

Biography

Mark Goeke received his Master of Science in Photo Engineering from the University of Applied Science, Cologne in 1994.

After holding various positions in lithography engineering he started working with Dainippon Screen Mfg.Co. (now Screen SPE, Germany) in 1999.

Here he moved to hold the position of the Europen Product Engineering Manager, responsible for engineering, technology and product marketing for Screen´s product lines of lithography and single wafer processor equipment.