Materials

J. Dekoster
Program Manager
imec, Leuven, Belgium

Biography
Johan Dekoster received the M.S. degree in Exact Sciences (Physics) in 1988 from the KU Leuven, Belgium. In 1993 he received the Ph.D. degree (Physics), also from the KU Leuven. From 1993 till 1999 he held postdoctoral fellowships from the Research Council and the Fund for Scientific Research at the Institute of Nuclear and Radiation Physics of the KU Leuven. In 1999 he joined the OTN business unit of Siemens. He was project leader for several hardware firmware development projects for data, voice, video and LAN. In 2007 he became program manager OTN at Nokia Siemens Networks. In April 2008 he joined imec as R&D manager of the Epitaxy group with responsibility on epitaxial deposition of group IV and III-V semiconductor materials. Since November 2012 he is program manager for equipment and materials suppliers collaborations at imec.

Advancing Atomic Layer Deposition and Atomic Layer Etching

H. Knoops
Atomic Scale Segment Specialist
Oxford Instruments Plasma Technology, Bristol, United Kingdom

Abstract
Atomic scale processes such as atomic layer deposition (ALD) and atomic layer etching (ALE) are increasing in popularity with more and more applications requiring or benefitting from atomic level control. ALD and ALE provide the control they do because they are based on self-limiting surface processes. This contribution will discuss the basics for both techniques and discuss how they can be further advanced.

For ALD two trends will be discussed: i) controlling the ion energy in plasma ALD to tune material properties. Generally processes are optimized to have minimal ion energies to avoid potential damage. Interestingly, for these low damage plasma sources, the ion energy can be increased by substrate biasing providing additional knobs for tuning film properties. Key examples are stress-control of oxides such as achieving near-zero stress in TiO_2 and reduction of the resistivity of conductive nitrides (e.g. for TiN, HfN_x, and NbN). ii) Usage of novel plasma gases. For instance H_2S plasma gas mixtures have been shown to allow growth of 2D-MoS_2 at low temperatures and SF_6 plasma was found to allow ALD of AlF_3, which could be of interest as an optical coating or for batteries.

For ALE the basics will be discussed and how these can be used for applications. More and more processes are being developed (e.g. ALE of GaN, AlGaN, Si, SiO_2 & 2D materials). Interestingly besides the exact control of etch depth, other aspects of ALE might turn out to be more important for certain applications. For instance ALE of AlGaN was found to reduce the surface roughness, while generally plasma etching would increase the surface roughness somewhat. Other advances for both ALD and ALE are expected to be in the form of combinations with other techniques. Therefore clustering of ALD and ALE tools with 2D materials growth can allow precise control of interfaces and allow avenues into selective growth, surface cleaning and etching.

Biography

Dr.ir. Harm Knoops is an Atomic Scale Segment Specialist for Oxford Instruments Plasma Technology (OIPT) and holds a part-time assistant professorship position at the Eindhoven University of Technology. His work covers the fields of (plasma-based) synthesis of thin films, advanced diagnostics and understanding and developing plasma ALD and similar techniques. His main goals are to improve and advance ALD processes and applications for Oxford Instruments and its customers. He has authored and co-authored more than 40 technical papers in peer-reviewed journals.

Atomic layer deposition for the synthesis and integration of 2D materials for nanoelectronics

A. A. Bol
Associate Professor
Eindhoven University of Technology, Applied Physics, Eindhoven, Netherlands

Abstract
Graphene and other layered 2D materials have been the focus of intense research in the last decade due to their unique physical and chemical properties. This presentation will highlight our recent progress on the synthesis and integration of 2D materials for nanoelectronics applications using atomic layer deposition (ALD). ALD is a chemical process that is based on self-limiting surface reactions and results in ultrathin films, with sub-nm control over the thickness and wafer-scale uniformity. Two of the critical issues in unlocking the potential of graphene are the ability to deposit ultra-thin high-K dielectrics on grapene and fabricate low resistance contacts to graphene. Technologically, it is desirable to use atomic layer deposition (ALD) for this purpose. The inert nature of graphene however has made ALD on graphene very challenging. This presentation will give an overview of ALD techniques that were developed in our lab to initiate oxide and metal ALD on graphene to form ultrathin dielectrics and low-resistance contacts, without deteriorating graphene's electrical properties.
In addition, ALD might prove as a key enabler for tackling the current challenge of large-area growth of 2-D materials with wafer level uniformity and digital thickness controllability. We have implemented plasma-enhanced ALD to synthesize large-area MoS2 thin films with tuneable morphologies i.e. in-plane and vertically standing nano-scale architectures on CMOS compatible SiO2/Si substrates. The large scale 2D in-plane morphology has potential applications in nanoelectronics, while the 3D nanofin structures could be ideal for catalysis applications such as water splitting.

Biography
Ageeth Bol is associate professor of Applied Physics at Eindhoven University of Technology, the Netherlands. She received her MSc and PhD in Chemistry from Utrecht University, the Netherlands. After obtaining her PhD degree in 2001 she worked for Philips Electronics and at the IBM TJ Watson Research Center in the USA. In 2011 she joined the faculty of Eindhoven University of Technology. In 2012 she received a prestigious VIDI grant from the NWO (Netherlands Organization for Scientific Research) and in 2015 she was awarded a Consolidator Grant by the ERC (European Research Council). Her current research interests include the fabrication, modification and integration of 1-D and 2-D nanomaterials for nanodevice applications and catalysis.

Innovative Compound Semiconductor Based Engineered Substrates for Photonics, Power, Solar and RF Applications

E. Guiot
Product Development Manager
Soitec, Bernin, France

Abstract
The Smart Cut ™ technology applied to the fabrication of SOI, is used in volume manufacturing by SOITEC, serving digital, RF, power and photonics markets. Application of this technology using ion implantation to transfer thin films of compounds semiconductors has also been developed. The Smart Cut ™ process has technical and economical advantages. Transfer of thin layers onto many various materials with both a good thickness homogeneity and a high crystalline quality has been demonstrated. From an economic point of view, the possibility of reusing the remainder of the implanted substrate helps to reduce costs, especially for the III-V materials. We will focus on the application of the Smart Cut ™ technology for two different materials, InP and GaN.
InP is widely used for the optoelectronic market. The Smart Cut ™ technology, has been tuned to this material. In addition to the cost advantage of the recycling, different receiver substrates such as GaAs, Sapphire or Si have been evaluated to enable new functions: receiver lift off, lower fragility, better integration. Using the InP-on-GaAs engineered substrate combined with direct wafer bonding, Soitec together with Fraunhofer ISE and CEA Leti have demonstrated wafer bonded 4-junction solar cells with highest conversion efficiency of 46.1 %. We will discuss also how the Smart Cut™ technology can enable the use of InP for RF 5G products.
Regarding GaN, Smart Cut ™ technology enables the layer transfer of up to 1 µm thick GaN films either from bulk GaN or GaN on sapphire. We have demonstrated up to 3 cycles of reuse of the GaN donor substrate. Different receiver substrates such as Sapphire, Molybdenum and polycrystalline Aluminum Nitride have been evaluated. Through this innovative engineered GaN substrate, we have demonstrated a 20µm GaN epi growth. This breakthrough could enable new vertical GaN devices for high power application such as electric vehicle powertrain and RF power products serving the 5G market.

Biography
Dr. Eric Guiot, Materials Science Doctor (Ph.D. from Paris University, Pierre et Marie Curie), now is product development manager for compound semiconductors in Soitec. He is graduated from the Ecole Centrale engineering school in France. He made his PhD on the development of epitaxy of iron oxide targeting giant magnetoresistance materials. He then joined Corning Fontainebleau Research Center in France for the development of integrated optics devices for telecommunication. In 2002 he joined Soitec in France. He has been working on the development of advanced engineered substrates targeting various applications covering digital application at advanced nodes and optoelectronics. He is now leading the product development group focused on compound semiconductor engineered substrates targeting power, solar, photonics and RF application.