Advanced Packaging Conference

S. Kroehnert
Senior Director Technology Development
Amkor Technology Holding B.V., Germany,
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Biography
Steffen Kroehnert is Senior Director Technology Development at Amkor Technology, Business Development Europe. Before the acquisition of NANIUM by Amkor Technology in May 2017, he worked for 20 years in different R&D and management positions at Siemens Semiconductors, Infineon Technologies, Qimonda and NANIUM in Germany and Portugal. Steffen is active member of several technical and conference committees of IEEE EPS, IMAPS, SMTA and SEMI. Since begin of 2016 he is chair of the European SEMI integrated Packaging, Assembly and Test (ESiPAT) Special Interest Group. Steffen is author and co-author of 23 patent filings and many technical papers in the field of Packaging Technology. He received his Master of Science degree in Electrical Engineering and Microsystems Technologies from the Technical University of Chemnitz, Germany, in 1997.

Advanced Packaging Developments—Where Are We Going?

J. Vardaman
President and Founder
TechSearch International, Inc., xxx, United States

Abstract
The semiconductor industry packaging and assembly business continues many changes. The smart factory is the new industrial revolution, driving sensors, machine-to-machine communication, as well as data storage and analysis. The adoption of 5G and ADAS changes the package designs and materials. Growing demand for datacenters and artificial intelligence or machine learning is pushing us to the next semiconductor nodes at a faster rate. The adoption of the next advanced semiconductor nodes will present challenges that must be met with new package developments. In addition, the next 10 years is likely to see new drivers for advanced packaging. This presentation describes some of the applications and the challenges for advanced packaging.

Biography
Jan Vardaman is the President and Founder of TechSearch International,Inc., which has been providing licensing and consulting services in semiconductor packaging since 1987. She is co-author of Nikkan Kogyo's How to Make IC Packages (in Japanese), a columnist with Circuits Assembly Magazine, and the author of numerous publications on emerging trends in semiconductor packaging and assembly. She is a member of IEEE CPMT, IMAPS, MEPTEC, and SEMI.

SEMI Standards: Update on Fan-Out Panel Level Packaging Standardization

J. Amano
Sr Director, Int'l Standards
SEMI, Standards, Milpitas, United States

Abstract
Fan-Out Panel Level Packaging (FO-PLP) technology is an enhanced packaging technology, embedding die in a low-cost substrate which is patterned to allow higher density of IOs than would otherwise be supported by the chip size.

A number of different formats – including circular and rectangular – have been proposed for the panels into which the die are embedded, with a large number of different rectangular sizes. This wide range is delaying broad acceptance of FO-PLP technologies, as the tools must be customized for each different format.

Panel substrates today range from 300 mm to 920 mm. Cost advantages depend on package and substrate size, and lack of standardization is a barrier to high volume manufacturing.

Despite its advantages, fan-out packaging has challenges to overcome. To address these issues, the SEMI Standards Fan-Out Panel Level Packaging Task Force is currently developing standards focusing on panels, targeting dimensions, ID marking and orientation, edge exclusion, and other parameters such as total thickness variation (TTV), bow, and warp.

Created in 1973, the SEMI International Standards Program brings together industry experts to exchange ideas and work towards developing globally accepted technical standards. SEMI provides the forum for the essential collaborations that must be achieved to move new and existing markets forward efficiently and profitably.

Biography
James Amano has led the SEMI International Standards Program since 2008. Prior to joining SEMI, he worked as the Silicon Valley sales engineer for Matsusada Precision, and as a trade specialist for the Japan External Trade Organization (JETRO). He holds degrees in Economics and Environmental Conservation from the University of Colorado at Boulder.

Optimising Surface Chemistry After Plasma Dicing (SPTS Technologies & Versum Materials US, LLC)

J. Hopkins
Etch Applications Manager
SPTS Technologies Ltd, Newport, United Kingdom

Abstract

Authors: J. Hopkins, O. Ansell, R. Barnett (SPTS Technologies) & M. Phenis, D. Pfettscher, R. Peters, M. Sistern (Versum Materials US, LLC)

Plasma dicing has shown many benefits over other dicing techniques such as increased die strength, smaller/thinner die and reduced cost of ownership.
This dicing process uses the established Bosch Process, with alternating etch and deposition steps to etch through the silicon wafer. The nature of the process means that there will be F residues remaining at completion due to the CF_x polymer layer deposited on the wafer surfaces[1]. This can be removed by an O_2 plasma however when solder bumps are present and subjected to the same dicing/Bosch process, the bumps can react with F radicals to form SnF_2 which cannot be removed by an O_2 plasma alone. An additional plasma process can be performed to reduce the F levels further, however, this still leaves F present. Studies are underway to determine whether this is an issue for subsequent steps or indeed whether the presence of F may help solderability[2]. However, in this work, the effectiveness of post-dicing wet cleans to remove the SnF_2, and avoid any potential issues, is investigated.
Tests were carried out comparing plasma DAG (dicing after grind) processes with different post residue treatments. A screening test was carried out using several different wet etch formulations, and two suitable formulations were identified. Further tests were carried out to optimise the conditions and check the tape compatibility. The F levels, measured by EDX, were reduced to <1% at a level comparable to the control sample (with no plasma dicing).
The work has shown that a wet chemistry post plasma dicing treatment is capable of removing F residues and is compatible with the plasma dicing process flow.

References

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2. Hosoda et al, Proceedings of ECO design 2003, Tokyo, Japan, December 8-11, 2003, p 710-713

Biography

Janet Hopkins is the Etch Applications Manager at SPTS Technologies, currently focusing on plasma dicing.
Janet joined the company in 1995, as Process Engineer in the Si etch group. During her career, she has worked in developing different plasma sources and processes, including early commercialisation of the Bosch Process for deep silicon etching of MEMS. She is the author of many papers and patents.
She holds a BSc in Physics and Chemistry of Materials from The University of Durham and a PhD in Plasma Surface Modification.

Solutions for thin and tiny dies with high die strength and for thinning WLCSP and eWLB wafers

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DISCO HI-TEC EUROPE, Sales Department,
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Abstract
DISCO Corporation is a leading manufacturer for equipment and tools for wafer thinning/dicing. “Bringing science to comfortable living by Kiru (Dicing), Kezuru (Grinding) and Migaku (Polishing)” is DISCO’s mission. By combining these three core technologies, DISCO provides total solutions to meet the demanding requirements of the Semiconductor industry in terms of manufacturing thin dies with high die-strength and several new approaches for advanced packaging.

A wide range of devices tend to have narrow street widths (cut margins), partially covered with low-k or ultra low-k layers in order to maximize the number of dies formed on a wafer. Furthermore, mobile and IoT consumer products incorporate an ever-increasing number of such circuit components. Quality requirements of consumer products are heading for same level as automotive products or even exceed those.

In order to fulfil all these requirements, DISCO proposes several solutions focusing on avoidance of side wall cracks and interfacial layer damages.

DISCO will update on latest status of Stealth Dicing, high quality laser grooving, multi beam ablation laser cutting, dicing wafers with the active side facing to the tape, applying plasma dicing and remote plasma as well as combinations of these technologies in one process flow.

WLCSP and eWLB applications are facing issues in wafer thinning, as the wafers, due to consisting of resin mold and Silicon dies while having high bumps on the front side, tend to easily break when thickness becomes lower than the bump height. Nevertheless, such low thickness is required due to increasing bump thickness.
DISCO offers a unique technology to grind wafers with 200 µm high bumps down to 50 µm wafer thickness.

DISCO HI-TEC EUROPE GmbH, having its facilities close to Munich airport, offers certified Dicing and Grinding Production Services, so that customers can utilize most of the afore mentioned DISCO technologies in production, even without investing into DISCO equipment.

Biography
Gerald Klug

Biography

Gerald Klug studied business engineering at the University of Siegen and graduated in 1998 as Dipl.-Wirt.-Ing., completing his thesis at BMW in Munich. He started his career as a designer of coil processing lines for nearly 3 years at a German machine manufacturing company, Heinrich Georg GmbH. At the end of 2000, he joined DISCO as a Sales Engineer for the area of Scandinavia. Meanwhile he has been almost 18 years at DISCO, nowadays operating as General Sales Manager for the whole of Europe

Impact of Plasma Dicing Singulation Techniques on Die Breakage Strength and Robustness

D. Parker
Project Manager
ST Microelectronics, Back-end Manufacturing & Technology R&D, Rousset, France

Abstract
For all end applications where a semiconductor device is used, there is a constant demand for improved performance under all environmental conditions. One such application, which we all use regularly, is the smartcard chip. This secure microcontroller can be found predominantly in our bank or travel cards and passports, where it may receive much physical punishment in normal usage. The demands for severe robustness criteria for these card-based applications are continually increasing to ensure that the packaged chips are able to withstand more rigorous treatment without breaking.
Key to achieving these exacting standards is the singulation of the chips in a way that does not generate any inherent mechanical weakness. The standard blade sawing process has so far met existing requirements but the technology roadmap for such devices has presented new challenges with the deployment of fragile ultra-low k BEOL dielectrics. This has prompted the introduction of laser grooving before dicing to minimise damage to these materials caused by the sawing blade but this, in combination with mechanical dicing can itself cause weakening of the die and a higher risk of failure.
This paper will examine the relationship between die strength and some new approaches to die singulation with a strong focus on plasma dicing, in which die separation is achieved by etching the silicon in the scribe lane. As there is no mechanical element we should expect significant improvements in die strength so we will explore the inherent performance with this method as the etching output parameters and masking steps are varied. Additionally, this technique requires that the silicon is exposed in the scribe street, which must be free of metals and dielectrics before etching. Again laser grooving can be used to meet these conditions and we will describe how sequential laser grooving and plasma etch processes affect the die strength and reliability performance versus the more severe test criteria.

Biography
Mr Parker graduated in Chemistry from The University of Manchester, UK in 1981. Since the start of his career in semiconductors with Inmos Ltd the following year he has spent over 30 years with ST Microelectronics both in Agrate, Italy and Rousset, France.
Beginning as a process engineer, mainly in deposition and patterning, he has extensive experience of front-end operations, including device engineering, process integration and technology transfer. In recent years he has taken on a project management role to lead ST's interests in plasma dicing within the Back-end Manufacturing and Technology R&D team that is based in Grenoble.

H. Pristauz
Vice President, Technical Development Advanced Technology DA
Besi, Radfeld, Austria

Biography

Dr. Hugo Pristauz is VP at Besi for technology development and has about 20 years of experience in advanced die attach equipment area, both in R&D and business positions.
He started his semiconductor carrier by joining Datacon in 1999, where he was majorly assigned to product management and development of the successful 8800 advanced die attach platform.
After acquisition of Datacon by Besi in 2005 Hugo Pristauz was running emerging die attach business in VP position like RFID, flip-chip, thermo-compression and fan-out bonder business.
Since begin of 2016 Hugo Pristauz is focusing on technology scouting and networking to support Besi's roadmapping process.

Acceleration in packaging development through 5G and mmWave applications

C. Goetze
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Abstract
The next network generation will enable high bandwidth applications like Ultra HD videos for mobile devices and at the same time support wireless Virtual Reality (VR) gears. Smart city and smart home applications are requiring a high flexibility in integration of different devices into the network. IoT and wearables are less demanding in terms of data rate, but mean a tremendous increase of connected devices and at the same time a strong demand for super low power. Beside these applications, advanced health care, connected cars and autonomous driving are emerging. These mission (?) critical applications are requiring a high data rate together with the absolute reliability of the systems.
GLOBALFOUNDRIES' new 22FDX-mmw technology is targeted to serve ultra low power, digital data processing and analog IP integration and allows system architects to design IP into one single SoCs. To package these mixed signal SoCs, our industry is facing complex challenges by a high number of digital I/Os, sophisticated power and ground networks and highly sensitive RF signal routing. The packaging integration of millimeter Wave, in combination with high frequency antennas needs new levels of chip-package-co-design and thorough usage of advanced packaging materials.
In this presentation, we will show the challenges associated with mmWave based mobile networks, packaging solutions that can be adopted and how the design flow can improve system integration and overall performance.

Biography
Christian Goetze is Member of Technical Staff in the global Packaging Technology Integration group at GLOBALFOUNDRIES, based in Dresden, Germany. He is leading several RF-packaging development projects for 5G, mmWave and IoT applications incorporating advanced silicon technology nodes such as 45RFSOI, 28nm and 22FDx. In this role Goetze is the main interface to RnD institutes and supports lead customers in the network industry in product enablement.
Christian Goetze joined Globalfoundries in 2010 and managed multiple packaging development and qualification programs with close collaboration to global Assembly and Test houses.
Prior to joining Globalfoundries, Goetze worked as process and integration engineer at NOKIA-SIEMENS-Networks, Qimonda and Infineon. In these positions he worked on the second level assembly process development and optimization for memory modules and communication boards.
Christian Goetze received a Master of Science degree in Electrical Engineering from the Dresden University of Technology, Germany. In his Master's work, a cooperation of TU Dresden and SIEMENS, he studied the interfaces in Pb-free second level interconnects and their influence to the board level reliability.

Advanced Packaging Solution for High Performance Computing and AI

Y.-p. Wang
Sr. Director
SPIL, Taichung city, Taiwan

Abstract
For years the IC industry has been driven by the demand of Smartphone and tablet. IoT was most expected as the next growth engine but all of sudden, high performance computing (HPC) and AI have emerged as the major driving forces thanks to the booming of crypto-currency mining and both cloud computing and edge computing.
There are assembly challenges for HPC and AI, first of all, to achieve high computing performance, the logic IC is bigger and generates high thermal dissipation. And the bigger the die size, the lower the manufacturing yield rate. Secondly, the interconnection between logic IC and the memory needs to be very quick so it won't slow down overall system performance. Finally, a variety of SiP are required to realize AIoT (AI of Things)
To properly address those assembly challenges, a variety of advanced packaging solution are in development. For high power consumption, advanced silicon node is applied for large FCBGA to save the power, and advanced thermal interface material (TIM) with higher thermal conductivity is in development for more thermal dissipation. Furthermore, one big IC can be redesigned as several identical smaller ones with higher manufacturing yield rate, and by utilizing 2.5DIC technology, an interposer with fine lines is introduced for homogeneous integration. As for heterogeneous integration between logic IC and the memory, they are packaged together with 2.5DIC technology or Fan-Out MCM based on fine line requirement for faster interconnection. As for SiP, not only for small form factor, but also better EMI and antenna in SiP are in development for better and faster wireless communication.
In this paper, technical risks of each advanced packaging solutions mentioned are reviewed, and possible actions of each risk are explored. And with the ready of these advanced packaging solutions, HPC and AI are off and running.

Biography
Dr. Yu-Po Wang
Director
CRD Center
SPIL

Education:
Ph.D., Mechanical Engineering, State University of New York at Binghamton, New York, U.S.A.

Experience:

1997-1998 Gintic Institute of Manufacturing Technology, Singapore
1998-Present SPIL, Taiwan

Collective Die Bonding Technologies for Heterogeneous Integration in Advanced Packaging

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Business Develoment Director
EV Group, St. Florian am Inn, Austria

Abstract
As die area is constantly reduced especially for small package sizes and heterogeneous integration with high interconnect density becomes crucial. For large packages sizes heterogeneous integration and die segmentation gets an increasing role of processing applications. Here, heterogeneous integration leads to an overall increased yield, mainly as smaller dies generally can be produced with higher yield. In the same time and most importantly, memory, processors, sensors and such from different sources can be combined using heterogeneous integration. Aforementioned yield improvements by splitting dies into several parts and improving the performance cost.
Combining the segmented dies in an advanced package can be done by two different bonding technologies, namely sequential die bonding or a collective die bonding approach. For the collective bonding, individual dies are populated and tacked either on an interposer or a so-called handling carrier, depending on the bonding technology applied. In case of tacking die face-down on an interposer or other active silicon die, bonding is usually being done by thermal bonding. Here, heating and cooling of the substrates are only done once, considerably reducing process cost and thermal budget of the underlying substrate. The second case is tacking the dies face up on a carrier substrate. This reconstructed dies on a carrier can now be processes again on wafer scale, this means preprocessing steps such as direct bonding can be done before bonding the wafers using fusion or hybrid bonding.
In this presentation we will show different integration approaches for collective die bonding for both thermal bonding as well as fusion / hybrid bonding. For both processes, results in terms of die placement and sequential alignment accuracy of the integrated process will be compared and discussed, together with current and potential applications of these processes for future devices.

Biography
Dr. Thomas Uhrmann is director of business development at EV Group (EVG) where he is responsible for overseeing all aspects of EVG’s worldwide business development. Specifically, he is focused on 3D integration, MEMS, LEDs and a number of emerging markets.
Prior to this role, Uhrmann was business development manager for 3D and Advanced Packaging as well as Compound Semiconductors and Si-based Power Devices at EV Group. He holds an engineering degree in mechatronics from the University of Applied Sciences in Regensburg and a PhD in semiconductor physics from Vienna University of Technology.

Two side molded WLCSP

T. Kamphuis
Assembly Industrialization Manager
NXP, Package Innovation, Nijmegen, Netherlands

Abstract
Increasingly WLCSP are used as solution for packaging, especially when the area needed for I/O matches the area needed for the function. Industry trend is to go thinner devices and smaller pitches. The mechanical integrity of WLCSP's is stressed not only in the application, but also during board assembly at the customer.
The breakthrough technology presented provides protection for both the top and bottom of the product, thus protecting the 8 corners of the device during handling at manufacturing and customer. Different material sets and molding technologies for encapsulation of the WLCSP were investigated, each with their own merits. The challenges experienced to create the two side encapsulated concept and way forward to overcome them will be shared. First results on Board Level Reliability will be shared.
The encapsulation concept to achieve full encapsulation is demonstrated at supplier site and the building blocks towards a true industrial solution is shared. Balancing the front and back side thickness of the compound enables reduction of the overall height while at the same time improve the BLR performance compared to more well-known 5 side protected WLCSP in the same package thickness.

Biography
Tonny Kamphuis received his master in Mechanical Engineering at Twente University in 1986. The same year he joined Philips Semiconductors in the field of IC assembly equipment. He worked in Kaohsiung Taiwan from 1991 to 1992, after which he joined the discrete assembly equipment development department in Nijmegen. He has developed die bonders, wire bonders, molding machines as well as all type of handling equipment for both reel to reel and strip to strip based industrializations. Since the year 2000 he is focusing on assembly process development and industrialization for IC again. In 2007 NXP was founded, at NXP, he has filed several patents related to wafer processing, package concepts and process improvements.

Advanced substrates for MEMS and photonic applications

V.-P. Lempinen
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Abstract
Requirements for lower cost and higher volumes are driving towards miniaturization of MEMS and photonic devices. Requirements for reliability and performance improvements on the other hand drive for improvements in precision of BSOI materials, and use of hermetically sealed structures enabled by Cavity SOI (C-SOI) wafers or wafer level packaging. Following examples of advanced substrate-based solutions are shown and discussed:

• Use of thick SOI or C-SOI for manufacturing released MEMS structures. Comparison of different SOI substrates from process integration and manufacturing complexity point of view. Benefits of SOI and C-SOI based approach for flatness and dimensional precision of the released structures.
• Combination of C-SOI based MEMS and wafer level packaging by patterned capping wafers with poly Si TSVs. Properties of advanced C-SOI and TSV substrates.
• C-SOI based approach for high performance inertial sensors, with benefits in process integration, reliability and performance optimization.
• Thick SOI based optical waveguides using E-SOI substrates for maximum efficiency.

Okmetic's new turnkey solution of providing full C-SOI process flow, from silicon crystal growth to cavity patterning and SOI wafer manufacturing, from one source is introduced. Fully in-house C-SOI processing allows an industrial-scale solution to C-SOI manufacturing, and enables the sensor manufacturers to focus on their core competencies in the directly sensing-related parts of the manufacturing process. Integrating the reliability-critical fusion bonding part of the MEMS process as a part of starting wafer manufacturing enables also streamlining of the manufacturing process flow, simplified process integration, and improved long- term reliability of the MEMS devices. In-house crystal growth and substrate wafer manufacturing enable full customization of material properties, such as Si layer resistivity and orientation, of each layer of the C-SOI structure.

Biography
Mr. Lempinen received his M.Sc. in Materials Physics from Helsinki University of Technology in 1999. Mr. Lempinen has over 15 years of experience in Silicon based material engineering. He has worked for Okmetic since 2000 and held various positions related to R&D, process engineering and applications support. Currently he is working as Senior Manager, Customer Support being responsible for the company's global technical customer support organization. Prior to his time at Okmetic, Lempinen was involved in photovoltaic research in Electron Physics laboratory of Helsinki University of Technology, Finland and Microelectronics Research Center of Iowa state University, U.S.A.

New automatic transient thermal analysis equipment to inspect the quality of sintered interconnects

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Scientific Research Assistant
Technische Hochschule Ingolstadt, IIMo,
Ingolstadt, Germany

Abstract
The ability to test the quality and reliability of interconnects of semiconductor packages conclusively through non-destructive tests gains importance with increased requirements. Sintered interconnects depend critically on the surface quality of the contact pads and metallic sinter particles. Unstable chemistry of the paste can also cause failures. While X-Ray or acoustic microscopy hardly detect these, thermal methods are sensitive to identify these failures.
By TTA measurements the transient thermal impedance Zth is obtained and the thermal resistance Rth is calculated as per JEDEC51-14. But the measurement and data evaluation is time consuming and often requires experts. The relative thermal resistance measurement method is applied in the paper using the automatic tester to evaluate the thermal path and the thermal resistance, wherein the sensitivity and thermal load are not measured but are obtained by thermal path normalization to good samples whose values are known.
LEDs are sintered on substrates, measured initially (0-hour quality) and subsequently after hours/cycles of accelerated stress testing (reliability) using the automated TTA tester. The measurement electronics are mounted on a movable 3-axis system to enable use of short cables with low parasitic inductance. To resolve the thermal resistance between the LED die and substrate the forward voltage of the LEDs after current switching needs to be measured well below 10µs. The developed current source allows very fast switching within 100ns and stabilize the detection current within 5µs. In addition an In-Situ tester measures thermal impedance providing additional data to support analysis.
In this paper automated TTA test equipment and In-Situ tester are presented which enable to measure the transient thermal impedance and by that identify the thermal integrity of the interconnect after assembly and within accelerated reliability tests. By known good reference samples failures are automatically identified.

Biography
Sri Krishna Bhogaraju
Scientifc Research Assistant - IIMo - Technische Hochschule Ingolstadt

Education:
2010-2012 - Master of Engineering - International Automotive Engineering, University of Applied Sciences, Ingolstadt, Germany.
2006-2010 - Bachelor of Engineering - Mechanical Engineering, University Visvesvaraya College of Engineering, Bangalore University, Bangalore, India.

Work Experience:
Jan 2018* - Scientific Research Assistant - IIMo - Technische Hochschule Ingolstadt.
Feb 2016 - Dec 2017 - Process Design Specialist - Corporate Rules & Standards, Corporate Quality & Environment, Continental AG, Hannover, Germany.
Apr 2014 - Jan 2016 - Project Co-Ordinator & On-Site specialist - ContiTech Power Transmission (Sanmen) Ltd., Sanmen, P.R.China.

Nov 2013 - Mar 2014 - Project Co-Ordinator - Roulunds Rubber Korea Co. Ltd., Busan, South Korea.
Oct 2012 - Oct 2013 - Project Co-Ordinator - ContiTech Power Transmission Ltd., Sonepat, India.
Mar 2012 - Sept 2012 - Product Manager - Asia - ContiTech Fluid Shanghai Co. Ltd.

P. Cockburn
Senior Product Manager - TCI
Xcerra Corporation, TCI, Verwood, United Kingdom

Biography
Peter Cockburn has worked in the ATE industry for over 28 years at Schlumberger, NPTest, Credence, LTX-Credence and now Xcerra.
After developing real-time and GUI software for ATE systems, he moved into product marketing and launched several new SOC ATE systems and analog test options as well as providing marketing and sales support in USA, Asia and Europe.
As Senior Product Manager of the Test Cell Innovation team, he is now responsible for defining and delivering complete test cells to customers that reduce cost, increase uptime and improve quality when testing semiconductors including pressure and motion sensors, microphones and wafer-level packages.
He has an Engineering degree from the University of Southampton, UK.

MEMS Sensor Testing - Yesterday, Today and Tomorrow (an OSAT's perspective)

G. John
Sr Director Advanced Test
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Abstract
The concept of MEMS sensor testing has evolved from a fantasy to a reality over the last two decades. What was once considered impossible in high volume manufacture has now become mainstream in the industry. Initially, MEMS sensor devices were introduced as an alternative to bulky technologies, with lower performances than their predecessors. However, today's MEMS devices with proven reliability and performances have surpassed their predecessors and are competing with their high-cost and high-end counterparts. Examples of such MEMS sensor devices can be seen in the MEMS microphones whose early specifications started off as a simple audio transducer, now has morphed into high-fidelity MEMS device, competing with the high-end studio microphones.
Testing such “high-performance” MEMS sensor devices in high volumes at the lowest possible costs with little or no compromises calls for an innovative combination of test techniques and close cooperation between the OSAT and the MEMS design engineers, product engineers and the applications engineers. Areas that are often overlooked are, the form factor of the device under test, the use of test techniques that can provide a higher throughput than electrical testing and the final end application. The ability to include self-test and self-calibration structures into the design will reduce the test burden. The main challenge faced during MEMS sensor test is in the stimulus development, while the electrical testing can be easily accomplished by a low-end tester. When creating MEMS test specifications, a careful balance needs to be drawn between too much and too little test coverage.
This keynote focuses on the evolution, challenges, and opportunities for MEMS sensor testing spanning the yesterdays, today and will provide a vision for the future of lower cost MEMS sensor test.

Biography
Gerard joined Amkor in 2005, and has supported and managed hardware and software test development for a variety of Amkor packaging. He currently serves as an advanced test technical expert for MEMS, 2.5D, WLFO, HDFO, fine pitch probe and optical devices, supporting customers in the US and Europe. Prior to joining Amkor, Gerard worked in various semiconductor test positions for Conexant Systems, Flarion Technologies (acquired by Qualcomm) and Motorola. He holds a BA degree in electronics and telecommunications engineering from Osmania University and an MBA from Gainey School of Business in Michigan.

He holds multiple patents in the field of MEMS Test.

Reliability Investigation of Wafer Level Chip Scale packages under thermal cycling condition and validation using simulation methodology

B. Nandhivaram Muthuraman
Package & Material Simulation Engineer
Dialog Semiconductor GmbH, Stuttgart, Germany

Abstract
In this paper, reliability investigation of Large Wafer Level Chip Scale package of size 54 mm2 with different die thickness and underfill conditions is discussed. Test vehicles were constructed based on the design variation using different silicon chip/die thicknesses and different underfill conditions. To assess the device reliability, extensive Board Level Reliability Temperature Cycling Tests (BLR-TCT) were carried out with a temperature load variation between -40°C till +85°C until significant solder joint fatigue failures are observed. It is evaluated that the failure mode in underfill package is different than the package without underfill. Devices with no underfill showed solder joint bulk cracks under thermal cycling condition, whereas the devices with the underfill experienced cracks on the intermetallic layer between the silicon chip and redistribution copper layer. To investigate and validate BLR-TCT reliability measurement data, Finite Element Method (FEM) simulations were carried out. Parameters like Aluminium Pad thickness and the routing method of Redistribution layer – Aluminium pad interconnection is evaluated using numerical techniques. Significant parameters were investigated in the numerical simulation model to understand the effect of package structural variation on the failure mechanism shift observed in Board level reliability (BLR) measurement tests. Results from the numerical simulation study validate the failure modes observed in BLR temperature cycling tests. Large WLCSP devices with underfill experienced a higher delamination stress on the metal interface. After design optimization study, relevant solutions have been found and illustrated. This research work can serve as a guide towards reliability assessment involved in large-scale WLCSP packages and necessary stress reduction techniques to be implemented in such smart devices.

Biography
Balaji Nandhivaram Muthuraman is working as Packaging and Material Simulation engineer in Dialog Semiconductor GmbH, Germany. He obtained his Bachelor's degree in Aeronautical Engineering from Anna University, Chennai,India. Followed by, Master's degree in Computational Mechanics of Materials and Structures from University of Stuttgart, Germany. His current area of working interest are Board level reliability of electronic packages, Developing fatigue model for reliability assessment of Dialogs products.

Advanced package test solution for the automotive market

A. Waldauf
VP of Platfrom Engineering
Cohu, NPE, Rosenheim, Germany

Abstract
Consumer demand and competitive pressure have pushed automotive manufacturers to build greater intelligence into automobiles and trucks. For example, the Chevy Volt uses nearly 100 microprocessors running about 10 million lines of code in total, placing the Chevy Volt's software content close to that of the Boeing 787 Dreamliner. As with that electric vehicle, mainstream automotive design is increasingly relying on more sophisticated electronic systems.

Indeed, advances in automotive technology revolve around five key trend:
• Advanced Driver Assistance System (ADAS) and autonomous driving
• Advanced Motor Control
• Engine/Energy Management Systems
• Graphical Interfaces and entertainment
• Vehicle System of Systems in the Internet of Things

These growing trends require new advanced packages which had not been used to such an extent in harsh automotive environment in the past, e.g. combination of dedicated vision processors, multicore CPUs and vision software. For motor control new MCU and FPGA Solutions, for IOT, new combo MEMS, 5G for wireless external connectivity and extended bus systems for internal subsystem links.

Most of these developments were possible by integrating more and more functionality into one package and maintaining the stringent automotive safety and reliability requirements.

New Backend test and handling systems had to be developed to address the new package requirements to ensure robust functionality.

This breakthrough technology provides:
• the lowest CoT for High Volume Manufacturing
• Tri-temp for WLP, Fan-out and other small and mid-size packages including vision inspection
• Stimuli for Combo MEMS
• Fine pitch Kelvin contacting

Biography
Alexander J. Waldauf - Vice President of Platform Engineering
Alex Waldauf was one of the founders of Cohu's Rasco subsidiary in 1998 and has been Vice President of Platform Engineering since July 2017. Mr. Waldauf was Vice President and General Manager of Rasco since January 2011, previously responsible for the Test-In-Strip product line, Managing Director of Rasco and global Vice President of Sales and Service. Prior to founding Rasco, Mr. Waldauf spent 6 years at Multitest and held key positions in engineering.
Mr. Waldauf has a Mechanical Engineering degree from the Austrian School of Technology in Salzburg (HTL).

Interpretation and Application of Test Socket and Probe Head Specification

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Abstract
Decisions should be supported with verifiable and repeatable performance data. This is true when selecting contactors, test sockets, and probe heads for test. This intent of this paper is to describe and define the data used to specify contactors, test sockets, and probe heads for test. This includes the source methodology and process for developing the lab data describing the performance of contactors, test sockets, and probe heads for test. With this the paper will lead the way to interpret and apply the statistically predicted field performance of the test probe as qualified in a test lab.

Presented will be lab data describing the performance of several mainstream probe architectures for contacting Wafer Level Chip Scale Packages (WLCSP). The goal of this paper is to create a common understanding of how to read, interpret, and communicate data for selecting the right probe technology for WLCSP test applications.

The paper goes beyond the probes and speaks to other factors that contribute to the overall performance of the contactors, test sockets, and probe heads for test. For example, the probe head housing design and materials used are important aspects that need to be understood for optimized performance. The success of the data-driven probe selection approach is reliant upon the quality of the supplier data. The paper will describe the reports provided including the WLCSP Metrology reports.

Focus Content:
• Interconnect technologies for improved performance and reliability
• The role of material, and material development for higher reliability
• Metrology and inspection methods

Biography
Bert Brost
Biography

Bert is a Senior Product Manager for Xcerra Corporation. With more than 35 years of experience in backend test, Bert has held senior management positions with Johnstech International and Control Data Corporation. Bert started his career in engineering with Micro Component Technology (MCT) designing test electronics and later worked as an engineer for Sick Optik Elektronic GmbH. Bert holds several undergraduate degrees and a MBA from the University of St. Thomas, Minnesota.

Materials and Processes for 3D Heterogeneous Integration

G. Beyer
Program Manager
IMEC, 3001 Leuven, Belgium

Abstract
3D heterogeneous integration opens new paths for System On Chip (SOC) and System In Package (SIP) to integrate computing, storage, in and output and other functions in a system efficiently. As interconnect requirements between the various components differ in terms of bandwidth and energy per bit, 3D technologies need to provide different interconnect solutions within a system. In order to realize significant wire length savings of a partitioned processor, small interconnect pitches below 1µm are required. Connections to off-processor memory are longer and have wider pitches. In this presentation, the co-existence of these different 3D interconnect technologies and their need for new materials and integration solutions is discussed.

Biography
Gerald Beyer has been working in the field of 3D Technologies since 2012 as the technology program manager of the 3D System Integration Program of IMEC. Prior to this he was the interconnect program manager and group leader of BEOL integration. He received a PhD in materials science from Imperial College, London and a MSc from Thames Polytechnic, London.

Secure packaging for addressing hardware security challenges

J. Fournier
Senior scientist
CEA Leti, DSYS/SSSEC, Grenoble, France

Abstract
The advent of the IoT has put the device on the centerstage of security-related debates. Attacks on the device itself can have a severe impact on the provided services (e.g. attacks on the Philips Hue lamp). Conversely, the device can be an attack entry door for the entire system (e.g. the connected cameras used making a D-DoS on DNS servers). Protecting the device does not only mean that we need to protect the way the device is architectured, the way the embedded applications are implemented but also the way the device is manufactured and packaged.
In this presentation, we shall first introduce the underlying hardware security issues before focusing on physical attacks like reverse-engineering, side channel analysis and fault attacks. We shall then explain how some of those issues can be addressed with a secure packaging. We shall provide an overview of existing secure packaging technologies and conclude on the remaining challenges for innovative secure packaging solutions.

Biography
Dr Jacques Fournier is a Senior Scientific Advisor in embedded systems' security at the CEA Leti which he joined 2009. Prior to that, he held several technical positions in the Security Lab of smart card manufacturer Gemalto from 2001 to 2009. Jacques obtained his "Habilitation" from the University of Limoges (FR), a PhD from the University of Cambridge (UK), an MSECE from Georgia Tech (USA) and an engineering degree from the French Grande Ecole Supélec.

Innovative Adhesive Developments for Next Gen Sensing Modules

K. Wu
Product Development Manager
Henkel Electronic Materials, Product Development
Semiconductor Materials, Shanghai, China

Abstract
As electronics industry enters a new era of IoT devices, more and more sensing modules are becoming essential to make devices “smart” and "intelligent". Representative ones are camera modules, proximity and ambient light sensors, biometric (3D ID) sensors and MEMS devices. As signal sensing and processing become more advanced and demanding, the adhesives used need to meet more stringent requirements of process flexibility, application accuracy, adhesion strength, drop test and reliability. Henkel evolves together with leading sensing module makers by further developing specialized adhesives for them. For example, in camera modules, low temperature cure and low shrinkage are critical for active alignment and enabling ultra-high image quality. Hybrid resin and curative designs enable cure below 80°C while achieving ultra-low cure shrinkage and excellent adhesion to various substrates. A versatile chemistry toolbox - incl. epoxy, acrylate, silicone and hybrid resins - is used to develop new adhesives for MEMS with a wide modulus range (1 MPa up), stable modulus during operation and high toughness. Through catalyst selection, different UV and/or thermal cure mechanisms are entailed to enable different application processes with higher output. For each chemistry, the adhesive rheology must be tailored to fit challenging aspect ratios using needle dispensing, jetting, printing or laser assisted transfer. For image sensor, lid, cap and stiffener attach and grounding, various levels of electrical and/or thermal conductivity are incorporated by specially developed resin and filler systems. Finally, adhesive FILM is getting preferred over liquids due to advantages in bond line thickness control, tight keep-out zone, low warpage and low stress by low temperature cure, latent catalyst selection and B-stage processing. This presentation will give a clear overview of the sensor assembly challenges AND innovative adhesive solutions to enable Next Gen Sensing Module developments.

Biography
Kily Wu is Product Development Manager with Henkel Electronic Materials and based in Shanghai. His team is developing specialized Semiconductor Die Attach and Sensor Assembly adhesives. Kily has a Master degree in Chemistry with “Macromolecular Chemistry and Physics” as major.

Enhanced Mechanical Properties of Copper for Fan-Out Wafer Level Packaging Applications

R. Schmidt
R&D Manager, Semiconductor
Atotech Deutschland GmbH, Berlin, Germany

Abstract
Redistribution layers are essential to a variety of packaging technologies, as it is with more RDLs that I/O density is increased. Increasing the I/O count allows for more complex, high speed die to be packaged and supports improved reliability performance. Next generation devices for FOWLP require decreasing the RDL pitch down to 2x2µm.

Successful formation and plating of such fine features, however, pose a challenge for both suppliers and manufacturers, with the primary plating challenge being the simultaneous plating of ultra fine L/S, large Cu pads, and filling of microvias with a deposition rate that optimizes throughput. Additionally, the mechanical properties and impurity requirements for the Cu deposition become more difficult to control and optimize with sub 10µm L/S: 1) (large) optimum grain size, polygonal Cu crystal structure for high (ductility) mechanical strength and low resistivity which impacts electrical performance; 2) low internal stress for minimized wafer warpage and good adhesion – both of which impact yield; and 3) low organic co-deposition for minimized micro voiding.

Electroplating with standard Cu electrolytes results in micro voiding that amass after thermal cycle testing and may lead to failures or breakages in the Cu metal lines. To overcome this, the bath conditions, additives, and current density should be adjusted to optimize their influence on the deposit properties in terms of impurities and grain size. This paper will discuss how the mechanical properties of Cu can enable higher reliability, and will present plating results achieved with a new electrolyte.

Biography
For the past 6 years Ralf Schmidt has held various roles related to R&D at Atotech Deutschland GmbH, wherein he focused primarily on the development of innovative copper plating processes.
He was Team Manager for the central R&D team New Methods & Technologies and has recently assumed the role of R&D Manager Semiconductor Advanced Packaging.
He started at Atotech in 2011 in the central R&D team, where he focused on a variety of topics including additives for electrolytic and electroless Cu deposition as well as electrolytic and electroless Ni processes.
Ralf recieved his PhD in Chemistry at the Julius-Maximilian University of Würzburg, Germany, where he began his career as scientist for the synthesis of dyes for organic electronics.

High Performance Thermal Conductive Substrates for Power Module Packaging

S. Im
Global Segment Leader
DuPont, Electronics & Imaging, Wimington, United States

Abstract
Increased adoption of hybrid and electrical vehicles as well as renewable energy systems are driving the innovation in power module packaging. Thermal substrate, one of the major components of power modules, is not an exception, and technological advancements are necessary to meet increased reliability requirements.
Herein, we show that a high-performance power electronic substrate can be designed with newly developed highly thermally conductive polyimide film to address potential issues industry strives to solve.
The most widely used ceramic based substrates tend to degrade severely with prolonged thermal cycles, a typical requirement of EVs and HEVs, reducing the reliability and lifetime of the power electronic device. Also, common design of the power module requires many layers that adds thermal resistance at each bonding surface.
DuPont's new Temprion™ Organic Direct Bond Copper (ODBC) has been developed and designed to address aforementioned problems, increasing thermal durability and reliability as well as enabling system layer suppression.
Temprion™ ODBC's dielectric layer, Temprion™ DB film will absorb thermo-mechanical stress from the metals due to CTE mismatch, dramatically improving durability of the system. In addition, various kinds of metals including Cu and Al can be easily bonded to Temprion™ DB films through simple process. There are no thickness limitations on bonding metal sheets and metal attached at the bottom can be used as an integrated heat sink/baseplate.
This presentation will provide an overview of the power module market, highlighting current challenges and alternative solutions to address them.

Biography
Sejin has over 10 years of experience in the automotive and chemical industry in various disciplines including business planning and strategy, product management and engineering. Currently he works at DuPont with teams and partners to help the industry solve one of its biggest challenges – thermal management – with DuPont's latest technology.

Sejin holds a BSME from University of Wisconsin at Madison and an MBA from Kellogg School of Management at Northwestern University.