Innovation Showcase (pre-recorded)

Better Tool Qualification Decisions with Optimization

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Abstract
As process complexity increases and tool fleets grow more specialized, qualification management has become one of the most capacity-intensive and least-optimized planning problems in semiconductor manufacturing. Tools must be qualified for specific capabilities through dedicated tests that consume production capacity. Manual management is complex and often suboptimal resulting in over-qualification that wastes capacity, or under-qualification that creates bottlenecks and missed delivery targets. In collaboration with X-FAB, INFICON developed the Tool Qualification Optimizer (TQO) to address this problem through automated, optimization-driven decision making.
TQO automates three interconnected decisions: which tools should be qualified for which capabilities, how WIP should be distributed across available tools, and when qualifications should occur. It operates over a configurable multi-period planning horizon, carrying unprocessed demand forward across time buckets and adapting decisions as conditions evolve.
The optimization pipeline combines Linear Programming and Mixed-Integer Linear Programming in a multi-step approach: determining minimum tool counts per capability through workload balancing, making binary qualification decisions that account for qualification time costs and tool diversification requirements, and allocating WIP using priority-weighted optimization based on lot urgency and due-date proximity.
TQO is deployed in a production fab, integrating with the factory data warehouse to ingest tool states, WIP snapshots, and qualification expiration data automatically. Benchmarked against a qualify-all baseline, qualification reductions of 10 to 40% were observed, directly recovering capacity previously lost to unnecessary qualification runs. Consistent coverage also reduces excursion risk from lapsed qualification, protecting yield. Recommendations are generated in minutes, with consistent decision logic across shifts and operators.

Biography
Shima Azizi, Ph.D., is a Data Scientist at INFICON, where she develops advanced analytics and optimization solutions to improve operational performance and support data-driven decision-making in fabs. Over the past two years, she has focused on developing optimization-based products for semiconductor manufacturing, leveraging linear programming, mixed-integer programming, and metaheuristic approaches to automate and enhance fab operations and planning decisions.
Prior to joining INFICON, Dr. Azizi served as an Assistant Professor of Business Analytics at St. John's University, where she taught analytics courses and conducted research on developing advanced analytics solutions for real-world challenges. She earned her Ph.D. in Operations Management from Worcester Polytechnic Institute (WPI).
Her expertise spans operations research and data science, with applications in semiconductor manufacturing, healthcare, humanitarian operations, and sustainability. Dr. Azizi is passionate about translating complex fab challenges into practical solutions that help make semiconductor manufacturing more predictable, efficient, and productive.< div class="simple-translate-system-theme" id="simple-translate" >< div >< div class="simple-translate-button isShow" style="background-image: url("chrome-extension://cllnohpbfenopiakdcjmjcbaeapmkcdl/icons/512.png"); height: 22px; width: 22px; top: 38px; left: 0px;" > < div class="simple-translate-panel " style="width: 300px; height: 200px; top: 0px; left: 0px; font-size: 13px;" >< div class="simple-translate-result-wrapper" style="overflow: hidden;" >< div class="simple-translate-move" draggable="true" > < div class="simple-translate-result-contents" >< p class="simple-translate-result" dir="auto" ></p>< p class="simple-translate-candidate" dir="auto"

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References

Platform Based Design Technology Co-optimization using 3DEXPERIENCE PLATFORM

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Abstract

Design-to-Technology Co-Optimization (DTCO) is a critical strategy for maximizing the performance, power, and manufacturability of semiconductor devices as process nodes continue to shrink to Angstrom era. DTCO involves the simultaneous optimization of both the design and technology parameters, ensuring that the design is well-aligned with the limitations and opportunities of the manufacturing process. This approach addresses the challenges of advanced semiconductor nodes by leveraging process-specific insights, such as Design for Manufacturability, Design for Testability, and Design for Yield. A platform-based DTCO framework further enhances these benefits by providing a unified environment that connects process technology development, simulation with requirements and manufacturing. Accurate CMP simulations are critical elements for DTCO. In this paper we will show how Chemical Mechanical Planarization can be improved using simulation.This paper further illustrates how the entire CMP environment can be visualized, modeled, and simulated within a unified platform, the 3DEXPERIENCE platform. The platform enables sustainable business innovation with systems engineering approach that integrates requirements, design, simulation, and manufacturing on a single platform. By connecting all stages of the development process, it enhances collaboration, ensures traceability, and enables faster, more efficient product realization. The platform-based design technology co-optimization approach brings following values

1.Streamline BOM Management: implement strategies to efficiently manage and update Bills of Materials (logical, engineering, manufacturing, and process BOM), ensuring alignment with design changes and facilitating seamless integration with manufacturing processes

2.Accelerate Time-to-Market: through early-stage simulations and optimizations, reduce the risk of costly design iterations, thereby shortening development cycles and expediting product delivery

3.Enhance Design Robustness: utilize CMP modeling and simulation to predict and mitigate potential manufacturing defects such as dishing and erosion, ensuring that designs are resilient to process variations

4.Optimize Layout Efficiency: leverage DTCO principles to refine layout patterns, improving performance, power, and area (PPA) metrics while adhering to advanced process design rules.

By providing such platform for DTCO improves cooptimization efficiency and accelerates advances node design innovation.

Biography

Smriti is currently working as a Solution Experience Senior Manager for Semiconductor Industry (High-tech) with Dassault Systèmes leading solution strategy. Prior she was responsible for understanding, consolidating and driving semiconductor technical solutions. She develops new solutions and provide enablement worldwide for semiconductor customers. She has over 14 years of R&D experience working with different foundries ST Microelectronics, Altis Semiconductor, X-FAB and research lab like CEA –LETI and Lip6 (U.P.M.C.).She received her Doctoral (Ph.D) degree in Nanoelectronics and Nanotechnolgy from INP Grenoble (France) in 2013.

Manuel Joined Dassault Systèmes in 1986 and based in France. He is working as Semiconductor Industry Solution Experience Director. He brings over 35+ years of experience supporting Dassault Systèmes' global customers in high-tech and automotive markets.He held various positions of responsibility in the development of Dassault Systemes solutions dedicated to the Electronics and semiconductor industry. Since 2011, he's been in charge of the High Performance Semiconductor Solution Experience, dedicated to creating Virtual Twins of semiconductor devices.

References

PIXEurope Pilot Line Training: Advanced Skills in PIC manufacturing for Industry

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Abstract

Skills shortages remain a major barrier to innovation in photonics, particularly in the evolving field of Photonic Integrated Circuits (PICs). Addressing this challenge requires coordinated, structured approaches beyond isolated training efforts. This work presents the development of a comprehensive training programme, outlining its objectives, design principles, and early outcomes. The training programme is designed and delivered within PIXEurope, the first fully integrated, open-access PIC pilot line, which bridges the gap between laboratory prototyping and full-scale manufacturing. Targeting SMEs, start-ups, and industrial users, it delivers industry-aligned training in advanced PIC manufacturing, leveraging Pilot Line infrastructure and expertise. By focusing on training unique to pilot line technologies, it will complement existing initiatives in the field. Its objective is to equip users to become literate in the pilot line research, technologies, and processes and to enable them to translate and apply the skills and expertise in their own environments. The programme will be fully operational by summer 2028 and expected to engage 1000 users annually.

It is designed as a modular and expandable structure, with low access barriers being critical for its success. The programme offers training in PIC design, fabrication, packaging, testing, reliability, and equipment operation. These courses are delivered as stand-alone modules at introductory, advanced and specialised levels, allowing users to select courses aligned with their skills, needs, and interests.

One example of an advanced stand-alone module is hands-on training in micro-transfer printing, a key enabling technology for heterogeneous integration in next-generation PICs. Developed and delivered by Tyndall National Institute's in-house experts, this course offers the world's first hands-on training programme in this cutting-edge technology for heterogeneous integration. It provides training on the state-of-the-art equipment, processes and semiconductor materials that underpin micro-transfer printing. To date, 64 professionals have been trained, with consistent oversubscription reflecting strong demand within the PIC ecosystem. The course achieves a recommendation rate exceeding 90%, demonstrating the high quality of the training provided.

Biography

Elisabeth (Liz) Wintersteller is Training Manager in the Advanced Packaging Team at Tyndall National Institute, University College Cork. She has over a decade of experience designing and delivering large-scale STEM training programmes across universities and international research centres. Her expertise includes coordinating complex education initiatives at national, European, and global levels, with a strong focus on interdisciplinary, research-driven environments. Previously, she held project management roles in the Human Brain Project education programme and delivered training at EMBL. She also managed major photonics training programmes at IPIC. In her current role, she leads the training programme for PIXEurope, developing impactful activities aligned with advanced research and innovation needs.

References

AI-ready Subfab Infrastructure – A Foundation for Edge Intelligence and Energy-Optimized Subfab Operation

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Abstract
Semiconductor manufacturers face growing pressure to reduce emissions and energy consumption in the subfab while maintaining strict process stability and uptime. A major obstacle to deploying artificial intelligence (AI) in this environment is the lack of a unified, high-resolution data layer connecting process tools, vacuum systems and scrubbers. This presentation introduces a subfab control and monitoring platform implemented at a high-volume manufacturing site, where it is used as the backbone for future edge AI applications in energy and emissions optimization.

The case study follows the journey from initial deployment to AI-ready operation in a 300 mm fab with complex multi-chamber process tools and clustered scrubber systems. It explains how standardized interfaces between process tools and subfabequipment were established, which data (e.g. flows, status signals) are collected at high frequency, and how this information is synchronized and contextualized at the tool and chamber level. On this basis, the fab engineering team can now analyze process-gas usage and scrubber loading patterns across the tool base consistently, without changing existing production workflows.

Building on this foundation, the presentation highlights several AI use-cases for edge deployment. These range from learning typical exhaust and loading patterns to optimize the interaction between process tools, vacuum systems and scrubbers, to dynamically adapting operating parameters such as fuel-gas setpoints or post-combustion times within defined safety limits.

By positioning the subfab platform as an open enabler rather than a proprietary black box, both semiconductor manufacturers and subfab equipment suppliers gain a flexible environment to develop, validate, and scale AI-driven energy efficiency optimizations over time. This case study demonstrates how investing in AI-ready subfab infrastructure can translate into measurable reductions in fuel-gas consumption, emissions and unplanned downtime, supporting nature-positive production and enable energy efficiency optimization in real manufacturing conditions using AI.

Biography
Stefanie Hammer, General Manager of algorismic gmbh has 12 years of experience in technology, strategy and digital transformation. She holds a Bachelor’s degree in Digital Business & Innovation and focuses on digitalization, software management, digital business model development and international project management. In her work she builds bridges between business and technology to turn digital transformation into concrete results and measurable impact.

References

From Pilot-Line Readiness to Trusted Deployment: A Cloneable Manufacturing Blueprint for European Semiconductor Resilience

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Abstract

Europe's semiconductor ecosystem faces a deployment gap. RTOs and pilot lines are essential for developing new technologies, but many security-, safety- and long-lifecycle applications require something different: stable, auditable and repeatable manufacturing capacity at mature nodes, combined with advanced packaging, test and traceability.

This contribution presents the European Reference Fab concept as a non-commercial manufacturing blueprint to close that gap: a cloneable 300-mm infrastructure model for 130 nm with an optional evolution path to 65 nm, integrating front-end manufacturing, packaging, chiplet integration, test, open design enablement and auditable process and data flows.

The news is not another pilot line or a single national flagship fab. The proposed Reference Fab is an industrial deployment architecture. It defines how mature process modules, open PDKs/ADKs, documented tool flows, traceability mechanisms, MPW and small-series access, and packaging/test capabilities can be combined into a governed manufacturing environment. Clone sites could be implemented as front-end lines, assembly/test hubs or combined facilities, depending on regional and sectoral needs.

The concept addresses several bottlenecks in semiconductor adoption. First, it provides a trusted manufacturing route for defence, critical infrastructure, automotive, industrial, med-tech and aerospace applications that do not necessarily require leading-edge nodes but do require long-term availability, provenance and auditability. Second, it creates an industrial endpoint for RTO and pilot-line results, helping promising technologies move from readiness to deployment. Third, it lowers access barriers for SMEs, start-ups and system integrators through open design kits, harmonised design interfaces and fair MPW/small-series schemes. Fourth, it embeds smart-manufacturing principles such as MES-based traceability, inline metrology, SPC/ML-assisted control, documented audit trails and secure data flows from design through manufacturing and final test.

The presentation will outline the core architecture of the Reference Fab, the rationale for the 130 nm to 65 nm pathway, the role of packaging-first system integration, and the mechanisms by which open design enablement, auditable manufacturing and workforce development can support trusted electronics, supply-chain resilience and European semiconductor competitiveness.

Biography

Dr.-Ing. Norbert Herfurth is a research group leader, programme coordinator and semiconductor technologist with more than ten years of experience at the interface of microelectronics research, collaborative R&D programmes, open-source chip design, failure analysis and semiconductor strategy. He currently leads the Diagnostics, Sensors & Emerging Modules group at IHP – Leibniz Institute for High Performance Microelectronics in Frankfurt (Oder), Germany, where he is responsible for building and managing a newly established interdisciplinary unit with activities in diagnostics, sensors, photonic and emerging module technologies.

His work combines technical depth in semiconductor devices and failure analysis with strategic programme leadership. Before taking on his current group-leader role, he initiated, structured and coordinated several publicly funded collaborative R&D projects in the field of open-source microelectronics, open PDKs and trusted electronics. He has contributed to the development and positioning of Europe's open-source chip-design ecosystem, including work around IHP's open 130 nm PDK activities and European discussions on open-source EDA, design access and semiconductor sovereignty.

Norbert Herfurth earned his doctorate in electrical engineering from Technische Universität Berlin, where his research focused on semiconductor devices and silicon-level failure analysis. During his academic work, he operated and developed advanced diagnostic and failure-analysis methods, including photon-emission microscopy, thermal and optical techniques, probing methods and cleanroom-based experimental workflows. Since 2024, he has also been a lecturer at Technische Universität Berlin for the course "Debug of Integrated Circuits on Silicon Level", which combines IC debug, failure analysis and hands-on diagnostic methods.

In addition to his technical work, he has extensive experience in consortium building, project governance and strategic technology communication. He has led or coordinated multiple BMBF-funded collaborative projects, developed R&D work programmes, managed milestone- and review-driven project structures and worked with partners from research organisations, SMEs, industry, funding bodies and public-sector stakeholders. His current activities include the development of strategic concepts for open and trustworthy semiconductor ecosystems, especially where design enablement, manufacturing access, packaging, test, traceability and trusted electronics intersect.

Norbert Herfurth is one of the contributors to the European Reference Fab / Transparent Reference Fab concept, a proposed open, cloneable manufacturing blueprint for trustworthy mature-node semiconductor production in Europe. In this context, he focuses on the connection between open design enablement, auditable manufacturing, trusted electronics, chiplet-aware system integration and the transition from pilot-line readiness to industrial deployment. He is also a founding member of the VDE ITG expert group on trustworthy electronics.

His professional interest lies in translating complex semiconductor technology topics into actionable strategies for research, industry and policy stakeholders. This includes open PDKs and open EDA, trusted manufacturing, semiconductor resilience, system-level integration, failure analysis, photonic and electronic diagnostics, and the role of public-interest infrastructure in strengthening Europe's semiconductor ecosystem.

References

PFAS-free lubricants and greases for semiconductor manufacturing

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Abstract
Emerging PFAS regulations are threatening the availability of perfluorinated lubricant oils and greases used throughout semiconductor manufacturing equipment. If Europe intends to lead the world in transitioning away from PFAS chemistry, we must take action towards deploying alternative lubricant chemistries now, particularly considering qualification timelines and industry specific validation requirements for new lubricants.

This work showcases the development and production of ionic liquid lubricants and greases that offer a PFAS-free lubrication solution for demanding vacuum and ultra-clean environment applications. The new lubricants developed are not just "PFAS-free": they are silicon-free, halide-free, lihium-free, and fluorine-free. Third-party laboratory studies show that, when compared to state-of-art vacuum lubricants, they offer 10,000 times lower evaporation, up to 30 times the lifetime, up to 50% friction reduction in ball bearings, ball screws, and linear guides operated in a vacuum atmosphere and a remarkable level of surface protection.

This scalable and Europe-manufactured lubricant platform has been validated in vacuum-operated machine components, providing the European semiconductor industry with a practical pathway to replace PFAS-based lubricants while establishing leadership in next-generation high-performance lubrication for vacuum applications.

Biography
Dr. Román de la Presilla is the CEO and co-founder of Sverion AB, a Swedish deep-tech company developing next-generation ionic liquid lubricants for high-performance industrial applications, including the semiconductor, aerospace, and defense industries. He co-founded Sverion in 2024 to translate his research into commercial technologies, developing PFAS-free, high-efficiency lubrication solutions.
Román holds a PhD in Machine Design from KTH Royal Institute of Technology, where he maintains a research affiliation with the Department of Engineering Design. His work focuses on tribology, lubrication, and ionic materials for extreme operating conditions. He has authored numerous scientific publications and actively collaborates with academia and industry to accelerate the development and deployment of sustainable, high-performance lubrication technologies.

References