imec ITF - Building the silicon backbone of Europe’s AI leadership

Welcome Remarks

K. Marent
EVP & Chief Marketing and Communications Officer
imec, Berlin, Germany

Abstract
Welcome Remarks

Biography
Katrien Marent has an engineering degree in microelectronics. She joined imec in 1992 as analog design engineer and specialized in design of low-noise readout electronics for high-energy physics. In 1999, she became press responsible and scientific editor at imec's business development division and was responsible for authoring and editing the research organization's numerous company technical documents and publications. In 2001, she was appointed corporate communications director at imec. Her responsibilities expanded in August 2007, when she got the position of external communications director including corporate, marketing and outreach communications. In October 2016, she became VP corporate, marketing and outreach communication. Since April 2020 she is Executive Vice President & Chief Marketing and Communications Officer and member of the executive board of imec.

References

Orchestrating a scalable AI revolution

P. Vandenameele
CEO
imec, Berlin, Germany

Abstract
Artificial intelligence is becoming the defining technology of our era, but its long-term impact depends on one critical challenge: scalability. As AI evolves toward complex, agentic systems operating from cloud to edge, demands on compute, memory, and connectivity are growing at an unprecedented pace. This keynote explores how sustaining the AI revolution requires innovation across the entire technology stack, from advanced CMOS and heterogeneous integration to photonic interconnects and system-level co-optimization. Looking further ahead, emerging paradigms such as quantum and brain-inspired computing may unlock new forms of efficient intelligence. Ultimately, scalable AI will not emerge from a single breakthrough, but from orchestrating a global ecosystem of technologies, disciplines, and innovators.

Biography
Patrick Vandenameele is Chief Executive Officer at imec - a globally recognized R&D center specializing in nanoelectronics and digital technologies - since April 1, 2026. His leadership underpins imec's commitment to addressing market-driven application challenges while advancing its world-class technology platforms through targeted internal investments and external collaborations.
Prior to this appointment as CEO, he served as Executive Vice President and Co-Chief Operating Officer at imec, where he was overseeing and shaping the organization's R&D strategy and its execution. In this position, Patrick was responsible for shaping and driving the center's innovation agenda, ensuring the alignment of research initiatives with emerging market needs, partner priorities and technological frontiers. Previously, as chief portfolio officer at imec until early 2024, he spearheaded strategic initiatives spanning business development, portfolio management, and venture creation.
Holding a PhD from KU Leuven, Patrick began his journey with imec in 1996, contributing to the wireless communications program. In 2000, he transitioned to entrepreneurship, founding and leading several deep-tech ventures, three of which were built on imec technology. Patrick also held senior positions at top semiconductor firms like Qorvo and Hisilicon/Huawei, leading 11 product launches and overseeing over 100 million units shipped. After returning to imec in 2017, Patrick has been instrumental in expanding imec's venture development activities, working closely with the deep-tech venturing fund imec.xpand to strengthen imec's position as a pioneer in technology-driven solutions.

References

What does an AI Workload actually need from silicon? imec's cross stack view

S. Latré
VP AI
imec, Berlin, Germany

Abstract
As AI workloads increasingly dictate hardware requirements, the semiconductor industry needs a common, vendor-neutral language to connect process and packaging decisions to real-world AI performance. This talk introduces imec's AI Stack: a benchmarking platform and layered framework that maps AI workloads — from inference to training — down through system architecture, device integration, and ultimately to process and materials choices such as lithography parameters and node scaling. Drawing on early results, including a GPU total-cost-of-ownership analysis, we show how fab-level decisions ripple through to workload economics, and outline imec's ambition to build an open ecosystem where hardware and AI software communities can jointly optimise the stack.

Biography
Steven Latré is Vice President AI at imec, the worldwide leading research centre on semiconductors.
In this role, he’s responsible for imec’s AI portfolio, focusing mainly on the intersection of hardware and software and how next generation AI workloads drive the semiconductor roadmap.
Steven has a 20+ year career in AI, leading and scaling highly technical teams on the intersection of AI and hardware.
Previously he was a professor in AI at the University of Antwerp, Chief AI Officer at OpenChip, a full stack chip player in HPC and AI, and was already previously Vice President AI at imec.

References

T. Vanhoutte
Partner - imec.xpand
imec, Leuven, Belgium

Biography
Tom Vanhoutte is founding partner of imec.xpand, an independently managed early stage and growth fund that invests in start-ups where knowledge, expertise, network and/or infrastructure of imec, the world-renowned semiconductor R&D center, plays a differentiating role in the success of the company. The two imec.xpand funds raised over 400 million EUR and are amongst the best performing venture capital funds globally.

References

Panelist

F. Del Maffeo
CEO & Co-Founder
Axelera AI, Berlin, Germany

Abstract
Coming Soon

Biography
Fabrizio Del Maffeo is the CEO and co-founder of Axelera AI, the Netherlands-based startup delivering the world's most powerful and advanced solutions for AI at the Edge. In his role at Axelera AI, Fabrizio leads a world-class executive team, board of directors and advisors from top AI Fortune 500 companies. In 2025 Fabrizio was named in the Top 25 AI CEOs globally, he is a frequent industry speaker, and a sought after expert on decentralized compute. Before establishing Axelera AI, Fabrizio Del Maffeo served as Head of AI at the Bitfury Group, a globally recognized emerging technologies company. Prior to joining Bitfury, Fabrizio was Vice President and Managing Director of AAEON Technology Europe, the AI and internet of things (IoT) computing company within the ASUS Group.

References

Beyond Automotive: chiplets as the Foundation for Autonomous Edge Platforms

G. Sommer
Regional Managing Director
imec, Berlin, Germany

Abstract
Edge High Performance Compute is becoming the “brain” of autonomous systems, enabling the rapid growth of L2+ and future autonomous mobility capabilities. However, the automotive industry faces a fundamental dilemma: compute requirements are increasing exponentially, driven by AI and advanced perception workloads, while the global automotive market remains relatively flat and cannot absorb the rising costs associated with leading-edge semiconductor technologies.

Imec believes interoperable chiplet architectures provide the path forward. By decomposing complex system-on-chip designs into modular building blocks, chiplets enable heterogeneous integration of compute, AI, safety, and memory functions, each optimized on the most appropriate technology node. This approach improves scalability, yield, cost efficiency, supply-chain resilience, and platform reuse while supporting the transition toward software-defined vehicles.

To accelerate adoption, imec is bringing together complementary initiatives across the chiplet value chain. The Automotive Chiplet Forum (ACF) aligns industry stakeholders around open, interoperable chiplet standards, while the Automotive Chiplet Program (ACP) advances pre-competitive research and technology development. Complementing these efforts, the new Chiplet Acceleration Center (CAC) at imec Germany supports design enablement, prototyping, and the path toward industrial deployment. Together, they help de-risk development, advance quality and reliability, and accelerate the transition from chiplet innovation to real-world automotive applications.

Building on the success of ACP, imec is expanding its vision beyond automotive with the launch of the Autonomous Edge Chiplet Program (AECP), addressing shared compute needs across robotics, humanoids, aerospace, and security applications. Complemented by the development of a reference autonomous edge platform, this cross-industry strategy aims to accelerate innovation, reduce costs, strengthen resilience, and establish interoperable chiplets as the foundation for next-generation autonomous systems.

Biography
Dr. Grit Sommer is the Regional Managing Director of imec Germany, a position she has held since July 2026. With almost three decades of experience in the semiconductor industry, she is recognized as a strategic technology leader, transformative executive, and accomplished people manager, combining deep technical expertise with a strong track record of building high-performing global organizations. Prior to joining imec, Dr. Sommer spent 20 years with Infineon Technologies, where she held a series of international leadership positions across Germany and Singapore. Most recently, she served as Senior Director Global Product Engineering Digitalization, leading the digital transformation of end-to-end product engineering across a global network of manufacturing and R&D sites. In this role, she drove the adoption of advanced analytics and artificial intelligence, enabling significant improvements in product development efficiency, yield optimization, and quality management. Throughout her career, Dr. Sommer has successfully led multicultural

teams across Europe, Asia, and the Americas, managing organizations with of up to 50 experts and influencing more than 1,000 employees worldwide. Her expertise spans semiconductor technology, advanced packaging, product engineering, manufacturing excellence, digitalization, and innovation management. She has consistently delivered business impact through strategic program leadership, operational excellence initiatives, and technology-enabled transformation. Before her tenure at Infineon, Dr. Sommer held research and leadership roles at the Fraunhofer Institute for Reliability and Microintegration (IZM), where she established and led advanced RF modelling and simulation activities and managed numerous industry and publicly funded research programs. Dr. Sommer holds a PhD (Dr.-Ing.) in Electrical Engineering and Computer Science from TU Berlin, specializing in RF modelling and design optimization. She also earned her Engineering Degree (Diplom-Ingenieur) in Electrical Engineering from TU Berlin with distinction. In addition to her executive responsibilities, she has served as a board member supporting the strategic development of Fraunhofer IZM and has contributed to industry governance and leadership selection processes. Driven by curiosity, innovation, and an entrepreneurial mindset, Dr. Sommer is passionate about advancing semiconductor technologies and strengthening Germany's role in the global microelectronics ecosystem.

References

Panelist

S. Dubois
CEO
Vertical Compute, Grenoble, France

Abstract
Coming Soon

Biography
Sylvain Dubois, a business executive with 25 years of experience in the compute and memory fields, has extensive knowledge of the deep tech ecosystem and a strong understanding of the memory bottleneck problem, which he explored during his time at Google. Before founding Vertical Compute, Sylvain Dubois held the position of Advanced Technology Sourcing & Partnerships for the Google Cloud Infrastructure group in Sunnyvale, CA. His responsibilities included identifying, analyzing, and developing emerging technology trends, with a focus on Artificial Intelligence hardware acceleration compute chips, memory, and chiplet integration. Prior to his role at Google, he served as Vice-President of Business at Crossbar, a California-based deep tech startup specializing in novel memory development, where he played a key strategic role with several fundraising rounds.

References

Closing keynote: RESOLVE: Engineering Sustainable Compute for Europe

J.-R. Lequepeys
CTO
CEA-Leti, Grenoble, France

Abstract
Coming soon

Biography
Jean-René Lèquepeys received an engineering degree in 1983 from CentraleSupélec, a top French graduate engineering school at Paris-Saclay University, France. He taught physics during 2 years in Ouarzazate, Morocco.

He joined CEA, a French Research and Technology Office focusing on applied research, in Paris Saclay in 1985. He first worked at the laboratory of the Central Security Office, on the evaluation of means of detection and intrusion. Two years later, he was promoted head of this laboratory.

In 1993, he moved to Grenoble, France, and joined the System Division of CEA-Leti. He worked on different projects in the field of image processing and telecommunication technologies. In particular, he was responsible for the "Telecom, Communicating Objects and Smart Card" programs from 1999 to 2004.

In 2005, he took the responsibility of the Circuits Design Division at CEA-Leti (200 people). He launched new research activities at CEA such as a new laboratory in Aix-en-Provence, France, on the development of secured chips. In 2000, Jean-René Lèquepeys received the prestigious award from the french Société de l'Electricité, de l'Electronique et des technologies de l'information et de la communication (SEE) "Grand Prix de l'électronique Général Ferrié" for his work in the telecommunications field (he holds 15 patents).

In 2010, he launched a new division at CEA focusing on Electronic Architectures, Integrated Circuit Design and Embedded Software. He established the structure on two sites (Paris and Grenoble) and led the division twice in his career.

He rapidly got involved in the creation of the Silicon Components Division at CEA-Leti, and took the lead of it in 2011 managing 350 people. Division encompasses micro and nanoelectronics (SOI, nanodots, quantum, memories, 3D technologies, substrates), Micro Systems (sensor, actuator, radiofrequency components) and Power Components. He established the French Nano2022 Program for research funding in microelectronics.

In 2019, he was appointed Chief Technology Officer of CEA-Leti, overseeing Science, relations with the European Commission, Industrial Partnership and Strategic Program Management in the scope of the institute (2,000 people, ~€350m budget). He took the responsibility of the Microelectronic Program at CEA level, spearheading technological and upstream research in the field of semiconductor technologies. For the past 2 years, he has been strongly involved in the CEA-Leti Next Gen FD-SOI project in the frame of France2030 and has played a key role in European chips Act pilot line promoting FD-SOI and Gate All Around technologies.

Having dedicated his career to applied research, he is regularly invited as a keynote speaker in international semiconductor conferences.

Jean-René is also Vice President of ACSIEL, a professional trade union gathering industrial companies in the French electronic value chain, member of the Board of EPOSS, the European Technology Platform on

Smart Systems Integration, a member of the Board of AENEAS, the Association for Europoean NanoElectronics Activities, and an expert consultant for the European Commission and French Research Agency

References

Panelist

F. Le Grevès
President France & EVP Europe and France Public Affairs
STMicroelectronics, Paris, France

Abstract
Coming Soon

Biography
Frédérique Le Grevès is STMicroelectronics' Executive Vice President, Europe and France Public Affairs. She has also held the position of President of STMicroelectronics France since March 2021.

In 1990, Le Grevès started her career in marketing and communication for various international companies in Europe and in the US. From 1995 to 2003, she worked at Aptiv (ex-Delphi Automotive) as EMEA Communication Director. In 2003, Le Grevès joined Nissan Motors as VP Communication for Europe and in 2004, she moved to Los Angeles as VP Communications for Nissan Americas. Le Grevès returned to France in 2008 and joined the Renault Group as Global VP for Corporate Communication. Two years later, she expanded her role to Global VP of Communications and Deputy to the Chief Marketing and Communication officer. In 2011, Le Grevès was appointed Chief of Staff for the Renault Nissan Mitsubishi Alliance Chairman and CEO. More recently, she worked as senior advisor for several companies helping on corporate effectiveness, operations efficiency, and brand reputation.

Le Grevès has been an independent board member of the Supervisory Board of TRIGO Holding from May 2021 to December 2024 and sat on the Strategic Board of Clinatec since October 2021. She is also an independent Director of the Supervisory Board of North Atlantic (formerly Esso SAS) and became a member of their audit committee in June 2024. In 2022, Le Grevès was appointed President of the Strategic Committee for the Electronics Industry sector in France, and in June 2025 became President of the newly created French Electronics Federation (FdEF). She has also been Vice President of the European Semiconductor Industry Association (ESIA) since 2023. Le Grevès was promoted Knight of the Legion of Honor by the French Ministry of Economy and Finance in January 2023.
Born in Suresnes, France, in 1967, Frédérique Le Grevès graduated with a master's degree in business management from the Paris School of Business (1991) and graduated from the Senior Executive Program at the London Business School (2019).

References

Panelist

A. Van den Bosch
VP Strategic Public Policy & Invest for R&D Ecosystems
imec, Leuven, Belgium

Abstract
Coming Soon

Biography
Coming Soon

References

Chips Act 2.0 and SSTS: Building Europe's Next Semiconductor Advantage

S. Shamuilia
ESG Program Director
imec, Berlin, Germany

Abstract
As Europe moves from capability creation to competitiveness, the success of Chips Act 2.0 will depend not only on research infrastructure, pilot lines and manufacturing capacity, but also on the intelligence, innovation and ecosystem collaboration required to sustain them. This presentation explores how imec's Sustainable Semiconductor Technologies & Systems (SSTS) program combines its Assess and Improve activities to create competitiveness intelligence across the semiconductor value chain. By connecting manufacturers, suppliers, researchers, system companies and emerging design ecosystems, SSTS helps address challenges related to sustainability, resilience, resource security and future design enablement. The presentation discusses how such ecosystem intelligence can contribute to Europe's long-term competitiveness and support the ambitions of Chips Act 2.0.

Biography
Sheron Shamuilia leads imec's ESG strategy, embedding sustainability across semiconductor R&D, operations, governance, and strategic partnerships. Her work focuses on positioning sustainability as a driver of responsible innovation, ecosystem resilience, circularity, and long-term value creation. With over 15 years of experience spanning the European Commission, corporate public affairs, and the semiconductor industry, including Cadence, she has worked at the intersection of technology, policy, innovation, and business strategy. Holding a Ph.D. in semiconductor physics, Sheron brings a unique combination of technology expertise, policy insight, and sustainability leadership, helping bridge research, industry, and government to accelerate sustainable innovation and competitiveness across the semiconductor ecosystem.

References

From Vision to Impact: Three Years of NanoIC Enabling Future Semiconductor Technologies

F. Holsteyns
VP R&D Unit Process & Modules
imec, Berlin, Germany

Abstract
Three years after its launch, NanoIC grows into a collaborative European innovation ecosystem that accelerates the development of the chips of the future. Driven by a shared ambition to strengthen the semiconductor innovation and expand manufacturing capabilities, NanoIC brings together industrial and research partners around advanced technology platforms and infrastructure. By highlighting key achievements in Logic, Memory and Heterogeneous Integration, we showcase how collaborative R&D and shared infrastructure can accelerate innovation and reduce barriers to technology development. Engagement with companies, leveraging this new ecosystem, allows to jointly shape the next generation of semiconductor technologies together.

Biography
Frank Holsteyns has been serving as the VP of R&D at imec, leading the Unit Process and Module Department since July 1, 2023. Before stepping into this role, he was the director of the same department, where he managed various process-development-focused groups, including surface and interface processing, etch, thin film deposition, epitaxy, plating, chemical mechanical polishing, layer transfer, and assembly.
Frank's journey at imec began in 2000, where he concentrated on wet cleaning research for semiconductor devices. His work in this area culminated in a PhD in Bio Engineering (surface chemistry) from KU Leuven, Belgium. In 2006, he transitioned to Lam Research AG in Villach, Austria, as a research scientist. There, he coordinated a university and research network focused on fluid dynamics, particularly cavitation, droplet impact, wetting, and dewetting.
In 2012, Frank returned to imec, taking on the role of manager for the Surface and Interface Processing Group. In this position, he specialized in wet clean and etch processes, as well as isotropic dry etches.

References

Design enablement services: lowering the barrier for IC design companies

R. Hoofman
Strategic Development Director
imec, Berlin, Germany

Abstract
As part of the EU Chips Act, the EU Chips Design Platform (EuroCDP) has been launched. EuroCDP's mission is to lower the barrier for fabless IC design companies, in particular startups. This will be done by lowering the technical barriers and the cost of the design process, plus in addition dedicated venture development together with private investors. EuroCDP is designed as a one-stop marketplace for startups, SMEs, and research teams, offering streamlined access to advanced design tools, manufacturing, IP, training, and funding.

Biography
Romano Hoofman is Strategic Development Director at imec since 2016. He is responsible for the coordination of both the EU Chips Design Platform and the EUROPRACTICE Service. In addition, his team is responsible for providing technology access and design enablement for the NanoIC pilot line, 2D-PL and SPINS (Quantum pilot line). He started his career in industry, where he worked as a Principal Scientist at Philips Research and later on NXP Semiconductors. He covered many different R&D topics, ranging from CMOS integration, advanced packaging, thin film batteries, photovoltaics and (bio)sensors. Romano received his PhD from the Technical University of Delft in 2000, where he investigated charge transport in semi-conducting polymers. He has authored more than 30 publications and holds more than 10 patents in various research areas.

References

Closing Remarks

K. Marent
EVP & Chief Marketing and Communications Officer
imec, Berlin, Germany

Abstract
Coming Soon

Biography
Katrien Marent has an engineering degree in microelectronics. She joined imec in 1992 as analog design engineer and specialized in design of low-noise readout electronics for high-energy physics. In 1999, she became press responsible and scientific editor at imec's business development division and was responsible for authoring and editing the research organization's numerous company technical documents and publications. In 2001, she was appointed corporate communications director at imec. Her responsibilities expanded in August 2007, when she got the position of external communications director including corporate, marketing and outreach communications. In October 2016, she became VP corporate, marketing and outreach communication. Since April 2020 she is Executive Vice President & Chief Marketing and Communications Officer and member of the executive board of imec.

References