Advanced Packing Conference

Welcome Remarks

L. Altimime
President
SEMI Europe, Berlin, Germany

Abstract
Coming Soon

Biography
Laith Altimime, as President of SEMI Europe, leads SEMI's activities in Europe and the Middle East and Africa (EMEA). Altimime has P&L responsibility as well as ownership of all Europe region programs and events, including SEMICON Europa. He is responsible for establishing industry standards, advocacy, community development, expositions, and programs. He provides support and services to SEMI members worldwide that have supply chain interests in Europe. He manages and nurtures relationships with SEMI members in the region and globally as well as with local associations and constituents in industry, government, and academia. Altimime has more than 30 years of international experience in the semiconductor industry. Prior to joining SEMI in 2015, He held senior leadership positions at NEC, KLA-Tencor, Infineon, Qimonda, and imec. Altimime holds an MSc from Heriot-Watt University, Scotland.

References

Opening Remarks by Session Chair

S. Kröhnert
President & Founder
ESPAT Consulting, Dresden, Germany

Abstract
Coming Soon

Biography
Coming Soon

References

Scaling Beyond the Fab: Advanced Packaging, Test, and Supply-Chain Outlook

C. Tseng
Sr. Director
SEMI, Milpitas, United States of America

Abstract
AI-driven growth is reshaping semiconductor manufacturing well beyond the wafer fab. As compute and memory requirements increase, advanced packaging and test are becoming more important to overall system performance, manufacturing capacity, and supply-chain planning.

This presentation will examine how the current semiconductor investment cycle is translating into stronger demand for test and assembly and packaging equipment, with particular attention to the growing complexity of AI accelerators, HBM, chiplet-based designs, and high-density integration. It will also explore how packaging and test capacity are distributed geographically, using SEMI's assembly and test facility data to assess the potential for greater regional diversification.

The presentation will conclude with a look at the implications for Europe, including opportunities in specialty semiconductor manufacturing, equipment, materials, and emerging packaging technologies such as glass core substrates. The key message is that future semiconductor scaling will depend increasingly on the industry's ability to expand not only wafer capacity, but also packaging, test, and the supporting supply-chain ecosystem.

Biography
Clark Tseng is Senior Director of Market Intelligence at SEMI, where he leads the development and execution of global market intelligence strategies covering the semiconductor manufacturing supply chain. He oversees SEMI's market research portfolio and global research partnerships, providing analysis and forecasts on fab investment, capacity, equipment, materials, and semiconductor manufacturing trends.

Clark has extensive experience analyzing the semiconductor industry across foundry, IDM, memory, fabless, and OSAT markets, with a particular focus on manufacturing investment, technology transitions, and regional supply-chain dynamics.
Before joining SEMI, Clark held strategic and analytical roles at leading technology companies. At MediaTek, he served as Deputy Director of the Computing, Connectivity, and Metaverse Business Group, providing market intelligence and competitive analysis across computing, connectivity, automotive, and emerging technology markets. Previously, he was Division Manager for Strategy and Business Development at Qimonda, where he led market and competitive intelligence activities for the Asia-Pacific region. He began his career as an analyst at IDC, covering semiconductor, flat-panel display, and telecommunications markets.

Clark holds a Bachelor of Business Administration and a Bachelor of Arts in International Relations from National Chengchi University in Taiwan.

References

Coming Soon

A. Chichkov
Head of Programmes & Communication
Chips JU, Brussels, Belgium

Abstract
Coming Soon

Biography
Anton Chichkov (pronounced Shishkov) is currently Head of Programmes at Chips Joint Undertaking (Chips JU). Holding a PhD in Computer Science from the Technical University of Lisbon and a background in chip design and design for test, Anton Chichkov brings 37 years of experience in the electronic components and systems (ECS) sector. His career spans roles as a chip designer, test equipment manufacturing, researcher in an RTO, and a decade in semiconductor manufacturing, before joining ENIAC JU and now contribute to shaping Europe's semiconductor ecosystem through Chips JU.

References

Advanced Packaging: Redefining the New Front End Through Materials Innovation

B. Ernst
SVP and Head of Strategy and Transformation
Merck KGaA, Darmstadt, Germany

Abstract
As semiconductor demand driven by AI continues to increase and traditional scaling methods near their limits, the trends toward advanced chip architectures and 3D densification are accelerating. The traditional boundary between front-end wafer fabrication and back-end assembly is increasingly blurring. Advanced packaging has become the “new front end,” where performance, power
efficiency, yield, and reliability are determined by processes and materials that increasingly resemble those used in the most advanced logic manufacturing environments, powered by the same fundamentals.
Feature sizes in advanced packaging are still relatively large today, but hybrid bonding is changing, driving miniaturization and complexity. It must be approached with the same level of process control, materials sophistication, metrology, and systems understanding that have defined front-end semiconductor manufacturing for decades. Merck’s integrated materials-and-systems solutions will be at the heart of it.
Europe has a unique opportunity to establish a strong position in advanced packaging. Building on its world-class semiconductor ecosystem—including leaders in equipment, process technologies, and innovation. Europe is well positioned to accelerate the next wave of semiconductor advancement through advanced packaging technologies.
In this keynote, Merck will share its perspective on how materials innovation is becoming a key enabler of advanced packaging growth. Critical materials including CMP slurries, cleaning solutions, thin-film deposition materials, and other specialty chemistries must now address challenges.
We will explore how front-end manufacturing experience provides a critical foundation for solving advanced packaging challenges, what differentiates packaging materials development from traditional front-end applications, and how collaborative innovation across the European semiconductor ecosystem can create a sustainable competitive advantage. As advanced packaging becomes a strategic driver of semiconductor performance, Europe has a timely opportunity to shape its
future, and materials innovation will be at the center of that journey.

Biography
Benedikt Ernst is the SVP and Head of Strategy and Transformation at the Electronics business of Merck KGaA, Darmstadt, Germany. As a member of the Electronics Executive Committee, he is responsible for the end-to-end strategic development and transformation of the business sector, encompassing market competitive intelligence, strategic roadmap, business transformation programs, and business and portfolio development. He joined Merck KGaA, Darmstadt, Germany in 2006, and has had various management positions. Since 2018, he has been heading Strategy and Business Development for Electronics and Semiconductor. Before he was Commercial Director for the Semiconductor business and Head of Packaging Business Field.
Benedikt Ernst studied physics at the Technical University of Munich and at the Max Planck Institute of Plasma Physics.

References

WalTIS: Wafer-Level Thermal Integration for Advanced Semiconductor Packaging

A. van Geelen
CTO
CoolSem Technologies, Eindhoven, The Netherlands

Abstract
The continuous increase in power density in modern semiconductor devices is placing unprecedented demands on thermal management at the package level. In RF, photonics, power electronics and compute, local power densities exceeding 10 W/mm² are increasingly common, while conventional substrates and package architectures often introduce thermal bottlenecks that limit device performance, reliability, and achievable integration density. Addressing these limitations requires a shift from package-level heat removal to thermal path engineering directly at the wafer level.
CoolSem introduces a packaging approach in which the thermal management of semiconductor devices is addressed at the wafer level rather than only during package assembly. The concept focuses on integrating a thermally optimized carrier and insulating stack directly beneath active semiconductor layers, enabling efficient heat spreading while maintaining electrical isolation and compatibility with standard semiconductor fabrication processes.
A central element of the CoolSem technology platform is WalTIS (Wafer-level Thermal Integration Stack), an integration architecture that combines a thermally conductive carrier with an electrically insulating layer stack to create a high-performance thermal path directly beneath active devices. WalTIS significantly shortens the thermal path between device junction and the heat-spreading substrate. Thermal modelling indicates that the WalTIS architecture can achieve up to a 10× reduction in junction-to-heatsink thermal resistance compared to state-of-the-art approaches based on thinned GaAs or GaN substrates mounted on regular heat spreaders. WaLTIS maintains electrical isolation and wafer-level manufacturability. The concept is compatible with a range of semiconductor technologies, including III–V RF devices, photonic components, and other high-power and high performance compute semiconductor platforms.
From a packaging perspective, WalTIS represents a new class of engineered carrier in which conventional semiconductor substrates are replaced by a thermally optimized integration stack. This architecture enables improved heat extraction while preserving mechanical stability. By relocating key thermal management functions from the package level to the wafer level, the approach opens new integration strategies for high-power semiconductor systems.

Biography
Dr. André van Geelen has a PhD in Physics and is an experienced executive in the semiconductor and mobile markets. After several roles at Philips and JDS-Uniphase, he was part of the management team of the high tech startup III-V Photonics around 2000. In 2007, he founded EPCOS Netherlands via a spin-out from NXP semiconductors to generate antenna tuners for mobile. This company was acquired by Qualcomm in 2014. From 2015 onwards, he supported high tech start- and scale-ups in finding their strategic direction, acquiring startup capital and in building the company team and culture. In 2025, he recognized increasing issues around thermal management of high power chips and together with his co-founders started CoolSem Technologies.

References

Hydrodynamics-Driven wet etching for scalable fabrication of high-aspect-ratio through-glass vias in glass core substrates

S. Zürcher
Head of Process Technology
AP&S International GmbH, Donaueschingen,
Germany

Abstract

The scalable fabrication of high-aspect-ratio through glass vias (TGV) in large-area glass core substrates remains a critical bottleneck for next-generation advanced packaging technologies. While hybrid laser–etching approaches have demonstrated fundamental feasibility, the lack of precise control over etch homogeneity, via geometry, and process scalability continues to limit their implementation in high-volume manufacturing. This work presents an integrated, simulation-driven wet processing approach that addresses these limitations by introducing hydrodynamic control within the etching stage, enabling deterministic shaping of TGV structures at wafer and panel scale.

The proposed solution builds on a combined femtosecond laser modification and selective wet chemical etching process chain, in which laser-induced structural changes in the glass bulk define regions of enhanced chemical reactivity. The key innovation presented here lies in the subsequent etching process: by engineering the fluid dynamics within the etch environment, mass transport limitations are actively mitigated. Within AP&S wet processing equipment, a novel hydrodynamic design enables uniform delivery of the etching medium. This controlled flow regime enhances local reactant availability while ensuring efficient removal of reaction by-products, resulting in improved etch kinetics and uniformity. Compared to conventional immersion-based approaches, the method allows for tighter control of critical geometrical parameters, including via diameter (20–100 µm), aspect ratios exceeding 10:1, and well-defined sidewall profiles across the entire substrate.

A central contribution of this work is the integration of computational fluid dynamics (CFD) into both equipment and process design. By leveraging simulation-based optimization, the hydrodynamic conditions can be pre-configured for varying substrate dimensions and layout densities without empirical iteration. This not only reduces development time but also enables rapid process transfer across different product configurations.

The results demonstrate that hydrodynamically optimized wet etching represents a key enabler for translating laser-based TGV fabrication from laboratory to industrial-scale manufacturability. The presented approach establishes a pathway toward highly uniform, high-throughput, and geometry-controlled TGV formation, thereby addressing a challenge in the deployment of glass core substrates for advanced electronic systems.

Biography

Stefan Zuercher is the Head of Process Technology at AP&S and has more than 15 years of experience in the semiconductor industry. He joined AP&S in 2011 as a process engineer for wet processes (etching, cleaning, drying, electroless UBM metallization), installing and qualifying wet process equipment worldwide for over a decade.

In 2014, he became the manager of the newly established AP&S DemoCenter, and in 2017 he advanced to Process Manager. In this role, he was responsible for all process-related tasks, including tool qualifications and optimization, as well as process development across AP&S equipment platforms for singlewafer, batch, and parts-cleaning applications for advanced semiconductor manufacturing.

Since 2024, as Head of Process Technology, he has fully focused on delivering customer-oriented process solutions across the AP&S product portfolio and DemoLAB, as well as driving advancements in simulation engineering within the AP&S SimLAB.

References

Engineering Bonding Materials for Power Devices Using Stress-Relaxing Sintering Materials and Transient Liquid Phase Diffusion Bonding Sheet

S. Abe
Senior R&D Manager
TANAKA Precious Metals, Ag Adhesive Global R&D, Frankfurt am Main, Germany

Abstract
The continuous evolution of power semiconductor devices, particularly SiC and GaN, is driving increasing demands on bonding technologies in advanced packaging. Bonding layers must provide electrical conduction, thermal management, and mechanical compliance against coefficient of thermal expansion (CTE) mismatch under high-temperature conditions.

In this study, we present an integrated approach to engineering bonding materials for next-generation power device packaging. This approach combines stress-relaxing sintering materials, transient liquid phase diffusion bonding (TLP bonding) sheets, and emerging Cu-containing systems, enabling optimized material selection for die attach, clip attach, and substrate attach.

First, a stress-relaxing sintering paste is introduced for die attach and clip attach. This material can be applied by dispensing or printing, offering flexibility for various package structures. Its engineered microstructure, with resin domains dispersed within the sintered network, reduces elastic modulus while maintaining high thermal conductivity. This enables effective stress dispersion and achieves stable reliability beyond 2000 thermal cycles with suppressed interfacial degradation. Compatibility with bare Cu surfaces further supports cost reduction and simplified processing.

Second, a TLP bonding sheet is presented for applications requiring high-temperature stability, including die attach and substrate attach. This material enables bonding at relatively low temperatures (~250 °C) while forming high-melting-point intermetallic compounds after bonding. The bonding layer maintains high mechanical strength at 300 °C and demonstrates reliability beyond 2500 thermal cycles. This approach is particularly advantageous for large-area joints, making it suitable for substrate-level interconnections and large die applications.

A bonding material selection framework is proposed, where stress-relaxing sintering materials are used for applications requiring compliance and process flexibility, while TLP bonding sheets are suited for high-temperature and large-area bonding.

Finally, Cu-containing bonding materials are briefly introduced as a future direction to improve cost efficiency and compatibility with Cu-based substrates.

In conclusion, a multi-material bonding strategy enables reliable bonding solutions for next-generation power devices.

Biography
Shintaroh Abe is a Global R&D Senior Manager at Tanaka Europe, specializing in bonding materials for power semiconductor packaging. His work focuses on the development and global deployment of Ag adhesives and stress-relaxing sintering materials for die attach applications.
He has experience in copper nanoparticle and printed electronics materials, and has expanded technologies originally developed in Japan into overseas markets, supporting their adaptation and advancement in both Asia and Europe. He has been engaged in global R&D activities, contributing to the development of next-generation composite materials for power devices.

References

Application of SnAg and Nano-Porous Cu Structures for Advanced Micro-Bump Pattern and Their Properties

K. Tatsumi
Manager
Mitsubishi Materials Tools Europe GmbH,
Advanced Product Group, Meerbusch, Germany

Abstract
As semiconductor devices continue to demand higher integration density, fine-pitch micro-bump interconnects have become increasingly important in advanced packaging technologies. Although SnAg solder bumps are widely used for flip-chip bonding, their application to ultra-fine pitch structures is limited by strict requirements for electroplating control and assembly precision. In particular, ensuring bump height uniformity and reliable bonding at micrometer-scale dimensions remains a significant challenge.

In this study, a novel micro-bump structure consisting of nanoporous copper coated with a SnAg passive layer (NP-Cu/SnAg) is proposed to address these limitations. The nanoporous Cu framework provides low-temperature sintering capability and mechanical compressibility, enabling effective absorption of bump height variations during bonding. Furthermore, the SnAg coating improves the structural stability of nanoporous Cu, preventing dissolution during processing.

Micro-bump test structures with diameters of approximately 10 μm and pitches of 20 μm were fabricated using electroplating techniques. Both conventional SnAg and NP-Cu/SnAg bumps were successfully formed and evaluated through morphological observation and bump height measurement. The NP-Cu/SnAg bumps exhibited excellent height uniformity, with variations below 2 μm, and their compressible structure enabled complete bonding even under fine-pitch conditions.

Electrical and reliability performance were assessed using daisy-chain resistance measurements and thermal cycling tests. The NP-Cu/SnAg bumps demonstrated lower initial electrical resistance compared to conventional SnAg bumps. Additionally, while the resistance of SnAg bumps increased after thermal cycling, NP-Cu/SnAg bumps maintained stable electrical characteristics, indicating superior thermal reliability.

These results confirm that NP-Cu/SnAg micro-bump structures provide improved process tolerance, enhanced electrical performance, and robust reliability. Therefore, they represent a promising solution for next-generation semiconductor packaging requiring ultra-fine pitch and high-performance interconnects.

Biography
After majoring in chemistry at university, I joined Mitsubishi Materials Corporation in 2011. I spent ten years engaged in the development of SnAg plating chemicals for semiconductor Advanced packaging. During this period, I also provided technical support to customers across Asia, as well as in Europe and the United States, contributing to the expansion and optimization of plating technologies in global markets.

I subsequently worked in a corporate planning role at the company’s headquarters for three years, where he was involved in business strategy and organizational initiatives.

Since June 2025, I have been based in Germany, serving as a manager responsible for European marketing and business development, actively driving growth and strengthening the company’s presence in the region.

References

A Design-Enabled Advanced Packaging Ecosystem for Heterogeneous Integration and Co-Packaged Optics

C. McDonough
Manager of 3DHI
AIM Photonics, Albany, United States of America
E. Lavigne
Senior Director, Tech Strategy and Partnerships
NY Creates, Albany, United States of America
G. Jampana
Associate Director, Business Development
NY Creates, Albany, United States of America

Abstract
Rapid growth in data generation and consumption continue to drive unprecedented bandwidth and energy-efficiency requirements. This has accelerated the need for innovations in advanced packaging and co-packaged optics (CPO). Access to these technologies is limited to volume manufacturers with narrow ranges of high-maturity processes and products. There is a need to access to cutting-edge, advanced packaging technologies for R&D, that are rapidly scalable, in manufacturing-relevant conditions. The New York Center for Research, Economic Advancement, Technology, Engineering and Science (Creates) and American Institute for Manufacturing Integrated Photonics (AIM Photonics) fill this need together by offering practical frameworks through five focus areas: interposers and custom 3DICs; hybrid bonding; wafer-level packaging; CPO; and test, assembly and packaging services. Key technologies are 300mm silicon interposer platforms, TSV integration (down to 1×10µm), and multiple 3D stacking approaches. Chip-level integration alongside wafer-level bonding allows designers to prototype across a wide range of interconnect densities and performance regimes. Hybrid bonding enables ultra-fine-pitch interconnects with orders-of-magnitude improvements in density over bump-based methods, while reducing energy consumption. Current development spans pitches down to 0.5µm with planned extensions to die-to-wafer integration. Wafer-level packaging capabilities further enhance prototyping by supporting fine-pitch bumping (<25µm), RDL for wafer-level fan-out, and TCB integration. CPO is emerging as a critical architecture for delivering low-power, high-bandwidth performance in the datacenter and beyond by tightly integrating electronics and photonics within the package. AIM Photonics supports this transition through multiple photonic integrated circuit platforms and a range of photonic packaging capabilities, including electronic-photonic interposers, on-chip laser integration, detachable fiber array units, and low-loss optical coupling strategies. Central to the AIM Photonics ecosystem is design enablement through PDKs and ADKs, linking device, package, and test considerations within a unified framework. Together, these capabilities establish a design-enabled prototyping environment that accelerates cycle time, reduces integration risk, and provides a scalable bridge from concept to deployment for next-generation advanced packaging systems at Creates' Albany NanoTech Complex.

Biography
Dr. Colin McDonough is Manager for 3D & Heterogeneous Integration for the American Institute for Manufacturing Integrated Photonics (*AIM Photonics*) at the New York Center for Research, Economic Advancement, Technology, Engineering and Science (*Creates*) in Albany, NY. Colin specializes in 3D integration and advanced packaging, with a particular focus on silicon photonics and interposer technologies. He has lead development efforts in TSV fabrication, wafer-to-wafer direct bonding for electro-optic heterogeneous integration, and on-chip laser integration. Colin earned his Ph.D. in Nanoscale Science & Engineering in 2011 at the University at Albany, State University of New York and is a Senior Member of IEEE.

Dr. Erin Lavigne is a senior leader in the semiconductor industry with more than 15 years' experience spanning technologies, businesses, and continents. Erin began her career at IBM developing leading-edge advanced patterning and metrology solutions for IBM's high-end server products. From there, she moved to a role in Leading-Edge Product Management at GlobalFoundries, where she drove their technology and customer strategy for their 14/12nm FinFET programs. Most recently, Erin was at Meta developing innovative process engineering and integration for advanced displays for AR/VR/MR applications. Throughout this journey, Erin has led multidisciplinary teams spanning Europe and the USA. In her current

role at NY Creates, she has returned to her roots, leading the technology strategy and partnerships ecosystem for NY Creates' EUV and Advanced Patterning Center, Design Enablement Ecosystem and Advanced Packaging in Albany, NY.

Gayathri Jampana is currently working as Associate Director in Business Development team for Advanced Packaging at NY Creates. She started her career in Advanced Packaging as Graduate Research Assistant at University of Arkansas fabricating a 100 micron interposer at HiDEC Fab. After graduation, she was hired by Brewer Science as Associate Applications Engineer developing processes for WaferBOND materials. After that, Gayathri was hired at SUSS Microtec as Applications engineer for XBS300 Wafer Bonding tool and developed process flows for different temporary wafer bonding materials. She moved to Canada and worked as Program Manager at TechInsights before starting at NY Creates.

References

SWIR Illumination for Sub-Surface and Backside Inspection in Advanced Packaging Metrology

D. Stacey
Business Development Manager
CoolLED, Andover, United Kingdom

Abstract
As advanced packaging continues to increase in complexity, optical inspection and metrology are facing new challenges in detecting defects hidden beneath the surface or on the backside of packaged assemblies. Conventional visible-light imaging often lacks the contrast and optical penetration needed to reliably reveal these defects, particularly in the presence of dense structures, mixed materials, and highly reflective interfaces.

This presentation will discuss the role of short-wave infrared (SWIR) illumination in improving inspection and metrology capability for advanced packaging applications. In particular, it will examine how wavelength selection, angular illumination, polarization, and etendue influence image formation, optical throughput, and defect visibility. These factors will be considered in the context of common advanced packaging structures such as hybrid bonds, redistribution layers, micro-bumps, through-package features, and heterogeneous integration assemblies.

The talk will describe how SWIR-based illumination can support both defect detection and quantitative metrology by improving contrast for sub-surface and backside features, enabling more robust segmentation and feature extraction, and improving measurement repeatability across different package materials and geometries. Practical considerations for calibration, system integration, and reproducibility will be addressed.

Overall, the presentation will highlight how SWIR illumination can extend the reach of optical inspection and metrology in advanced packaging, increasing the visibility of defects that are otherwise difficult to detect using conventional imaging methods.

Biography
Gerard Whoriskey is the Chief Technology Officer at CoolLED, a position he has held since the company's founding over 20 years ago. With a background in Electronic Engineering, Gerard's journey into photonics began during a university KTP project investigating LED technology, the outcomes of which were instrumental in the formation of CoolLED and the introduction of the first commercial LED illumination solution for scientific applications. Over the course of his career, he has developed deep expertise spanning both electronics and optics, positioning him at the forefront of LED-based illumination innovation.

References

Functional Silicon Interposers for 2.5D integration

C. Guhl
Fraunhofer IPMS-CNT, Dresden, Germany

Abstract
The ever-rising demand for computational power increase poses a great challenge, one solution is to combine multiple functions as chiplets with high I/O density employing a silicon interposer. The key to successful combination of chiplets in a system is high I/O density, thus small pitches approaching BEoL dimensions. Usage of silicon interposers with damascene based interconnect lines has the key benefit of a mature technology easily scalable to sub µm dimensions. Unfortunately, Silicon interposers with damascene based RDLs are comparably expensive. One industry reaction to the cost issue was miniaturization of Silicon interposers for cost savings, namely EMIB. Another possible consequence of the cost issue for Silicon interposers is to raise their value by integrating passive devices to realize a functional interposer.

In the contribution we present the concept of integrated capacitors and resistor networks. By utilization of Silicon based production steps it is possible to integrate 3D capacitors in silicon interposers realizing capacity densities of up to 400nF/mm². As the capacitors move from a location next to active devices to directly below the active devices the wiring length can be reduces from several mm to few µm. The unique combination of close proximity high density capacity is crucial and allows to work e.g. without capacitor ladders.

Advanced chiplet interconnection schemes like UCIe 3.0 and mobile hardware trends to lower switching voltages further increase the demand for integrated passive devices. To realize high data transfer rates like 64 GT/s in UCIe 3.0 impedance matched transmission lines are crucial. One way to realize these is integration of distinct passive devices. For ultra low power devices not only the operation voltage, but also the voltage tolerance is minimal. Such low tolerances are challenging to realize and demand a maximum capacity in ultimate proximity to the active devices. Both challenges can be tackled by functional silicon interposers.

Biography
Conrad Guhl:
2009-2015 Bachelor & Master on Materials Science at Friedrich-Schiller-Universität Jena; Focus on metallic materials
2015-2018 PhD in Materials Science at Technische Universität Darmstadt; XPS on battery cathode materials
2019-2023 Scientist for Chemical Mechanical Polishing at Fraunhofer IPMS; Focus on design process interactions
2024-open Group Leader Interconnect Technologies; work package leader in EU Chips act project "*Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems*"

References

Leveraging Advanced Bonding Technologies to Enable Scalable Co-Packaged Optics Architectures

E. Brandl
Business Development Manager
EVG, St. Florian am Inn, Austria

Abstract
Heavy data workloads have already driven the deployment of optical interconnects as a practical solution to the limitations of electronic data transfer. Especially with artificial intelligence (AI), the need for efficient data transfer is again immensely increased. Optical interconnects are now used in modern data centers and high-performance systems, enabling high-bandwidth, low-latency, and energy-efficient communication across chips and racks. Supported by advances in silicon photonics and system integration, these optical technologies have become a key enabler for scaling today's large AI models and infrastructure.

In this work, we present an overview of manufacturing approaches for silicon photonic components and their integration into various optical interconnect architectures. A particular emphasis is placed on advanced bonding techniques as an enabler for heterogeneous integration. We examine both die-to-wafer and wafer-to-wafer bonding strategies, highlighting their advantages: die-to-wafer bonding provides flexibility for selectively integrating high-performance components, while wafer-to-wafer bonding enables parallel, high-volume fabrication with improved uniformity and scalability. The discussed bonding technologies include temporary bonding, plasma-activated fusion bonding, oxide-free direct bonding, and hybrid bonding. Such methods enable the integration of diverse material systems, including III–V semiconductors for realizing efficient on-chip light sources, as well as thin-film lithium niobate for high-performance electro-optic modulation. By combining these materials with silicon photonics platforms, it becomes possible to leverage their complementary properties. III–V compounds offer high optical gain compared to Si, and lithium niobate has a high electro-optical efficiency. By integrating different material systems, the functionality and performance of integrated photonic circuits is significantly enhanced.

By combining these advanced bonding techniques with scalable process flows, a versatile manufacturing toolbox is established, capable of supporting highly integrated, high-performance optical interconnect systems tailored to the stringent requirements of AI computing.

Biography
Elisabeth Brandl is business development manager at EV Group for temporary bonding and metrology. She holds a Master degree (DI) in technical physics from the Johannes Kepler University Linz specialized on nanoscience and - technology.
Since 12 years she works at EVG and was, amongst other topics responsible for the UV laser debonding launch. She published several articles and papers in the field of temporary bonding and metrology.

References

Application of Underfill and Benzocyclobutene in Advanced Flip Chip Technology for Packaging and Reliability in Terrestrial and Space Environments

R. Sur
Staff Product Engineer
Elevate Semiconductor, San Diego, United States of America

Abstract

Flip-chip technology is increasingly popular due to its low parasitics and compact package size, especially as traditional wire-bonded packages introduce higher parasitics. With the rise of artificial intelligence and the deployment of data centers in space, advanced packaging is essential for withstanding extreme atmospheric conditions and ensuring long-term reliability. Traditional flip-chip packaging has used both thin and thick polyimide, but both are prone to cracking over time. Benzocyclobutene (BCB) offers superior stress resistance and does not crack, making it a more reliable alternative. Effective use of BCB requires a tri-metal or under-bump metallurgy (UBM) layer; in my process, I used titanium, copper, and titanium, followed by BCB to open the vias for solder bump attachment. This paper outlines the BCB curing procedure, including the application and curing time before solder bumps are formed by electrochemical deposition. Electrochemical deposition is preferred because it produces more robust solder bumps than stenciling, which can fail during high-temperature operating life (HTOL) or temperature cycling. While some use reballing to continue testing, this is not standard practice in the Aerospace and Defense industry. The combination of BCB and UBM ensures solder balls remain secure during reliability stress testing.

Solder bump composition is critical for process robustness. This paper provides a detailed analysis of the solder bump materials required to withstand the extreme conditions found in Aerospace and Defense applications. As data infrastructure expands into space, selecting the appropriate solder bump composition, BCB, and underfill materials is essential for long-term chip reliability. One of the main challenges for integrated circuit chips in space is the stress caused by angular velocity and momentum. This paper details the entire flip-chip process, including the use of Dexter Hysol, which helps maintain solder bump reliability under these conditions. I have conducted extensive HTOL and temperature-cycling tests in accordance with MIL-STD-883 standards, with tests running for over 4000 hours without any damage to the flip-chip structure.

Biography

Rajesh Sur is a Senior staff product engineer with Elevate Semiconductor. He earned a B.S.E.E. degree from MIT Manipal, an M.S.E.E. from University of Arkansas, Fayetteville, and an M.B.A. degree from Wake Forest University. Rajesh is a senior member of the IEEE. He currently holds 868 worldwide patents and is one of the most prolific inventors in the state of North Carolina He is the author of eleven technical books. Rajesh has 23 years' experience as a senior product engineer, senior packaging engineer, and product engineering manager having previously worked at Texas Instruments, Freescale Semiconductor, Analog Devices and Qorvo.

References

Advanced Packaging for high mix and low volume, Flip Chip capabilities beyond the standard in Europe

D. Lieske
Senior Expert Advanced packaging
AEMtec GmbH, Advanced Packaging, Berlin,
Germany

Abstract
This presentation will showcase AEMtec's flip chip capabilities especially developed for harsh environments like applications in space. It will give first reliability results and processes, that have been used for qualification purpose under the support of ESA (European Space agency). Furthermore we will show the demand in future for FOWLP, Copper pillar and micro bump in the field of flip chip and chiplet applications.

Discover how AEMtec transformed from an IDM into a leading specialized OSAT, carving out a unique position in the European semiconductor landscape. While industry roadpaths often follow rigid lines, AEMtec thrives on complexity: we build custom-specific package designs that lay the groundwork for future technologies.

Biography
Daniel Lieske, Senior Expert Advanced Packaging @ AEMtec GmbH

Daniel Lieske is Senior Expert for Advanced Packaging Technologies at AEMtec in Berlin.
In this role, he supports both product and process development teams and advises the sales department on new customer projects. His technical focus includes advanced packaging technologies such as Fan-Out WLP, RDL, Flip Chip, and photonics packaging, ensuring that AEMtec meets current and future market demands.
He holds a diploma in Microelectronics and Microsystems from Brandenburg University of Technology in Cottbus. Daniel began his career as a Process Engineer at Infineon Technologies Dresden and Qimonda, working in the Backend on development, production, and technology transfer of multi-chip modules to high-volume manufacturing sites. As a Project Engineer at Freudenberg Mechatronics, he developed and optimized production equipment for automotive lighting applications.
For the past 15 years at AEMtec, he has been responsible for wafer-level solder ball attach, printing technologies, solder reflow, and failure analysis.

References

R. Antonicelli
Senior Director, Strategy & Business Innovation
JCET Group, Laussane, Switzerland

Biography
Coming Soon

References

Heterogeneous Integration for Chiplets for Broad Industrial Applications

B. Han
CEO
Silicon Box, Singapore, Singapore

Abstract
This presentation explores a broad range of applications utilizing chiplet integration. The diversity of these applications poses significant manufacturing challenges, particularly when investment for production variety must be minimized. To address these hurdles, various manufacturing schemes are evaluated, and the current industry consensus is examined. Ultimately, the direction of this technological convergence will provide valuable insights for future investment strategies.

Biography
Dr. BJ Han is the CEO and co-founder of Silicon Box, a forefront semiconductor integration and advanced packaging company. An industry pioneer and inventor with over 300 patents, Dr. Han brings extensive expertise to Silicon Box to address the global shortage in chiplet integration infrastructure. His innovations, including Quad Flat No-Lead (QFN) and Fine-Pitch BGA (FBGA) packages, ship over 100 billion units annually.
Prior to founding Silicon Box, Dr. Han spent 20 years at STATS ChipPAC, serving as Chief Executive Officer and Chairman of the Board. His distinguished 40-year career also includes leadership and research roles at AT&T Bell Labs, IBM Research, and Amkor, as well as consulting with Bain & Company. Recognized globally for his contributions, he was awarded the Leonardo International Prize in 2025 for strategic investments in Italy's technological landscape and named to *Tatler's* Asia's Most Influential list in 2024 and again in 2025. Dr. Han holds a PhD from Columbia University and is an alumnus of the Advanced Management Program (AMP) at Harvard University.

References

Scaling Advanced Packaging: The Wafer-to-Panel Revolution

N. Tien
Senior Technical Program Manager
ASE, Brussels, Belgium

Abstract
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Biography
Nicole Tien is a Senior Technical Program Manager at ASE Europe, where she drives advanced packaging technology development and innovation to support customer growth and ecosystem collaboration. She focuses on high-performance heterogeneous integration, including multi-die and 3D packaging solutions, enabling improved system-level performance, bandwidth, and energy efficiency. Nicole works closely with customers and industry partners to translate emerging requirements into scalable packaging solutions, supporting applications across AI, automotive, and high-performance computing. She is actively involved in advancing packaging strategies that push the limits of thermal, electrical, and mechanical performance, helping to enable next-generation semiconductor systems

References

Topic Coming Soon

C. Wendeln
R&D Manager
Atotech mks, Berlin, Germany

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References

Pilot-line implementation of advanced die-to-wafer integration based on hybrid and fusion bonding processes

S. Bickel
Fraunhofer IZM-ASSID, Moritzburg, Germany

Abstract
Advanced electronic packaging technologies enable next-generation system performance, driven by the increasing demands of AI, high-performance computing (HPC) and heterogeneous system integration. In this context, the APECS pilot line plays a central role in Europe by bridging the gap between research and industrial manufacturing, enabling the transfer of advanced packaging technologies into scalable and production-ready solutions. Fraunhofer IZM-ASSID contributes to this effort by developing and validating core process modules for chiplet integration.

Focusing, on die-to-wafer (D2W) bonding technologies, this work presents a technology-driven evaluation of low-temperature fusion bonding using both TEOS and SiCN as well as hybrid bonding at an interconnect pitch of 10 µm. Die sizes range from 4 mm x 4 mm to 9 mm x 9 mm and their corresponding thickness from 775 µm down to 100 µm. Adressing critical processing challenges such as surface preparation, die handling and bonding yield with respect to high component throughput as well as introducing novel characterization techniques, the study is conducted by Fraunhofer IZM-ASSID in close collaboration with Fraunhofer IMWS.

At first, the results point out the importance of precise process control on 300 mm wafer, paritcularly for dielectric deposition, chemical-mechanical polishing and the cleaning of singulated wafers. From a pilot-line perspective, the bonding yield for a given process is the most important metric. Therefore, densely populated 300 mm wafers were characterized by non-destructive methods. Only bonding areas exhibiting no detectable voids were considered for yield analysis. While bonding yields beyond 95% are obtainable using 4 mm dies for a given process-of-record (POR) flow, they drop distinctly in case of larger dies, thus requiring extensive adjustments and optimization, respectively.

The presented work provides a significant contribution to the development and qualification of high-throughput fine-pitch D2W bonding processes as a key enabling technology for chiplet integration within the APECS pilot line framework.

Biography
Steffen Bickel received a diploma degree in materials science in 2011 and a PhD degree in electrical engineering in 2025, both from TU Dresden. In 2021, he joined Fraunhofer IZM-ASSID and currently manages research projects to further develop wafer level packaging technologies for quantum computing applications and bonding technologies for heterogeneous chiplet integration.

References

J. de Koning Gans
Business Development Director
Cosmic Services, Stuttgart, Germany

Biography
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References

Does the Most Advanced Packaging Require the Most Advanced Metrology

E. OToole
R&D Director
Amkor Technology Portugal, Research and Development, Porto, Portugal

Abstract
The cutting edge of advanced packaging includes tens of stacked memory dies with intricate wire bond connectors as the top layer of a Package on Package solution for an application processor (for example). The application processor will likely have fine pitch micropillars for a flip chip connection to a multilayer RDL interposer. The RDL interposer can have line width and line space features down to single digit microns, requiring organic CMP processing to achieve the necessary interlayer coplanarity. The question remains as to whether the most advanced metrology solutions are required to control such an advanced process. This presentation aims to answer that question.

Biography
Eoin OToole is a the R&D director of Amkor Technology Portugal
Originally from Dublin Ireland where he obtained his primary and master degrees in material science from Trinity College Dublin.

References

Coming Soon

C. Ossmann
VP & COO
ACCRETECH GmbH, Munich, Germany

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References

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J. Malin
Director of Product Marketing for Software Solutions
Comet, Hamburg, Germany

Abstract
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Biography
Joscha Malin is the Director of Product Marketing for Software Solutions at the Systems Division of Comet that specializes in supplying X-ray and CT inspection solutions with a particular focus on the Semiconductor R&D and production sectors. In his role, Joscha oversees the division's software product portfolio, with the goal to enhance customer productivity by automation and empower them by data-driven insights derived from X-ray and CT image data. Joscha started his career with an Engineering diploma in Microelectronics from the Technical University Hamburg-Harburg. Over the years, he has worked in multiple roles within R&D in Semiconductor frontend design and system architecture, and within product management, with a consistent focus on image processing solutions.

References

High-Speed AFM Metrology for Advanced Packaging: Enabling High-Yield Hybrid Bonding at Sub-Micron Pitch

D. Haspel
Infinitesima, Abingdon, United Kingdom

Abstract
Advanced packaging has become a primary driver of semiconductor performance, with hybrid wafer bonding emerging as the key enabler of 3D integration. As bonding pitches scale toward sub-1-micron dimensions, the process window tightens: copper pad recess, dielectric roughness, and wafer-scale flatness must all be controlled simultaneously to achieve void-free, high-yield bonding interfaces. This creates a metrology “blind spot” – the need to capture sub-nanometre roughness and millimetre-scale topography across an entire wafer without sacrificing high-volume manufacturing (HVM) throughput.

Atomic Force Microscopy (AFM) has long been the gold standard for 3D surface resolution, but its historic speed constraints have confined it to R&D. This paper presents a paradigm shift in in-line process control using the Metron®3D, a hybrid optical-AFM system. Combined with a high-speed wafer stage and surface detection, it enables dense sampling across full 300 mm wafers at speeds compatible with mass production – measuring copper pad recess with picometre repeatability at throughputs exceeding 60 wafers per hour under standard sampling plans.

We demonstrate that a single high-speed AFM platform can deliver comprehensive, multi-scale characterisation – from local copper dishing and dielectric roughness to macro-scale wafer topography – at sub-nanometre precision. This makes it ideally suited to pre-bonding characterisation of post-CMP wafers, ensuring interfaces meet the stringent requirements for high yield hybrid bonding. Results from a 3D integration development partner will be presented, proving that the multi-scale data density of high-speed AFM is essential to securing bonding interfaces in advanced semiconductor manufacturing.

By moving AFM out of the R&D lab and onto the production line, this approach closes the metrology gap that today constrains hybrid-bonding yield – accelerating the cost-effective scaling of 3D-integrated devices for the AI and high-performance-computing era.

Biography
Dan Haspel is Product Manager at Infinitesima Limited, the UK company behind Rapid Probe Microscopy (RPM) — a breakthrough nanoscale metrology technology enabling true 3D imaging for next-generation semiconductor manufacturing.

With a PhD in Materials Science from Loughborough University and a background spanning Oxford Instruments and academic research, Dan brings together deep technical knowledge and commercial expertise to drive Infinitesima's product strategy. He works closely with semiconductor manufacturers, research institutions, and industry partners to translate cutting-edge science into real-world solutions.

Dan is passionate about bridging the gap between complex technology and the people who use it — from advanced metrology to the practical adoption of modern digital tools within high-tech organisations.

References

A. Grassmann
Vice President
Infineon Technologies, Bavaria, Germany

Biography
Coming Soon

References

We power AI from grid to core

A. Kessler
Senior Principal Engineer Package Concepts
Infineon Technologies, Regensburg, Germany

Abstract
We are all part of a technological revolution driven by AI, which is gaining momentum unpredictably. AI not only has the potential to significantly change our daily lives through digital assistants, financial services or programming new ways, but it also transforms and reshapes every part of the computing market. The heart of this transformation is the enormous power requirement of AI technologies.

To meet accelerating AI compute demand, next generation processors will need 2–4 kW per GPU, pushing rack power toward 1 MW+ by 2030. Increasing GPU cluster densities demands new power architecture designs that boost efficiency, thermal performance, and power delivery density while ensuring high reliability.

Today's AI racks use 1-phase PSUs to create a 50 V bus that is distributed to the compute trays and will support up to 250kW rack power. IBCs and high-density DC-DC stages supply <1 V GPU core power, making optimized conversion essential as currents rise into the thousands of amps.

Electricity and cooling are the major lever affecting GPU infrastructure TCO, often more impactful than minor differences in hardware acquisition costs. Even a seemingly small efficiency drop in a large GPU cluster translates to substantial financial impact. A reduction in cooling costs can be achieved not only through high efficiency but also through effective cooling due to a low Rth of the components.

This talk presents the path from grid to core for powering AI with focus on DC-DC power modules and their thermal management.

Biography
Angela Kessler has been with Infineon Technologies AG since 2000. After completing her diploma in Chemistry in Göttingen, she received her PhD in Physical Chemistry at the University of Regensburg. She has worked in package development for Power and Sensor Systems, Automotive, and Green Industrial Power divisions. Her current focus is on concepts for energy-efficient packages with high power densities, for power delivery from the grid to the processor core for AI and data centers.

References

Co-Designed and Co-Packaged Thermal Solutions for Advanced Semiconductor Packaging

H. A. Martin
Research Scientist
Netherlands Organization for Applied Scientific Research (TNO), Chip Integration Technology Center (CITC), Nijmegen, The Netherlands

Abstract

Wide-Bandgap (WBG) power semiconductors, such as Silicon Carbide (SiC) MOSFETs, Schottky diodes, and Gallium Nitride (GaN) transistors, are widely adopted in electric vehicles for power conversion and inversion. While traditional surface-mount package architectures feature a thermal metal slug on the PCB side, the industry is quickly shifting towards Top-Side Cooling (TSC) and Dual-Side Cooling (DSC) layouts to bypass the thermal bottlenecks of conventional circuit boards. Some prominent examples of surface-mount top-side cooled SiC MOSFETs are STMicroelectronics' HU3PAK™ and the standardized QDPAK platform adopted by Bosch, Infineon, and Nexperia.

However, TSC and DSC platforms still rely on external liquid-cooled heatsinks, complex Thermal Interface Material (TIM) management, and substantial coolant volumes. In contrast, the ACEPACK™ DRIVE power module from STMicroelectronics integrates liquid cooling directly onto the pin-fin baseplate structure, achieving a very low junction-to-fluid thermal resistance of 0.1 K/W. This cooling-integrated power module highlights the industry's critical point, which is the need to move beyond conventional heatsink-based cooling approaches and adopt thermal management as an integral co-designed element of the package architecture.

This presentation introduces a portfolio of co-designed and co-packaged thermal technologies currently under development at CITC (part of TNO). Thermal management is a multi-domain challenge governed by device architecture, power density, and transient operational characteristics, with different classes of electronic systems exhibiting fundamentally distinct thermal behaviors.

Four complementary integrated thermal solution classes will be presented:
1. Thermal Spreading: For devices suffering from highly localized hotspots and steep thermal gradients, advanced thermal spreaders based on diamond and Cu-diamond composites are being integrated to redistribute heat spatially before it reaches the cooling interface.
2. Thermal Dissipation: For systems operating at extreme power densities, near-chip microfluidic cooling architectures are being integrated directly within the package to enable efficient heat extraction while minimizing coolant consumption.
3. Thermal Regulation: For transient and pulsed workloads, Phase Change Materials (PCM) based thermal buffers are being investigated to temporarily absorb thermal peaks and reduce temperature swings.
4. Adaptive Thermal Dissipation: Finally, adaptive thermal dissipation concepts based on shape-change materials are being explored to dynamically regulate cooling performance and coolant flow in response to changing thermal loads.

The presentation will provide an overview of integration strategies, packaging architectures, and application spaces associated with each technology, illustrating how thermal spreading, heat removal, thermal buffering, and adaptive cooling can be combined to address the increasingly diverse thermal requirements of next-generation semiconductor packages.

Ultimately, this work provides attendees with a practical framework for selecting and co-designing thermal solutions based on power density, hotspot characteristics, and transient operating conditions.

Biography

Henry A. Martin is a Research Scientist at the Chip Integration Technology Center (CITC), which is part of the Netherlands Organization for Applied Scientific Research (TNO).
He holds an MSc in Mechanical Engineering from Eindhoven University of Technology (TU/e) and a PhD in Electrical Engineering from Delft University of Technology (TU Delft).
His research focuses on heterogeneous integration, advanced packaging, and integrated thermal

management.

References

J. Lopez
Sr Manager & Sr Expert : Semiconductor Packaging
STMicroelectronics, Grenoble, France

Biography
Coming Soon

References

How to enable ‘semiconductorization’ of photonic chip packaging ?

S. Dorrestein
Program Manager Integrated Photonics
PITC, Photonics Integration Technology Center,
Nijmegen, The Netherlands

Abstract
The photonics industry has successfully demonstrated the performance potential of photonic integrated circuits. Today, however, the challenge is no longer the chip itself. It is how to package, connect, and manufacture photonic systems at the scale demanded by emerging AI and data-centric applications.

This keynote examines how advanced packaging technologies can transform photonics from a specialized technology into a mainstream manufacturing platform. Drawing inspiration from the semiconductor industry, new approaches based on interposers, redistribution layers, panel-level processing, and pluggable optical interfaces are enabling a step change in scalability, performance, and cost.

This keynote talk will present a vision for highly manufacturable photonic systems where optical and electrical interconnections are integrated into modular packaging platforms, dramatically reducing assembly complexity while enabling high-density integration. Key developments in low-loss optical coupling and semiconductor-compatible assembly approaches will be highlighted, together with their implications for future co-packaged optics.

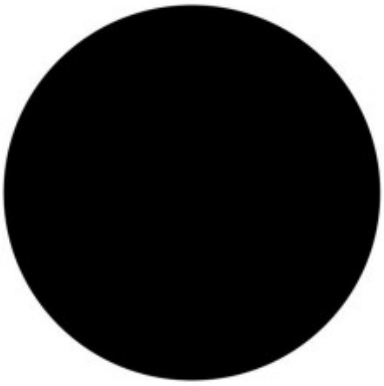
As the industry moves from innovation to industrialization, packaging will define the pace of photonics adoption. This keynote explores why packaging has become the critical enabler for the next generation of photonic products and systems.

Biography
Sander is Program Manager Integrated Photoncis at PITC - Photonics Integration Technology Center (part of TNO) based in The Netherlands. Sander has a Bachelor degree in mechanical engineering, with special interest and broad experience in bonding and joining applications in both micro-electrical and micro-optical packaging.
Sander has a proven track record of developing bonding and joining processes which are currently used in production for consumer, medical, industrial and automotive applications.

References

The Intersection of Silicon Photonics and Advanced Packaging for AI

D. Choy
Onto Innovation, Berlin, Germany



Abstract
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Biography
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References

Bridging the Gap from Prototype to Production: High-Volume Manufacturing Test and Qualification for Co-Packaged Optics

I. Leventhal
VP of Applied Research & Technology
Advantest America, Inc., San Jose, United States of America

Abstract
Co-Packaged Optics (CPO) enables higher bandwidth density and lower power for AI, HPC, and next-generation data centers by placing optical engines close to advanced compute and networking devices. However, scaling CPO from prototypes to high-volume manufacturing (HVM) requires more than photonic integration and advanced packaging. The main challenge is to build a production-ready test and qualification infrastructure that can handle optical, electrical, thermal, mechanical, and operational requirements with the repeatability and throughput expected in semiconductor manufacturing. Key barriers include reliable optical connectivity at package level, insertion-loss control, polarization preservation, connector wear, contamination sensitivity, precision alignment, external laser delivery, calibration stability, thermal-mechanical integration, serviceability, and long-term reliability. These issues affect both Final Test (FT) and System-Level Test (SLT) and must be solved without compromising automation, changeover efficiency, equipment utilization, or cost of test.
This paper presents a modular platform architecture to address these challenges. It extends existing semiconductor test cells with a dedicated co-packaged interface layer that supports optical routing, laser delivery, calibration, diagnostics, cleaning concepts, and photonic test integration while maintaining compatibility with current handlers, sockets, load boards, and automated test equipment. The platform approach allows different optical engine designs, connector concepts, and production test strategies — such as optical loopback, instrument-assisted characterization, and system-level qualification — to be supported without redesigning the full manufacturing cell.
By combining standardized interfaces, automated calibration, contamination mitigation, serviceable optical paths, and scalable test flows, the proposed architecture provides a practical path from New Product Introduction (NPI) to HVM. It helps manufacturers manage yield, reliability, throughput, and ecosystem interoperability as CPO devices move into production for photonic-enabled AI and HPC systems.

Biography
Ira Leventhal Ira Leventhal is the Vice President of Research & Venture at Advantest America, Inc. He has over 25 years of experience in semiconductor testing, including memory, SoC, wireless device, and system-level test. Ira has led the design and development of multiple generations of ATE systems and holds 15 patents in a variety of test-related technologies. In his current role, Ira is focusing on how state-of-the-art and emerging technologies can be applied to meet the challenging test requirements driven by HPC/AI devices and advanced packaging. Ira is an SBEE graduate of the Massachusetts Institute of Technology.

Preet Paul Singh is Engineering Director, Research & Ventures at Advantest America, where he leads advanced semiconductor test and measurement initiatives for next-generation semiconductor and optical interconnect technologies. Over a career spanning more than two decades, he has led the development and deployment of multiple generations of semiconductor test systems for memory, logic, and system-level test applications.
His experience spans product development and leadership roles at Advantest, Verigy, Agilent Technologies, and Hewlett-Packard. His expertise includes semiconductor test system architecture, high performance compute, instrumentation, and manufacturing test solutions. He currently leads R&D activities focused on packaged silicon photonics and co-packaged optics (CPO), addressing the test challenges of next-generation AI and high-performance computing infrastructure. Preet holds a B.S. in Electrical Engineering and Computer Science from the University of California, Berkeley.

References