Advanced Packing Conference

S. Kröhnert
President & Founder
ESPAT Consulting, Dresden, Germany

Biography
Coming Soon

References

Welcome Remarks

L. Altimime
President
SEMI Europe, Berlin, Germany

Abstract
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Biography
Laith Altimime, as President of SEMI Europe, leads SEMI's activities in Europe and the Middle East and Africa (EMEA). Altimime has P&L responsibility as well as ownership of all Europe region programs and events, including SEMICON Europa. He is responsible for establishing industry standards, advocacy, community development, expositions, and programs. He provides support and services to SEMI members worldwide that have supply chain interests in Europe. He manages and nurtures relationships with SEMI members in the region and globally as well as with local associations and constituents in industry, government, and academia. Altimime has more than 30 years of international experience in the semiconductor industry. Prior to joining SEMI in 2015, He held senior leadership positions at NEC, KLA-Tencor, Infineon, Qimonda, and imec. Altimime holds an MSc from Heriot-Watt University, Scotland.

References

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A. Chichkov
Chips JU, Brussels, Belgium

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References

R. Antonicelli
JCET Group, Laussane, Switzerland

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Coming Soon

References

Heterogeneous Integration for Chiplets for Broad Industrial Applications

B. Han
CEO
Silicon Box, Singapore, Singapore

Abstract
This presentation explores a broad range of applications utilizing chiplet integration. The diversity of these applications poses significant manufacturing challenges, particularly when investment for production variety must be minimized. To address these hurdles, various manufacturing schemes are evaluated, and the current industry consensus is examined. Ultimately, the direction of this technological convergence will provide valuable insights for future investment strategies.

Biography
Dr. BJ Han is the CEO and co-founder of Silicon Box, a forefront semiconductor integration and advanced packaging company. An industry pioneer and inventor with over 300 patents, Dr. Han brings extensive expertise to Silicon Box to address the global shortage in chiplet integration infrastructure. His innovations, including Quad Flat No-Lead (QFN) and Fine-Pitch BGA (FBGA) packages, ship over 100 billion units annually.
Prior to founding Silicon Box, Dr. Han spent 20 years at STATS ChipPAC, serving as Chief Executive Officer and Chairman of the Board. His distinguished 40-year career also includes leadership and research roles at AT&T Bell Labs, IBM Research, and Amkor, as well as consulting with Bain & Company. Recognized globally for his contributions, he was awarded the Leonardo International Prize in 2025 for strategic investments in Italy's technological landscape and named to *Tatler's* Asia's Most Influential list in 2024 and again in 2025. Dr. Han holds a PhD from Columbia University and is an alumnus of the Advanced Management Program (AMP) at Harvard University.

References

Scaling Advanced Packaging: The Wafer-to-Panel Revolution

N. Tien
Senior Technical Program Manager
ASE, Brussels, Belgium

Abstract
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Biography
Nicole Tien is a Senior Technical Program Manager at ASE Europe, where she drives advanced packaging technology development and innovation to support customer growth and ecosystem collaboration. She focuses on high-performance heterogeneous integration, including multi-die and 3D packaging solutions, enabling improved system-level performance, bandwidth, and energy efficiency. Nicole works closely with customers and industry partners to translate emerging requirements into scalable packaging solutions, supporting applications across AI, automotive, and high-performance computing. She is actively involved in advancing packaging strategies that push the limits of thermal, electrical, and mechanical performance, helping to enable next-generation semiconductor systems

References

Pilot-line implementation of advanced die-to-wafer integration based on hybrid and fusion bonding processes

S. Bickel
Fraunhofer IZM-ASSID, Moritzburg, Germany

Abstract
Advanced electronic packaging technologies enable next-generation system performance, driven by the increasing demands of AI, high-performance computing (HPC) and heterogeneous system integration. In this context, the APECS pilot line plays a central role in Europe by bridging the gap between research and industrial manufacturing, enabling the transfer of advanced packaging technologies into scalable and production-ready solutions. Fraunhofer IZM-ASSID contributes to this effort by developing and validating core process modules for chiplet integration.

Focusing, on die-to-wafer (D2W) bonding technologies, this work presents a technology-driven evaluation of low-temperature fusion bonding using both TEOS and SiCN as well as hybrid bonding at an interconnect pitch of 10 µm. Die sizes range from 4 mm x 4 mm to 9 mm x 9 mm and their corresponding thickness from 775 µm down to 100 µm. Adressing critical processing challenges such as surface preparation, die handling and bonding yield with respect to high component throughput as well as introducing novel characterization techniques, the study is conducted by Fraunhofer IZM-ASSID in close collaboration with Fraunhofer IMWS.

At first, the results point out the importance of precise process control on 300 mm wafer, paritcularly for dielectric deposition, chemical-mechanical polishing and the cleaning of singulated wafers. From a pilot-line perspective, the bonding yield for a given process is the most important metric. Therefore, densely populated 300 mm wafers were characterized by non-destructive methods. Only bonding areas exhibiting no detectable voids were considered for yield analysis. While bonding yields beyond 95% are obtainable using 4 mm dies for a given process-of-record (POR) flow, they drop distinctly in case of larger dies, thus requiring extensive adjustments and optimization, respectively.

The presented work provides a significant contribution to the development and qualification of high-throughput fine-pitch D2W bonding processes as a key enabling technology for chiplet integration within the APECS pilot line framework.

Biography
Steffen Bickel received a diploma degree in materials science in 2011 and a PhD degree in electrical engineering in 2025, both from TU Dresden. In 2021, he joined Fraunhofer IZM-ASSID and currently manages research projects to further develop wafer level packaging technologies for quantum computing applications and bonding technologies for heterogeneous chiplet integration.

References

J. de Koning Gans
ROOD Mictrotech, Stuttgart, Germany

Biography
Coming Soon

References

Does the Most Advanced Packaging Require the Most Advanced Metrology

E. OToole
R&D Director
Amkor Technology Portugal, Research and Development, Porto, Portugal

Abstract
The cutting edge of advanced packaging includes tens of stacked memory dies with intricate wire bond connectors as the top layer of a Package on Package solution for an application processor (for example). The application processor will likely have fine pitch micropillars for a flip chip connection to a multilayer RDL interposer. The RDL interposer can have line width and line space features down to single digit microns, requiring organic CMP processing to achieve the necessary interlayer coplanarity. The question remains as to whether the most advanced metrology solutions are required to control such an advanced process. This presentation aims to answer that question.

Biography
Eoin OToole is a the R&D director of Amkor Technology Portugal
Originally from Dublin Ireland where he obtained his primary and master degrees in material science from Trinity College Dublin.

References

Coming Soon

C. Ossmann
VP & COO
ACCRETECH GmbH, Munich, Germany

Abstract
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Biography
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References

High-Speed AFM Metrology for Advanced Packaging: Enabling High-Yield Hybrid Bonding at Sub-Micron Pitch

D. Haspel
Infinitesima, Abingdon, United Kingdom

Abstract
Advanced packaging has become a primary driver of semiconductor performance, with hybrid wafer bonding emerging as the key enabler of 3D integration. As bonding pitches scale toward sub-1-micron dimensions, the process window tightens: copper pad recess, dielectric roughness, and wafer-scale flatness must all be controlled simultaneously to achieve void-free, high-yield bonding interfaces. This creates a metrology “blind spot” – the need to capture sub-nanometre roughness and millimetre-scale topography across an entire wafer without sacrificing high-volume manufacturing (HVM) throughput.

Atomic Force Microscopy (AFM) has long been the gold standard for 3D surface resolution, but its historic speed constraints have confined it to R&D. This paper presents a paradigm shift in in-line process control using the Metron®3D, a hybrid optical-AFM system. Combined with a high-speed wafer stage and surface detection, it enables dense sampling across full 300 mm wafers at speeds compatible with mass production – measuring copper pad recess with picometre repeatability at throughputs exceeding 60 wafers per hour under standard sampling plans.

We demonstrate that a single high-speed AFM platform can deliver comprehensive, multi-scale characterisation – from local copper dishing and dielectric roughness to macro-scale wafer topography – at sub-nanometre precision. This makes it ideally suited to pre-bonding characterisation of post-CMP wafers, ensuring interfaces meet the stringent requirements for high yield hybrid bonding. Results from a 3D integration development partner will be presented, proving that the multi-scale data density of high-speed AFM is essential to securing bonding interfaces in advanced semiconductor manufacturing.

By moving AFM out of the R&D lab and onto the production line, this approach closes the metrology gap that today constrains hybrid-bonding yield – accelerating the cost-effective scaling of 3D-integrated devices for the AI and high-performance-computing era.

Biography
Dan Haspel is Product Manager at Infinitesima Limited, the UK company behind Rapid Probe Microscopy (RPM) — a breakthrough nanoscale metrology technology enabling true 3D imaging for next-generation semiconductor manufacturing.

With a PhD in Materials Science from Loughborough University and a background spanning Oxford Instruments and academic research, Dan brings together deep technical knowledge and commercial expertise to drive Infinitesima's product strategy. He works closely with semiconductor manufacturers, research institutions, and industry partners to translate cutting-edge science into real-world solutions.

Dan is passionate about bridging the gap between complex technology and the people who use it — from advanced metrology to the practical adoption of modern digital tools within high-tech organisations.

References

A. Grassmann
Vice President
Infineon Technologies, Bavaria, Germany

Biography
Coming Soon

References

We power AI from grid to core

A. Kessler
Senior Principal Engineer Package Concepts
Infineon Technologies, Regensburg, Germany

Abstract
We are all part of a technological revolution driven by AI, which is gaining momentum unpredictably. AI not only has the potential to significantly change our daily lives through digital assistants, financial services or programming new ways, but it also transforms and reshapes every part of the computing market. The heart of this transformation is the enormous power requirement of AI technologies.

To meet accelerating AI compute demand, next generation processors will need 2–4 kW per GPU, pushing rack power toward 1 MW+ by 2030. Increasing GPU cluster densities demands new power architecture designs that boost efficiency, thermal performance, and power delivery density while ensuring high reliability.

Today's AI racks use 1-phase PSUs to create a 50 V bus that is distributed to the compute trays and will support up to 250kW rack power. IBCs and high-density DC-DC stages supply <1 V GPU core power, making optimized conversion essential as currents rise into the thousands of amps.

Electricity and cooling are the major lever affecting GPU infrastructure TCO, often more impactful than minor differences in hardware acquisition costs. Even a seemingly small efficiency drop in a large GPU cluster translates to substantial financial impact. A reduction in cooling costs can be achieved not only through high efficiency but also through effective cooling due to a low Rth of the components.

This talk presents the path from grid to core for powering AI with focus on DC-DC power modules and their thermal management.

Biography
Angela Kessler has been with Infineon Technologies AG since 2000. After completing her diploma in Chemistry in Göttingen, she received her PhD in Physical Chemistry at the University of Regensburg. She has worked in package development for Power and Sensor Systems, Automotive, and Green Industrial Power divisions. Her current focus is on concepts for energy-efficient packages with high power densities, for power delivery from the grid to the processor core for AI and data centers.

References

Co-Designed and Co-Packaged Thermal Solutions for Advanced Semiconductor Packaging

H. A. Martin
Research Scientist
Netherlands Organization for Applied Scientific Research (TNO), Chip Integration Technology Center (CITC), Nijmegen, The Netherlands

Abstract

Wide-Bandgap (WBG) power semiconductors, such as Silicon Carbide (SiC) MOSFETs, Schottky diodes, and Gallium Nitride (GaN) transistors, are widely adopted in electric vehicles for power conversion and inversion. While traditional surface-mount package architectures feature a thermal metal slug on the PCB side, the industry is quickly shifting towards Top-Side Cooling (TSC) and Dual-Side Cooling (DSC) layouts to bypass the thermal bottlenecks of conventional circuit boards. Some prominent examples of surface-mount top-side cooled SiC MOSFETs are STMicroelectronics' HU3PAK™ and the standardized QDPAK platform adopted by Bosch, Infineon, and Nexperia.

However, TSC and DSC platforms still rely on external liquid-cooled heatsinks, complex Thermal Interface Material (TIM) management, and substantial coolant volumes. In contrast, the ACEPACK™ DRIVE power module from STMicroelectronics integrates liquid cooling directly onto the pin-fin baseplate structure, achieving a very low junction-to-fluid thermal resistance of 0.1 K/W. This cooling-integrated power module highlights the industry's critical point, which is the need to move beyond conventional heatsink-based cooling approaches and adopt thermal management as an integral co-designed element of the package architecture.

This presentation introduces a portfolio of co-designed and co-packaged thermal technologies currently under development at CITC (part of TNO). Thermal management is a multi-domain challenge governed by device architecture, power density, and transient operational characteristics, with different classes of electronic systems exhibiting fundamentally distinct thermal behaviors.

Four complementary integrated thermal solution classes will be presented:
1. Thermal Spreading: For devices suffering from highly localized hotspots and steep thermal gradients, advanced thermal spreaders based on diamond and Cu-diamond composites are being integrated to redistribute heat spatially before it reaches the cooling interface.
2. Thermal Dissipation: For systems operating at extreme power densities, near-chip microfluidic cooling architectures are being integrated directly within the package to enable efficient heat extraction while minimizing coolant consumption.
3. Thermal Regulation: For transient and pulsed workloads, Phase Change Materials (PCM) based thermal buffers are being investigated to temporarily absorb thermal peaks and reduce temperature swings.
4. Adaptive Thermal Dissipation: Finally, adaptive thermal dissipation concepts based on shape-change materials are being explored to dynamically regulate cooling performance and coolant flow in response to changing thermal loads.

The presentation will provide an overview of integration strategies, packaging architectures, and application spaces associated with each technology, illustrating how thermal spreading, heat removal, thermal buffering, and adaptive cooling can be combined to address the increasingly diverse thermal requirements of next-generation semiconductor packages.

Ultimately, this work provides attendees with a practical framework for selecting and co-designing thermal solutions based on power density, hotspot characteristics, and transient operating conditions.

Biography

Henry A. Martin is a Research Scientist at the Chip Integration Technology Center (CITC), which is part of the Netherlands Organization for Applied Scientific Research (TNO).
He holds an MSc in Mechanical Engineering from Eindhoven University of Technology (TU/e) and a PhD in Electrical Engineering from Delft University of Technology (TU Delft).
His research focuses on heterogeneous integration, advanced packaging, and integrated thermal

management.

References

J. Lopez
Sr Manager & Sr Expert : Semiconductor Packaging
STMicroelectronics, Grenoble, France

Biography
Coming Soon

References

How to enable ‘semiconductorization’ of photonic chip packaging ?

S. Dorrestein
Program Manager Integrated Photonics
PITC, Photonics Integration Technology Center,
Nijmegen, The Netherlands

Abstract
The photonics industry has successfully demonstrated the performance potential of photonic integrated circuits. Today, however, the challenge is no longer the chip itself. It is how to package, connect, and manufacture photonic systems at the scale demanded by emerging AI and data-centric applications.

This keynote examines how advanced packaging technologies can transform photonics from a specialized technology into a mainstream manufacturing platform. Drawing inspiration from the semiconductor industry, new approaches based on interposers, redistribution layers, panel-level processing, and pluggable optical interfaces are enabling a step change in scalability, performance, and cost.

This keynote talk will present a vision for highly manufacturable photonic systems where optical and electrical interconnections are integrated into modular packaging platforms, dramatically reducing assembly complexity while enabling high-density integration. Key developments in low-loss optical coupling and semiconductor-compatible assembly approaches will be highlighted, together with their implications for future co-packaged optics.

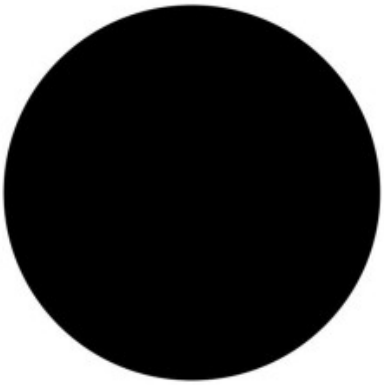
As the industry moves from innovation to industrialization, packaging will define the pace of photonics adoption. This keynote explores why packaging has become the critical enabler for the next generation of photonic products and systems.

Biography
Sander is Program Manager Integrated Photoncis at PITC - Photonics Integration Technology Center (part of TNO) based in The Netherlands. Sander has a Bachelor degree in mechanical engineering, with special interest and broad experience in bonding and joining applications in both micro-electrical and micro-optical packaging.
Sander has a proven track record of developing bonding and joining processes which are currently used in production for consumer, medical, industrial and automotive applications.

References

Coming Soon

D. Choy
Onto Innovation, Berlin, Germany



Abstract
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Biography
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References

Bridging the Gap from Prototype to Production: High-Volume Manufacturing Test and Qualification for Co-Packaged Optics

I. Leventhal
VP of Applied Research & Technology
Advantest America, Inc., San Jose, United States of America

Abstract
Co-Packaged Optics (CPO) enables higher bandwidth density and lower power for AI, HPC, and next-generation data centers by placing optical engines close to advanced compute and networking devices. However, scaling CPO from prototypes to high-volume manufacturing (HVM) requires more than photonic integration and advanced packaging. The main challenge is to build a production-ready test and qualification infrastructure that can handle optical, electrical, thermal, mechanical, and operational requirements with the repeatability and throughput expected in semiconductor manufacturing. Key barriers include reliable optical connectivity at package level, insertion-loss control, polarization preservation, connector wear, contamination sensitivity, precision alignment, external laser delivery, calibration stability, thermal-mechanical integration, serviceability, and long-term reliability. These issues affect both Final Test (FT) and System-Level Test (SLT) and must be solved without compromising automation, changeover efficiency, equipment utilization, or cost of test.
This paper presents a modular platform architecture to address these challenges. It extends existing semiconductor test cells with a dedicated co-packaged interface layer that supports optical routing, laser delivery, calibration, diagnostics, cleaning concepts, and photonic test integration while maintaining compatibility with current handlers, sockets, load boards, and automated test equipment. The platform approach allows different optical engine designs, connector concepts, and production test strategies — such as optical loopback, instrument-assisted characterization, and system-level qualification — to be supported without redesigning the full manufacturing cell.
By combining standardized interfaces, automated calibration, contamination mitigation, serviceable optical paths, and scalable test flows, the proposed architecture provides a practical path from New Product Introduction (NPI) to HVM. It helps manufacturers manage yield, reliability, throughput, and ecosystem interoperability as CPO devices move into production for photonic-enabled AI and HPC systems.

Biography
Ira Leventhal Ira Leventhal is the Vice President of Research & Venture at Advantest America, Inc. He has over 25 years of experience in semiconductor testing, including memory, SoC, wireless device, and system-level test. Ira has led the design and development of multiple generations of ATE systems and holds 15 patents in a variety of test-related technologies. In his current role, Ira is focusing on how state-of-the-art and emerging technologies can be applied to meet the challenging test requirements driven by HPC/AI devices and advanced packaging. Ira is an SBEE graduate of the Massachusetts Institute of Technology.

Preet Paul Singh is Engineering Director, Research & Ventures at Advantest America, where he leads advanced semiconductor test and measurement initiatives for next-generation semiconductor and optical interconnect technologies. Over a career spanning more than two decades, he has led the development and deployment of multiple generations of semiconductor test systems for memory, logic, and system-level test applications.
His experience spans product development and leadership roles at Advantest, Verigy, Agilent Technologies, and Hewlett-Packard. His expertise includes semiconductor test system architecture, high performance compute, instrumentation, and manufacturing test solutions. He currently leads R&D activities focused on packaged silicon photonics and co-packaged optics (CPO), addressing the test challenges of next-generation AI and high-performance computing infrastructure. Preet holds a B.S. in Electrical Engineering and Computer Science from the University of California, Berkeley.

References