## 2D (TechARENA)

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**Biography**
Johan Dekoster received the M.S. degree in Exact Sciences (Physics) in 1988 from the KU Leuven, Belgium. In 1993 he received the Ph.D. degree (Physics), also from the KU Leuven. From 1993 till 1999 he held postdoctoral fellowships from the Research Council and the Fund for Scientific Research at the Institute of Nuclear and Radiation Physics of the KU Leuven. In 1999 he joined the OTN business unit of Siemens. He was project leader for several development projects for data, voice, video and LAN. In 2007 he became program manager OTN at Nokia Siemens Networks. In April 2008 he joined IMEC as R&D manager of the Epitaxy group with responsibility on epitaxial deposition of group IV and III-V semiconductor materials. Since November 2012 he is program manager of the equipment and materials suppliers collaborations within the Process Technology Unit at IMEC.

### Epitaxial MoSe2 semiconductor heterostructures on AlN/Si(111) substrates

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**Abstract**
Two dimensional (2D) semiconductors such as transition metal dichalcogenides (TMD) offer ultimate thickness scaling down to the single layer limit for low power versatile nanoelectronics. TMDs have already demonstrated their potential in electronics since generic ICs of the type used in CMOS have been fabricated [1]. However, most of these advancements have been made on small flakes exfoliated from bulk materials. For real world applications, materials must be epitaxially grown in thin film form on large area engineered substrates on silicon to demonstrate a scalable manufacturing. The availability of high quality 300 mm MOCVD grown AlN/Si(111) substrates already developed for III-Nitride lighting and power devices creates the prospect that 2D semiconductor devices and circuits can be manufactured in a Si compatible processing flow for future volume production.
In this work, the first atomically thin MoSe2 layers grown by MBE on AlN(0001)/Si(111) substrates are reported. The growth optimization procedure monitored by electron diffraction, XRD, XPS and HRTEM will be reviewed emphasizing on the influence of the substrate on the physical properties. It will be shown that high quality single crystal MoSe2 can be obtained on nearly lattice matched AlN with abrupt crystalline interfaces. The quality is further improved using epitaxial Bi2Se3 buffer layers despite the large mismatch between the two materials. Using electronic valence band imaging by in-situ ARPES, it is shown that single layer MoSe2 directly deposited on AlN has a direct band gap making it suitable for optoelectronic applications. First results on planar FETs will be presented emphasizing on the immunity to short channel effects in <100 nm devices. Finally, excellent quality multilayer heterostructures of MoSe2 with Bi2Se3 topological insulator and other selenide compounds are grown showing the prospect for novel vertical transport devices.
[1] e.g. B. Radisavljevic et al., ACS Nano 5, 9934 (2011).

**CV of presenting author**
Dr. Dimoulas obtained his Ph.D in Applied Physics from the University of Crete in Greece in 1991 on MBE heteroepitaxial gowth and characterization of GaAs and related compounds on Si. He was Human Capital & Mobility Fellow of the EU at the University of Groningen in Holland until 1994, a Research Fellow at the California Institute of Technology (CALTECH), Chemical Engineering, Pasadena USA until 1996 and Research Associate at the University of Maryland at College Park (UMCP) USA, until February 1999. In addition, he was visiting research scientist at NRL, Washington DC in 1992 and at IBM Zurich Resarch Laboratory, Switzerland in 2006 and 2007. Since 1999, he is Research Director and head of the Epitaxy and Surface Science laboratory at the National Center for Scientific Research DEMOKRITOS, Athens, Greece. He has coordinated several European-funded projects in the areas of advanced CMOS, the last being DUALLOGIC- a flagship CMOS project in FP7 and he is now leading the EU project 2D NANOLATTICES on silicene and other 2D crystal channels for post CMOS applications. Also, he has received the prestigious ERC (IDEAS) 2011 Advanced Investigator Grant -SMARTATE on smart gates for "green" electronics and the Greek Excellence (ARISTEIA) project TOP-ELECTRONICS. He has authored or co-authored more than 120 technical presentations in refereed journals including 3 monographs in Springer book chapters on high-k gates on Si and high mobility channels. In addition, he has more than 70 presentations in conferences including 30 invited in conferences, tutorials and summer schools. He has more than 2000 citations and an h-index of 27. He is co-editor in a Springer book and guest editor in three special volumes of international journals. He has organized MRS and E-MRS symposia in 2005, 2003, 2009, 2010 and 2013. He was the general chair of INFOS 2007 conference and he is in the steering committee of INFOS and ESSDERC/ESSCIRC conferences and he has chaired the TPC committee of ESSDERC/ESSCIRC 2007 and the IEDM 2012 Process Technology subcommittee. His expertise includes MBE growth of semiconductors and dielectric materials, VCD growth of graphene, nanodevice processing by optical and e-beam lithography materials structural and physical characterization & device electrical characterization.

## What can we expect from two-dimensional materials for electronic applications? A simulation study

G. Fiori
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**Abstract**
Research community has great expectations towards two-dimensional materials, since they could be the option for ultimately scaled devices. Many issues however still remain open due to the embryonic stage of nowadays fabrication technology. Computer simulations can represent a powerful tool in order to predict the real performance of two-dimensional material, giving useful hints on the solutions to be discarded as well as those to bet on.
Here we provide an overview of state-of-the-art devices, showing which solutions are in our opinion the most promising, as well as those which we believe will never comply with Industry requirements. In particular, attention will be posed on vertical and lateral heterostructures, as well as bilayer graphene based devices for both digital and analog applications.
An overview on energy applications will be provided as well, showing that graphene can represent a viable option for transparent electrode and a valid substitute for Indium Thin Oxide contact in organic solar cells.

**CV of presenting author**
Gianluca Fiori is an Assistant Professor at the University of Pisa. His main field of activity includes the development of models and codes for the simulation of CMOS transistors with ultra-short channel and innovative devices based on new architectures and new materials. In particular, at the beginning he focused his attention on quantum confinement, short channel effects and the random distribution of dopants in Silicon

MOSFETs: part of these models have been included into the commercial device simulator ATLAS, within a collaboration, in Autumn 2002, with Silvaco International, one of the worldwide leading developers and vendors of Technology Computer Aided Design (TCAD) software dedicated to Process and Device Simulation. Due to the increased interest in carbon electronics, Dr. Fiori has focused his attention on carbon based devices, through repeated research visits (in 2004, 2005 and 2008) at the Network for Computational Nanotechnology, at Purdue University, (IN-USA). Within these activities, he has developed codes based on semi-empirical tight binding Hamiltonians and the Non-Equilibrium Green's Function Formalism (NEGF). Dr. Fiori has recently released, under the BSD open-source license, the in-house developed code NanoTCAD ViDES (http://vides.nanotcad.com), which includes most of the physical models implemented during his research activity.

## 2D materials : From Advanced CMOS to Beyond CMOS devices

C. Huyghebaert
R&D team leader
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**Abstract**
The information infrastructure is growing and becoming ubiquitous around us. Continuous connectivity, which we take for granted now, did not exist 10 years ago. This growth has been largely fueled by the scaling of the transistors which has allowed increased performance for comparable energy consumption and lower cost. Continuing growth further will demand a variety of electronic systems with different performance and energy efficiency requirements to satisfy a large set of functionality and cost needs.

Early on, the scaling of the transistors was driven by the lithographic improvements. More recently, the scaling is that of the performance and relies on new materials (high K dielectrics and metal gates) and on devices structure innovations (fully-depleted channel devices). The performance scaling of the next decade will likely bring concerted changes not only at the transistor level but also at the interconnect and at the architecture level as the 3rd dimension will be conquered.

The pace of innovation will likely continue further as it is driven by technological needs. The scaling of the transistor will be influenced by fundamental physical limits of device switching.

At imec, we are a investigating not only advanced CMOS devices and "end of the roadmap" transistors, but also Beyond CMOS devices which rely on advanced materials like graphene and 2D semiconductors but also devices that employ a different state variable. This talk will outline the research on the 2D materials family.

Imec has been carrying out endeavors whose main focus is to provide an answer to the question of whether the family of 2D materials could really hold the promises for a successful use in microelectronics. This is being accomplished with a strategy encompassing two main aspects of research: (1)to evaluate novel device concepts based on the fundamental properties of 2D materials (2) to work towards industrial compatible solutions for 2D material integration in a semiconductor environment.

**CV of presenting author**
**Cedric Huyghebaert** is currently leading the nano-applications and material engineering team at imec dealing with the integration of nano materials as CNT, nanowires,graphene and MoS2 in functional applications, in the field of beyond Si scaling, advanced interconnect and energy storage applications.
He started as a junior researcher in the materials and component analyses group at imec. He studied the oxygen bean interactions during sputtering profiling of semiconductors. He received his PhD in Physics in 2006 at the KULeuven in Belgium. In 2005 he joined imecs pilot line management team, especially dealing with integration challenges and the process contamination control. In 2008 he joined the 3D integration team to organize the migration of the 3D technology from a lab environment to the a pilot line. He was the lead integration engineer of the first demonstration of 3D TSV interconnects by wafer to wafer bonding.

## Scaling up Chemical Vapour Deposition Graphene to 300 mm Si substrates

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**Abstract**
Graphene is a 2D carbon material with unique properties such as high mobility, wideband optical transparency and large thermal conductivity. To make use of these characteristics in high performance electronic applications, it is necessary to grow and integrate graphene using modern Si chip manufacturing processes. This paper discusses the growth of graphene by Chemical Vapour Deposition. The synthesis process begins with the deposition and crystallization of a nucleation layer, namely thin film Cu. We study the characteristics of this Cu film and the subsequent graphene growth kinetics and formation. Once Graphene is produced, it is transferred from the Cu film to the target substrate using a variety of integration techniques such as polymer-based or electrolytic transfer.

Monolayer Graphene on Si or Cu/Si wafers are commercially available in sizes up to 100mm and are typically used to develop and characterise graphene device performance. There are currently only few organizations able to produce high quality monolayer graphene on wafer in sizes exceeding 100mm in diameter. To enable the commercialization of graphene as a large scale product, significant and successive cost reduction must be achieved. Here, we report the development of CVD tools in both scaling up the CVD production of graphene from 100mm to 300mm wafers but also report the increase in throughput from 1x100mm wafer in 2 hours to 2x300mm wafer in under 1 hour.

**CV of presenting author**
Dr Alex Jouvray received his PhD in CFD from Warwick University in 2004. He is currently the Engineering Project Leader for Aixtron's NanoInstruments products. He has significant experience of managing the development of new products and systems for a range of industial and scientific applications. He has managed several publicly funded projects and is the author / co-author of sevral papers and patents.

## Single-Layer MoS2 - 2D Devices, Circuits and Heterostructures

A. Kis
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**Abstract**
Single-layer molybdenum disulphide (MoS2), a direct-gap semiconductor is a typical example of new graphene-like materials that can be produced using the adhesive-tape based cleavage technique originally developed for graphene. The presence of a band gap in MoS2 allowed us to fabricate transistors that can be turned off and operate with negligible leakage currents [1]. Furthermore, our transistors can be used to build simple integrated circuits capable of performing logic operations and amplifying small signals [2] [3].

We have also successfully integrated graphene with MoS2 into heterostructures to form flash memory cells [5] that could be used to extend the scaling of this type of devices. Next, I will show photodetector devices based on MoS2 that have a sensitivity surpassing that of similar graphene devices by several orders of magnitude. Incorporating MoS2 in van der Waals heterostructures can open the way to an extremely diverse

range of materials where different layers cam be mixed and matched to different functionalities. This is not only limited to two-dimensional materials: classical 3D semiconductors with saturated dangling bonds can also be integrated with 2D semiconductors, as I will show on the example of p-Si/n-MoS2 heterostructures that behave as diodes and can be used to achieve light emission and energy harvesting in a broad energy range [6].

[1] B. Radisavljevic et al., Nat. Nanotechnol. 6, 147 (2011).
[2] B. Radisavljevic, M. B. Whitwick and A. Kis, ACS Nano 5, 9934 (2011).
[3] B. Radisavljevic, M. B. Whitwick and A. Kis, Appl. Phys. Lett. 101, 043103 (2012).
[4] B. Radisavljevic and A. Kis, Nat. Mater. 12, 815 (2013).
[5] S. Bertolazzi, D. Krasnozhon and A. Kis, ACS Nano 7, 3246 (2013).
[6] O. Lopez-Sanchez et al., ACS Nano (2014).

**CV of presenting author**

Prof. Andras Kis was born in 1975 in Croatia where he finished his undergraduate studies in physics in 1999 at the University of Zagreb. In 2000, he moved to Switzerland where he obtained his PhD (Physics) in 2003. In 2004 he was awarded the prestigious Latsis Universiy prize for his PhD work. From 2004 to 2007 he was a postdoctoral researcher at the University of California, Berkeley in the group of Prof. Zettl. At Berkeley he studied electrical and mechanical properties of carbon and boron nitride nanotubes and gained experience in microfabrication techniques at the Berkeley Microlab. In 2007 he returned to Switzerland and joined the Electrical Engineering Institute at EPFL and formed a research group as a tenure track Assistant Professor. Andras Kis and his group study electrical properties of low-dimensional materials such as 2d transition metal dichalcogenides. In 2009, Andras Kis was awarded the ERC starting grant (1.8 million Euros) for a research project (acronym FLATRONICS) in the area of electrical properties of dichalcogenide nanolayers.

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