EU Projects

Development and manufacturing of Co-Packaged optics demonstrator on IC Substrate technology for the beyond state-of-the-art smart NICs and Switches

G. Park
Advanced Technologies and Solutions, Research and Development, Leoben, Austria

Abstract
As artificial intelligence, machine learning, and big data workloads have explosive growth, the demand for high-performance infrastructure as hyperscale data centre is pushing the limits. HiConnects is aiming to support industrial challenges by developing heterogenous integration core technology solution for energy-efficient and high-performance cloud and edge computing.
In a subtask 3.3.2, we focused on the development of a co-packaged optics demonstrator based on the specifications of NVIDIA and the photonic components development in the pilot line. Specifically, the defined design will be delivered from NVIDIA after specifications of the envisioned product requirements for co-packaged optics NIC and switch. According to the design, AT&S will provide the proper solution on Integrated Circuit Substrate (ICS) or PCB with considering system levels needs. In addition, the simulation of heat spreading and mechanical stability (warpage) will be executed by considering different material parameters such as CTE, thermal and electrical conductivity, dielectric constant, and dissipation factor, respectively. PHIX will provide optimized interconnect solution and assemble the Silicon Photonics Transceiver interposer developed by IMEC, network chip, and driver ICs on the ICS. Thermosonic flip-chip bonding technique will be used where Gold micro bumping will be applied either on the ICS or chips. The micro-optical lenses from Teramount will be bonded on the SiPh transceiver chip and Fiber Connector will be attached accordingly. Finally, a functional testing of fully co-packaged optics demonstrator will be done by NVIDIA.
In this work, we investigated the test vehicle in order to achieve the working demonstrator at the end of HiConnects project. The progress for the test vehicle preparation and output from the project will be presented in this talk. In addition, we will outline a perspective supply chain for co-packaged optics in smart NICs and switches.

Biography
Gyuhyeon Park obtained his Doctor of Engineer (Dr.-Ing) in Mechanical Science and Engineer from the Technical University of Dresden, Germany in 2021. He continued his research at Leibnitz Institute for Solid State and Materials Research (IFW-Dresden) as post-doctor in Dresden, Germany in 2023. His research focused on the fabrication of micro-sized device with thin film of magneto-thermo-electric quantum material. After he join Advanced Technologies and Solutions (AT&S), Austria, now he is focusing on the Optical Communication in the R&D department as Project Manager and delivering successful projects across various industries.

References

Integration and Assembly of Co-Packaged Optics (CPO) for smart Networks and Switches

A. Sundararajan
Project Leader - Photonics Packaging
PHIX Photonics Assembly, Enschede, The Netherlands

Abstract

The rapid scaling of data center bandwidth requirements is pushing the limits of traditional pluggable optical modules, leading to the emergence of Co-Packaged Optics (CPO) as a promising solution for next-generation network interface cards (NICs) and switch architectures. This presentation outlines a collaborative workflow and integration scheme for CPO systems, highlighting the step-by-step assembly of photonic integrated circuits (PICs), drivers (EICs), and high-bandwidth fiber optics connectors for smart networking devices. We describe the joint contributions from key industrial and research partners—including Teramount (TM), AT&S, IMEC, PHIX, and NVIDIA—covering substrate design, optical/electronic die integration, and high-precision flip-chip bonding. Emphasis is placed on the alignment precision and thermal stability required for the successful coupling of fiber arrays, drivers (EICs) to PICs. The final packaging steps are optimized for signal integrity and thermal management to enable deployment in high-performance data center environments.

Biography

Anneirudh Sundararajan is a Project Leader at PHIX Photonics Assembly, where he leads several EU-funded initiatives as well as customer-driven projects. He specializes in flip-chip bonding technology and the advanced packaging of photonic integrated circuits (PICs). Prior to joining PHIX, Anneirudh worked in Germany as a Process Development Engineer at a photonic packaging company, gaining hands-on experience in scalable photonic assembly processes. Anneirudh pursued his PhD at the University of Twente, where his research focused on the integration of optical components with MEMS-based microfluidic systems. His work involved the development of Coriolis mass flow sensors and spectroscopic techniques for multiparameter fluid characterization. With a strong interdisciplinary background in optics, microfluidics, and photonic packaging, he is actively contributing to the development of next-generation photonic sensing platforms.

References