

EU Projects

Towards Quantum-Ready End-to-End Security and Resilience for Critical Infrastructures

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Abstract

This talk will examine the challenges of delivering **end-to-end security and resilience** in critical infrastructures and resource-constrained settings, focusing on **quantum-era protection mechanisms**. Key aspects include **hybrid post-quantum cryptography**, **programmable hardware**, and **adaptive network components** that enable advanced algorithmic security principles. Ongoing work from **two EU Horizon projects coordinated by the KIOS Research and Innovation Centre of Excellence** will be presented, showcasing practical approaches that bridge research and real-world deployment.

Biography

Dr. Angelos. K. Marnerides is a Professor (Asst.) of Cyber Physical Systems Security at the University of Cyprus, in the Department of Electrical & Computer Engineering and KIOS Research and Innovation Centre of Excellence. Previously, he was a Professor (Assoc.) at the University of Glasgow, leading the Glasgow Cyber Defence Group. His research has received significant funding in excess of 15M+ by both industry and governmental bodies and focuses on security and resilience in Cyber Physical Systems and programmable networks. Prof. Marnerides is a senior member of the IEEE, has consulted a variety of governmental and industrial stakeholders in the EU, US and the UK and he has played significant roles in various IEEE conferences, earning IEEE CoMSoc contribution awards in 2016 and 2018. He completed his PhD in Computer Science from Lancaster University in 2011, and has held lectureships and postdoctoral positions at institutions including Carnegie Mellon University, University of Porto, University College London, and Lancaster University.

References

Heterogeneous Integration of Co-Packaged Optics to navigate AI complexities

D. Velenis
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Abstract

Bandwidth and energy efficiency scaling of optical interconnects is required to address the growing needs of global data traffic and AI/ML applications within datacenters today. Combining optical interconnects with advanced packaging solutions is expected to be the answer for the extreme bandwidth density requirements for upcoming AI applications. An update of the different steps taken in the HiConnects project to bring optical interconnects into advanced system packaging are discussed in this presentation, together with a roadmap for serving both the computational and data bandwidth needs of AI applications through 3D integration of photonics and electronics.

Biography

Dimitrios Velenis is the leader of the silicon photonics device and characterisation group at imec. He has been with imec for more than 15 years, gaining experience on the benchmarking of advanced integration flows in 3D and Silicon Photonics interconnects. He has obtained M.Sc. and Ph.D. degrees from the University of Rochester. Previously, Dimitrios worked as Assistant Professor at the ECE Department at Illinois Institute of Technology, and as Research Associate at the University of Rochester. He is author and coauthor of more than 80 papers in journals and conference proceedings.

References

Development and manufacturing of Co-Packaged optics demonstrator on IC Substrate technology for the beyond state-of-the-art smart NICs and Switches

G. Park
Advanced Technologies and Solutions, Research
and Development, Leoben, Austria



Abstract

As artificial intelligence, machine learning, and big data workloads have explosive growth, the demand for high-performance infrastructure as hyperscale data centre is pushing the limits. HiConnects is aiming to support industrial challenges by developing heterogenous integration core technology solution for energy-efficient and high-performance cloud and edge computing.

In a subtask 3.3.2, we focused on the development of a co-packaged optics demonstrator based on the specifications of NVIDIA and the photonic components development in the pilot line. Specifically, the defined design will be delivered from NVIDIA after specifications of the envisioned product requirements for co-packaged optics NIC and switch. According to the design, AT&S will provide the proper solution on Integrated Circuit Substrate (ICS) or PCB with considering system levels needs. In addition, the simulation of heat spreading and mechanical stability (warpage) will be executed by considering different material parameters such as CTE, thermal and electrical conductivity, dielectric constant, and dissipation factor, respectively. PHIX will provide optimized interconnect solution and assemble the Silicon Photonics Transceiver interposer developed by IMEC, network chip, and driver ICs on the ICS. Thermosonic flip-chip bonding technique will be used where Gold micro bumping will be applied either on the ICS or chips. The micro-optical lenses from Teramount will be bonded on the SiPh transceiver chip and Fiber Connector will be attached accordingly. Finally, a functional testing of fully co-packaged optics demonstrator will be done by NVIDIA.

In this work, we investigated the test vehicle in order to achieve the working demonstrator at the end of HiConnects project. The progress for the test vehicle preparation and output from the project will be presented in this talk. In addition, we will outline a perspective supply chain for co-packaged optics in smart NICs and switches.

Biography

Gyuhyeon Park obtained his Doctor of Engineer (Dr.-Ing) in Mechanical Science and Engineer from the Technical University of Dresden, Germany in 2021. He continued his research at Leibnitz Institute for Solid State and Materials Research (IFW-Dresden) as post-doctor in Dresden, Germany in 2023. His research focused on the fabrication of micro-sized device with thin film of magneto-thermo-electric quantum material. After he join Advanced Technologies and Solutions (AT&S), Austria, now he is focusing on the Optical Communication in the R&D department as Project Manager and delivering successful projects across various industries.

References

Integration and Assembly of Co-Packaged Optics (CPO) for smart Networks and Switches

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Project Leader - Photonics Packaging
PHIX Photonics Assembly, Enschede, The
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Abstract

The rapid scaling of data center bandwidth requirements is pushing the limits of traditional pluggable optical modules, leading to the emergence of Co-Packaged Optics (CPO) as a promising solution for next-generation network interface cards (NICs) and switch architectures. This presentation outlines a collaborative workflow and integration scheme for CPO systems, highlighting the step-by-step assembly of photonic integrated circuits (PICs), drivers (EICs), and high-bandwidth fiber optics connectors for smart networking devices. We describe the joint contributions from key industrial and research partners—including Teramount (TM), AT&S, IMEC, PHIX, and NVIDIA—covering substrate design, optical/electronic die integration, and high-precision flip-chip bonding. Emphasis is placed on the alignment precision and thermal stability required for the successful coupling of fiber arrays, drivers (EICs) to PICs. The final packaging steps are optimized for signal integrity and thermal management to enable deployment in high-performance data center environments.

Biography

Anneirudh Sundararajan is a Project Leader at PHIX Photonics Assembly, where he leads several EU-funded initiatives as well as customer-driven projects. He specializes in flip-chip bonding technology and the advanced packaging of photonic integrated circuits (PICs). Prior to joining PHIX, Anneirudh worked in Germany as a Process Development Engineer at a photonic packaging company, gaining hands-on experience in scalable photonic assembly processes. Anneirudh pursued his PhD at the University of Twente, where his research focused on the integration of optical components with MEMS-based microfluidic systems. His work involved the development of Coriolis mass flow sensors and spectroscopic techniques for multiparameter fluid characterization. With a strong interdisciplinary background in optics, microfluidics, and photonic packaging, he is actively contributing to the development of next-generation photonic sensing platforms.

References

Scalable Fiber Assembly for co-package Optics and Advanced Semiconductor Packaging

E. Schleifer

Teramount, Jerusalem, Israel

Abstract

As the demand for high-speed, low-latency, and low-power data transfer grows in AI, high-performance computing, and data centers, optical interconnects are essential for scaling future generations of computing infrastructure. However, widespread adoption is limited by the complexities of fiber-to-photonics packaging in advanced 2.5D and 3D semiconductor architectures.

Teramount addresses these challenges through incorporation of wafer-level processes, including its Photonic-Bump and Photonic-Plug technology, which seamlessly aligns photonics packaging with standard semiconductor manufacturing and packaging flows. This approach enables large assembly tolerances, passive fiber attachment, and detachable mechanical connectivity, significantly improving yield, reworkability, and cost efficiency. The result is scalable, high-volume manufacturing that integrates fiber attachment processes into the highly demanding packaging requirements of advanced semiconductor packages.

This presentation will highlight Teramount's technological advances in wafer-level optics and integration workflows into standard semiconductor foundry and outsourced semiconductor assembly and tests (OSATs) processes. We will discuss how our innovations provide compatibility with advanced 2.5D and 3D packaging architectures, enabling post-reflow fiber attach, integration into thinned silicon photonic dies with TSVs, thin form factor support, and multiple testing points during the packaging process. These advancements are essential for driving the industry towards scalable, high-yield optical interconnects, unlocking the potential for large-scale deployment of AI and advanced computing systems.

Biography

Elad Schleifer

Teramount Ltd. (Israel)

Elad Schleifer is R&D manager at Teramount Ltd. Elad has a PhD in Physics from the Hebrew University of Jerusalem .

References