Materials Innovation

Accelerating nanoelectronic device innovation through atomistic simulation–driven material screening

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Abstract
The introduction of new materials in nanoelectronics has been a key driver of innovation and scaling since Moore's law began. Examples include the introduction of high-k insulating dielectrics, metal gates, silicon-germanium alloys, and alternatives to copper for interconnect layers. However, while the periodic table offers inspiration, it also presents challenges. The main issue is not only identifying materials with the right phase and properties but also ensuring they maintain these properties at the nanometer scale, can be conformally deposited, remain stable through various process steps, and have a low environmental impact. Thus, enabling new materials is a complex, multi-dimensional, time- and resource-intensive problem that requires a proper methodology and rigorous testing with devices at relevant dimensions. Traditionally, material candidates are identified through literature research and numerous trial-and-error experimental steps. Recent advancements in atomistic simulations are helping to optimize this procedure, enabling virtual screening of materials without prior experimental measurements. We will illustrate this process through the identification of candidates to build a selector function for memory arrays.

As process nodes continue to shrink, the spacing between parallel memory cells in the stack decreases, increasing the load on metal interconnects. Leakage current becomes an unavoidable issue, causing crosstalk between neighboring memory cells, affecting read and write operations, interfering with stored data, reducing storage lifespan, and increasing power consumption. To effectively suppress it, it is essential to control all possible leakage paths. The most efficient solution is to directly connect each memory cell to an independent device called a "selector," forming the memory array. The latter should ideally be built-in the memory device. Such a selector operates by switching between a high-resistance state (off) and a low-resistance state (on) when a certain threshold voltage is applied. Through this presentation, we will show how virtual material screening based on atomistic simulations of amorphous materials were used to design materials with tailored properties. When combined with machine learning, this approach is narrowing down potential candidates for device exploration and provide insights into precursor selection for the atomic layer deposition (ALD) of nanometer-thick films, while accounting for sustainability dimensions.

Biography
Geoffrey Pourtois studied Chemistry (1997) and obtained a PhD in Chemistry (2002) at the university of Mons Hainaut, Belgium. In 2003, he joined imec in Belgium, where he has been working in the field of atomistic modeling, with a special attention for establishing relations between material, interface defects and electrical device performances.

From 2003 to 2025, he has been building and heading the group of material simulation and physics in imec, where he has been focusing on the modeling, using atomistic simulations, of nanoelectronic related materials. His group is being involved in building fundamental insights into the relations between material, interface and device electrical performances for CMOS, memory, and exploratory devices concepts. During their exploration endeavour, his team studied complex material gate stacks involved in CMOS and memory applications and contributed to the identification and the study of new materials for interconnect, emerging

and magnetic memories. He was nominated imec fellow in 2020 and (co-) authored ~ 420 oral and peer-reviewed publications.

References

Innovative AMC Filtration solutions for future semiconductor production challenges

M. Zoermer
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Abstract
Filtration is crucial for maintaining high quality and process stability in semiconductor manufacturing. As processes advance and device geometries become more complex, high precision optics and process equipment demand optimal protection from particulate and molecular contamination.
As process nodes advance, molecular contamination has become just as important as particulate contamination. The necessity for innovative filtration solutions is emphasized by stricter requirements and new process chemicals.

Biography
Manfred Zoermer (born 1965), after studying chemistry (with focus on inorganic and high energy chemistry), started his professional career as sales engineer for analytical technology within the sales area Baden-Wuerttemberg. Several global positions in his career at suppliers of critical process materials to microelectronics, MEMS and compound semiconductor manufacturers connected him directly with clean room technology and led to high special process environment affinity. Further positions in and outside a wide range of industries in sales and marketing, led him to join MANN+HUMMEL Air Filtration at the beginning of 2020. In his current position, he is responsible for the development of a broadband product portfolio, particularly introducing chemical process technology to the air filter community. Manfred is involved as an expert in the standards and guidelines of VDMA, DIN and ISO workgroups.

References

Advances in AlScN Thin Films Deposited by Lam Research Pulsed Laser Deposition Platform

M. Dekkers
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Lam Research, Enschede, The Netherlands

Abstract
Pulsed laser deposition (PLD) is a very versatile thin film deposition technology that has the ability to deposit a wide range of advanced thin film materials. With today's market demand for enhanced and new material systems, PLD enables layers that cannot practically be deposited by conventional technologies like physical vapor deposition (PVD) reactive sputtering.

This deposition solution enables more advanced device design and is driving the next generation of radio frequency (RF) filters for 5G, WiFi 6 and 6E, high-end micro-electromechanical systems (MEMS), ferroelectric memory and photonics applications.

For piezoelectric aluminum scandium nitride, PLD has extended the limits of scandium doping in the AlScN compound, resulting in very high piezoelectric properties. Additionally, this PLD platform enables precise control over thickness uniformity and thin film stress, which are crucial for high-yield (RF) MEMS applications.

For the first time in semiconductor production, Lam is using lasers to deposit thin films and bringing PLD to wafer-level mass production. Lam Research PLD is expected to be key in developing cutting-edge specialty technologies devices, such as RF filters for 5G and Wi-Fi 6 and high-end MEMS microphones.

Biography
Matthijn Dekkers earned his PhD in Applied Physics from the University of Twente in 2007, the same year he co-founded SolMateS. As Chief Technology Officer, he led the R&D division in scaling the Pulsed Laser Deposition (PLD) technique for industrial applications. Following SolMateS' acquisition by Lam Research in 2022, Matthijn assumed the role of Director of Engineering for PLD, where he continues to drive innovation in advanced materials processing.

References

Substrate engineering for the benefit of advanced devices and integration

O. Bonnin
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Abstract
The continuous evolution of microelectronics and optoelectronics relies heavily on the development of innovative substrates that enable both performance enhancement and heterogeneous integration. Substrate engineering has emerged as a key enabler for advanced devices, offering tailored material properties, optimized interfaces, and scalable integration platforms. By leveraging techniques such as layer transfer, strain engineering, defect control, and heterogeneous bonding, engineered substrates provide pathways to overcome fundamental limitations of conventional materials. This approach not only supports the scaling of transistor architectures but also fosters the integration of diverse functionalities, including photonics, RF, power electronics... In this context, substrate engineering represents a cornerstone for the next generation of semiconductor devices, ensuring improved efficiency, reliability, and cost-effectiveness while enabling disruptive system-level innovations.

Biography
Olivier Bonnin is Senior Director of Soitec's Technology Development, which is gathering experts in various fields (Fundamental of Physics and simulation, Material, Process, Metrology and Device) and development teams.
He joined Soitec in 2006 as Product Engineering Manager and participated in the introduction of most of the existing Soitec's products.
Olivier Bonnin has authored or co-authored more than 30 papers. He has a PhD in Material sciences from CNRS.

References

„Materials, Innovations for Generations”

M. Joerger
Head of Business Line Power Electronic Materials
Heraeus Electronics GMBH, HANAU, Germany

Abstract
In the face of increasing environmental regulations and growing demand for sustainable electronics, the semiconductor and electronic packaging industries are under pressure to reduce their carbon footprint without compromising performance. This presentation introduces a series of material innovations that demonstrate how sustainability and high performance can go hand in hand.
We showcase three key developments: (1) **recycled gold bonding wire**, which maintains electrical and mechanical reliability while significantly reducing the environmental impact (2) **Die Top System Silver as a viable alternative to Die Top System Gold**, offering comparable electrical performance with a lower environmental and economic cost; and (3) **recycled tin in solder pastes**, which supports circular economy principles and reduces the carbon intensity of assembly processes.

Biography
Dr. Michael Jörger has 20 years experience in managing product development and launching of innovative materials for electronics and renewable energies with a focus of Power Modules and Semiconductor Packaging materials.
Michael holds a Ph.D in Material Science from ETH Zurich, Switzerland, and a diploma in chemistry from the University of Karlsruhe in Germany.
Currently he is leading the Business Line Power Electronic Materials at Heraeus Electronics.

References

Topic Coming Soon

O. Faynot
EVP, Head of Silicon Component Division
CEA-Leti, Grenoble, France

Abstract
Coming Soon

Biography
Olivier Faynot received the M.Sc and Ph.D. degrees from the Institut National Polytechnique de Grenoble, France in 1991 and 1995, respectively. His doctoral research was related to the characterization and modeling of deep submicron Fully Depleted SOI devices fabricated on ultrathin SIMOX wafers.
He joined CEA (CEA-Grenoble, France) in 1995, working on Partially Depleted and Fully Depleted SOI technologies development in the frame of Industrial Partnerships.
From 2008 to 2017, he managed various teams focussed on advanced CMOS, memories and 3D technology integration and was assigned on manufacturing sites to implement FDSOI technologies.
During that period, he was engaged in the transfer to production of 28nm and 22nm FDSOI technologies with industrial partners. Those technologies are now available in production.
From 2017 to 2019, he managed the Patterning department at CEA-LETI, within the Silicon Technology division.
Since 2019, he is managing the whole Silicon Component division at CEA-LETI.
He is author and co-author of more than 400 scientific publications in journals and international conferences, and was successively in the committees of the main international Semiconductors conferences like International Electron Device Meeting (IEDM), the symposium on VLSI Technology, the IEEE International SOI conference, the EUROSOI network, the Solid State Device and Materials (SSDM) conference and the International S3S conference.
He received the ‘Général Férié’ award in 2012 and the ‘Electron d’Or’ award with CEA-Leti, ST Microelectronics and SOITEC in 2017.
He has been elected as an IEEE Fellow in 2024 for leadership in CMOS technology development.

References