

SCREEN

Introductory note

M. Hollfelder
Vice President Service IQ & Technology
SCREEN SPE Germany GmbH, Ismaning, Germany



Abstract

Introductory note

Biography

Dr. Hollfelder received his Master of Science and Ph.D. in Physics from Technical University Aachen working on III/V Epitaxy, layer characterization, photonic devices, and HEMT transistors at Research Centre Juelich in Germany. He started his career at SCREEN in 1996 in various positions in Service Support and Technical Sales. For more than 10 years he has been managing the Product Engineering and Process Technology for Annealing, Cleaning, Lithography, and Measurement/Inspection products and he is now Vice-President for Service & Technology including the support of the various R&D collaboration for SCREEN Semiconductor Solutions in Europe.

References

Sustainability Initiatives to create innovative green solutions for carbon neutrality

T. Mikawa
Executive Officer of R&D strategy / IP strategy
SCREEN Semiconductor Solutions CO., LTD.,
Kyoto, Japan



Abstract

Recent advances in generative AI are accelerating device scaling, 3D stacking, and system-level integration. To support next-generation semiconductor technologies, increasingly complex device architectures and novel materials are being explored. These advancements demand innovative wet cleaning solutions capable of removing ever-smaller particles and achieving extremely high etching selectivity and uniformity. In parallel, environmental considerations are becoming critical. As device scaling increases, the number of process steps grows, leading to higher carbon footprints—particularly in terms of CO₂ emissions. To address this, we have developed chemical reduction strategies, including recycling cabinets and efficient chemical circulation systems for on-tool reclamation. However, the majority of our CO₂ emissions fall under Scope 3, which requires broader collaboration across the supply chain. To effectively reduce Scope 3 emissions, we must strengthen partnerships with upstream material suppliers and component manufacturers, as well as downstream chipmakers. Through our Semiconductor Eco System, we are fostering collaboration with research institutes, suppliers, and academia to co-develop innovative green wet process solutions. These solutions aim to deliver high yields at leading-edge nodes, minimize device damage, and significantly reduce carbon emissions during fabrication.

Biography

Takumi Mikawa is Executive Officer of R&D strategy / IP strategy at SCREEN Semiconductor Solutions. His interest is to develop process solutions based on the semiconductor equipment, collaborating with his partners such as imec, IBM and academia. He is also interested in the sustainable technology, and a leader of ESH/S of Silicon Device Roadmap committee of Japan (SRDJ). His background is the emerging memories, FeRAM and ReRAM at Panasonic Corporation. He is patent attorney and has lectured on intellectual property in Wakayama University as a visiting professor.

References

Enabling climate aware process development for IC chip manufacturing

E. Gallagher
Program Director, Sustainable Semiconductor
Systems and Technologies
imec, Leuven, Belgium



Abstract

imec has developed the imec.**netzero** virtual fab to quantify environmental impacts at the fab, technology and process levels. At imec, this methodology is used to identify technology hotspots and motivate process development projects in our 300mm fab. More recently, imec introduced the **e-score** metric to enable simple communication of environmental impact without demanding a background in LCA (Life Cycle Analysis) or the ESG (Environmental, Social, and Governance). The e-score methodology will be used to illustrate the life cycle of a semiconductor process project. We describe how we prioritize development activities in the fab by identifying technology hotspots, how a relevant project is defined, the process-level and module level data that is generated, and the quantification of potential impact reduction over a full logic technology. The communication of sustainable development results in a vocabulary that transcends the environment will be described.

Biography

Emily Gallagher is a program director for SSTS at imec, focusing on sustainability in semiconductor manufacturing processes. Emily earned her PhD in physics from Dartmouth College where she studied free electron lasers. After graduation, she joined IBM and became immersed in semiconductor technology. She held many wafer fabrication roles at IBM from functional characterization to process integration, to leading the EUV mask development effort. She joined imec in 2014 to continue EUV development work. Emily has authored over 100 technical papers, holds over 20 patents, is an SPIE Fellow and co-leads the SEMI Semiconductor Climate Consortium Scope1 Working Group.

References

Accelerating nanoelectronic device innovation through atomistic simulation-driven material screening

G. Pourtois
Fellow
Imec, STAMP, Leuven, Belgium



Abstract

The introduction of new materials in nanoelectronics has been a key driver of innovation and scaling since Moore's law began. Examples include the introduction of high-k insulating dielectrics, metal gates, silicon-germanium alloys, and alternatives to copper for interconnect layers. However, while the periodic table offers inspiration, it also presents challenges. The main issue is not only identifying materials with the right phase and properties but also ensuring they maintain these properties at the nanometer scale, can be conformally deposited, remain stable through various process steps, and have a low environmental impact. Thus, enabling new materials is a complex, multi-dimensional, time- and resource-intensive problem that requires a proper methodology and rigorous testing with devices at relevant dimensions. Traditionally, material candidates are identified through literature research and numerous trial-and-error experimental steps. Recent advancements in atomistic simulations are helping to optimize this procedure, enabling virtual screening of materials without prior experimental measurements. We will illustrate this process through the identification of candidates to build a selector function for memory arrays.

As process nodes continue to shrink, the spacing between parallel memory cells in the stack decreases, increasing the load on metal interconnects. Leakage current becomes an unavoidable issue, causing crosstalk between neighboring memory cells, affecting read and write operations, interfering with stored data, reducing storage lifespan, and increasing power consumption. To effectively suppress it, it is essential to control all possible leakage paths. The most efficient solution is to directly connect each memory cell to an independent device called a "selector," forming the memory array. The latter should ideally be built-in the memory device. Such a selector operates by switching between a high-resistance state (off) and a low-resistance state (on) when a certain threshold voltage is applied. Through this presentation, we will show how virtual material screening based on atomistic simulations of amorphous materials were used to design materials with tailored properties. When combined with machine learning, this approach is narrowing down potential candidates for device exploration and provide insights into precursor selection for the atomic layer deposition (ALD) of nanometer-thick films, while accounting for sustainability dimensions.

Biography

Geoffrey Pourtois studied Chemistry (1997) and obtained a PhD in Chemistry (2002) at the university of Mons Hainaut, Belgium. In 2003, he joined imec in Belgium, where he has been working in the field of atomistic modeling, with a special attention for establishing relations between material, interface defects and electrical device performances.

From 2003 to 2025, he has been building and heading the group of material simulation and physics in imec, where he has been focusing on the modeling, using atomistic simulations, of nanoelectronic related materials. His group is being involved in building fundamental insights into the relations between material, interface and device electrical performances for CMOS, memory, and exploratory devices concepts. During their exploration endeavour, his team studied complex material gate stacks involved in CMOS and memory applications and contributed to the identification and the study of new materials for interconnect, emerging and magnetic memories. He was nominated imec fellow in 2020 and (co-) authored ~ 420 oral and peer-reviewed publications.

Enabling Resilience and Circularity in Semiconductor Manufacturing: CEA-Leti's Role in FAMES, GENESIS, and SUBFAB LABS

L. Pain
Sustainable Electronics Program Director
CEA-LETI, Sustainable Electronics Program,
Grenoble, France



Abstract

The semiconductor industry is a cornerstone of the digital transformation, with the ICT market projected to double by 2030, driven by breakthroughs in AI, 5G, and cloud technologies. Meeting this demand requires not only innovation but also a shift toward sustainable manufacturing practices. Key challenges include reducing resource consumption (water, gases, and metals), limiting reliance on PFAS chemicals, and integrating circular approaches to effluent management.

To accelerate this transition, CEA-Leti has developed a comprehensive sustainability roadmap that spans the full value chain—from manufacturing processes to system-level solutions. This presentation will showcase CEA-Leti's pivotal contributions, notably through leadership in two flagship initiatives: the FDSOI FAMES pilot line and the Chips JU GENESIS program, where it serves as coordinator. It will also introduce **SUBFAB LABS**, a new collaborative platform with SEMI and ISRL, dedicated to advancing sustainable sub-fab technologies.

Biography

Laurent Pain is graduated from the Ecole Nationale Supérieure de Physique de Grenoble in 1992. He received his Ph D after his work on DUV resists study. He joined CEA-Leti in 1996 to work on infra-red technology, and then moved to STmicroelectronics in 1999 working on 193nm and e-beam lithography technologies. From 2008 to 2014, Laurent led the lithography laboratory of the silicon technology division of CEA-Leti. In July 2014, within the CEA-Leti Silicon Technology Division, he was in charge of the business and the partnerships developments of the Silicon Technologies Platform Division. Since Sept 2023, he is took the position of Sustainable Electronic Program Director with the mission to build and consolidate the strategy and programs of CEA6Leti in the field of evo-innovation and sustainability.

References

Sustainability with Dissolved Gases in Semiconductor applications

A. Barth
Lead Advanced Technology Group Plasma &
Reactive Gas Solutions – Ozone Products
MKS Instruments Deutschland GmbH, Berlin,
Germany



Abstract

Wet cleaning is a major part of the semiconductor manufacturing process and is becoming a more critical process with continued node scaling in Logic and Memory. At the same time, advanced technology nodes drive increased environmental impact and carbon footprint. Higher use of energy, utilities, gases, water and chemicals associated with advanced technology nodes drives the need for sustainable solutions by semiconductor manufacturers, OEMs and component suppliers.

As a component supplier, MKS supports process optimizations driven by semiconductor manufacturers towards reduced emissions. MKS provides dissolved gas solutions for wet chemistry wafer processing. Several options are available to reduce water, energy and gas consumption. Sleep, recirculation and reclaim modes help lowering the semi manufacturers' overall emissions.

Additionally, as a general concept, dissolved ozone can provide an environmentally friendly alternative to classical chemistry like sulfuric acid and hydrogen peroxide as oxidative species. The 'green' advantage of ozone is the point-of-use formation and a short lifetime, that eliminates the need for abatement.

This presentation will give an overview on Dissolved Gases used for advanced semiconductor cleaning and the possibilities to support industry sustainability initiatives.

Biography

- Anina has been with MKS for 8 years.
- She holds a PhD degree in Chemistry from Technical University in Berlin, Germany.
- She has started her career as cleaning expert for electrostatic and immersion wafer tables at Berliner Glas, now ASML.
- Anina then transitioned to project management for product development for 8 years and is a PMI certified project manager.
- In 2023 Anina transitioned back to science by joining the Advanced Technology Group for Dissolved Gases.
- She is leading this group since October 2023.
- Her expertise is in applications for cleaning and specialty etches with dissolved gases.
- Anina engages in activities to bring and keep women in the field of technology.

References

SU-3400 – Leading edge Single Wafer Processing for sustainable Manufacturing

M. Goeke
Senior Manager Technical Sales & Product
Engineering
Screen SPE, Technical Sales, Ismaning, Germany

Abstract

Wafer cleaning and surface preparation is a key discipline in semiconductor device manufacturing.

As many other manufacturing processes it can be inherently resource-intensive; requiring significant amounts of energy, gases, chemicals and water.

Based on the Screen Group's charter of corporate social responsibility, Screen is committed to actively develop and provide eco-friendly products and services and to strive continuously for reducing consumptions and environmental impact.

Showcasing Screen Semiconductor Solutions's Single Wafer Processor SU-3400, we will present how consumptions for common process chemicals and gases are reduced without trading off with performance. Improvements are enabled by new fluid handling systems, dispense methods for liquids and Nitrogen and exhaust design.

Together with sensor based consumption and trend monitoring, Screen's SU-3400 helps to minimize and control environmental footprint in the field of cutting edge processing.

Biography

Mark Goeke received his Master of Science in Photo Engineering from the University of Applied Science, Cologne in 1994.

After holding various positions in lithography engineering he started working with Dainippon Screen Mfg.Co (now Screen SPE, Germany) in 1999.

Here he moved to hold the position of the Manager Technical Sales & Product Engineering, responsible for technology and product engineering for Screen's line-up of semiconductor production equipment, comprising lithography tracks, single wafer processors, annealing and inspection systems.

References

Enhancing Sustainability in Semiconductor Manufacturing: Energy-Efficient Optical Crosslinking for Lithography Processes

H. Stokes

R&D Strategy Manager

SCREEN SPE USA, LLC, 3151 Jay Street, Suite 210,
Santa Clara, United States of America



Abstract

A critical challenge in semiconductor manufacturing is the high electricity consumption, especially by lithography tools, which significantly contribute to the industry's environmental impact. For lithography track systems, reducing the energy consumption of hotplate processes is essential due to their high energy demands. This study introduces an innovative, energy-efficient process that offers a viable alternative to conventional thermal crosslinking systems for spin-on carbon (SOC) and spin-on glass (SOG) underlayers, which typically require high temperatures for full film densification.

The proposed method utilizes an overall-wafer optical exposure system, integrated on SCREEN's DT-3000 track, to crosslink underlayer materials designed by Brewer Science to cure through light exposure. This paper demonstrates how this optical crosslinking approach can achieve substantial energy savings of 85% for SOC and 60% for SOG, while maintaining lithographic performance. The transition from a traditional hotplate process to a light-curing mechanism is thoroughly examined from multiple perspectives.

Biography

Dr. Harold Stokes received his PhD in Chemistry from the University of Texas at Dallas. After completing his education, he joined Atmel as a lithography process engineer where he was responsible for performing evaluations on incoming resist samples. After leaving Atmel, he served as a final clean engineer with Photronics responsible for ensuring defect free photomasks moving to receive pellicle mount. Approximately 20 years ago Dr. Stokes joined SCREEN to support the installation and qualification of lithography systems for customers in the US. From 2013 until 2021 he served as imec assignee for the advanced lithography program activities between SCREEN and imec. After completing his assignment in Belgium, he returned to the US where he joined SCREEN's global marketing team. Currently, he is serving as R&D strategy manager within SCREEN's technology enablement department. His career experience includes lithography, cleaning, and surface defect metrology.

References