AI Chip Design

Topic Coming Soon

C. Frey
Vice-President of EU Engagements & General Manager
Arm France, Sophia Antipolis, France

Abstract
Coming Soon

Biography
Based in Sophia Antipolis France, he has been the **General Manager of Arm France** since 2014. He also serves as **VP of EU Engagements** where he focuses on strengthening Arm's presence within the European semiconductor ecosystem.

Prior to Arm he has held various roles in design and management at STMicroelectronics in Crolles, France, for 12 years. He contributed to establish the Crolles2 alliance with Philips and Motorola, an experience that led to his first international immersion in Austin Texas.
He then joined the startup SOISIC, where he served as VP of Engineering before the company was acquired by Arm in 2006. At Arm, he has spent four years in Silicon Valley California as VP of Operations.
In 2024 he became an operating Partner at C4 Ventures investment fund, where he brings his 30 years of experience in the semiconductor industry.
He holds a MS degree from PHELMA Grenoble.

References

The EU Chips Design Platform: a catalyst for fabless startups in Europe

R. Hoofman
Strategic Development Director
imec, Leuven, Belgium

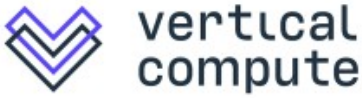
Abstract
The EU Chips Design Platform will enable fabless companies to access the resources they need quickly and efficiently via a cloud-based virtual environment, offering chip design resources, training, and capital. Coordinated by imec, twelve key European research players in the semiconductor ecosystem have joined forces in a consortium to create this design platform.
The platform aims to onboard the first startups and small and medium enterprises by early 2026, providing them with low-barrier access to European design capabilities, including route-to-chip fabrication, packaging, and testing. It will offer customized support to access commercial electronic design automation (EDA) tools, intellectual property (IP) libraries, EU Chips Act pilot line technologies, and access to design IP repositories, including open-source options. Additionally, the platform will feature a startup support program with incubation, acceleration, and mentoring activities next to financial assistance to help early-stage companies turn their innovative ideas into reality.

Biography
Romano Hoofman is Strategic Development Director at imec since 2016. He is currently responsible for the innovation programs at IC-Link and for the coordination of both the EU Chips Design Platform and the EUROPRACTICE Service.
He started his career in industry, where he worked as a Principal Scientist at Philips Research and later on NXP Semiconductors. He covered many different R&D topics, ranging from CMOS integration, advanced packaging, thin film batteries, photovoltaics and (bio)sensors.
Romano received his PhD from the Technical University of Delft in 2000, where he investigated charge transport in semi-conducting polymers. He has authored more than 30 publications and holds more than 10 patents in various research areas.

References

Shifting boundaries: Advancing Memory and Compute, Together.

S. Dubois
CEO
VERTICAL COMPUTE, Louvain-la-Neuve, Belgium



Abstract
Compute chip performance has surged over the last decades, but memory performance, using technologies like SRAM, DRAM, and 3D-NAND, has lagged, leading to complex memory hierarchies. The recent rise of Generative AI has pushed memory demands beyond current capabilities, resulting in expensive High-Memory-Bandwidth (HBM) chips and AI systems in the cloud, just as scaling roadmaps for the memory technologies are stalling.
This presents an opportunity for Vertical Compute's integrated memory, which vertically integrates magnetic bit strings directly above transistors. This offers greater density than DRAM (> Gb/mm2) and SRAM-like access latency (~10ns). Direct CMOS integration eliminates data bus bottlenecks, reducing power and enabling high-performance, in-memory compute for LLM inference on a single chip.
This presentation will cover the state of Generative AI hardware, the 100X potential of vertical integrated memories, and the path to industrial production.

Biography
Sylvain Dubois is the CEO and co-founder of Vertical Compute, a hardware semiconductor startup developing a proprietary vertical integrated memory technology, designed to unleash the data flow for data intensive workloads.

He previously worked at Google, in Advanced Technology Sourcing & Partnerships for the Google Cloud Infrastructure group in Sunnyvale, CA. His responsibilities included identifying, analyzing, and developing emerging technology trends, with a focus on Artificial Intelligence hardware acceleration compute chips, memory, and chiplet integration. Prior to his role at Google, he served as Vice-President of Business at Crossbar, a California-based deep tech startup specializing in novel memory development.

References

Arago: Practical Optical Computing

N. Muller
CEO
Arago, Arcueil, France

Abstract
Arago has built an energy-efficient AI chip powered by light, codenamed JEF, designed to run AI workloads with 10x to 30x lower energy and cost overhead. Its mission is to drive the course of history forward. Based in France, North America, and Israel, Arago has assembled a world-class team of engineers, scientists, and operators from leading companies and research labs, and is backed by executives from Apple, Arm, Nvidia, Microsoft, and Hugging Face, as well as prominent deeptech venture firms and exited founders.

Biography
Coming Soon

References

Sovereignty Comes from the Strongest Link in the Chain: Why Europe's technological strategy should be all in on areas of comparative advantage

E. Bithell
Head of Strategy and Sovereign Partnerships
Fractile, London, United Kingdom

Abstract
Technological sovereignty is often discussed in maximalist or minimalist terms, either demanding an entire onshore manufacturing chain or simply stockpiles of end products that rapidly become obsolete. Neither is a credible strategy for Europe: what we need is to focus on areas of competitive advantage which give strategic leverage in the long term, combined with wise partnerships overseas.

The strategic focus should thus be on parts of the supply chain that are ideally placed to maximise value and technological advantage in Europe, without leaning on inputs that are more expensive here. Fabless manufacturing is such a case, with AI making advanced semiconductors more strategically vital than ever before. If Europe succeeds in cutting edge innovation in these areas, the resulting technological advantages will enable global collaborations where Europe is a vital player, boosting European prosperity and resilience.

Biography
Ed Bithell is Head of Strategy and Sovereign Partnerships at Fractile. Prior to this, he was a UK civil servant and diplomat, as well as a policy analyst for emerging technologies such as semiconductors.

Fractile is building the hardware needed to unlock colossal scaling of frontier AI inference compute. The company’s custom silicon and software ecosystem is built around delivering hundreds of times faster access to memory, in turn allowing for extremely low inference latency while maximising throughput and minimising cost.

References

Ubiquitous AI Computing - AI Everywhere

A. Bond
Director - Silicon Verification
Axelera AI, Silicon, Bristol, United Kingdom

Abstract

Artificial Intelligence, Machine Learning, ChatBots, MCPs, and a plethora of other terms associated with the evolution of computing are becoming as ubiquitous as the technology itself. Whether it's asking Alexa for cinema recommendations from the comfort of your sofa, prompting Siri to curate a playlist for your Monday morning commute, or utilizing GitHub Copilot to fix your Python syntax, AI has become an integral part of our daily lives.

Despite this widespread integration, the underlying technology remains largely centralized and cloud-based, leaving edge customers underserved by existing solutions. From security and retail to industrial applications, robotics, automotive, and energy sectors, the demand for AI solutions continues to rise, yet the availability of suitable options lags behind.

The edge space presents a unique challenge due to the contrasting requirements of performance, cost, and power consumption, making it a technically demanding yet ripe area for innovation. When combined with the fragmented nature of these sectors and the diverse range of applications, the prospect becomes even more fascinating and challenging.

This presentation aims to introduce this rapidly evolving landscape and highlight the future challenges ahead. By referencing Axelera's innovative hardware and software approach, we hope to initiate a discussion on how we can progress together.

Biography

Andy has accumulated over 25 years of experience in the semiconductor industry, working across various fields from processors to networking, as well as audio and finance.
His experience covers most aspects of consumer electronics, primarily in the roles of design verification engineer and manager.

Beginning his career at ST Micro, Andy has led teams at Icera Semiconductor, NVIDIA, and Cirrus Logic. Currently, as the Director of Silicon Verification at Axelera AI,
he is applying his expertise to the dynamic field of artificial intelligence.

References