AI Chip Design

Welcome Remarks

L. Altimime
President
SEMI Europe, Berlin, Germany

Abstract
Welcome Remarks

Biography
Laith Altimime, as President of SEMI Europe, leads SEMI's activities in Europe and the Middle East and Africa (EMEA). Altimime has P&L responsibility as well as ownership of all Europe region programs and events, including SEMICON Europa. He is responsible for establishing industry standards, advocacy, community development, expositions, and programs. He provides support and services to SEMI members worldwide that have supply chain interests in Europe. He manages and nurtures relationships with SEMI members in the region and globally as well as with local associations and constituents in industry, government, and academia. Altimime has more than 30 years of international experience in the semiconductor industry. Prior to joining SEMI in 2015, He held senior leadership positions at NEC, KLA-Tencor, Infineon, Qimonda, and imec. Altimime holds an MSc from Heriot-Watt University, Scotland.

References

Building Europe’s Edge in the Age of Chiplets

C. Frey
Vice-President of EU Engagements
Arm France, Sophia Antipolis, France

Abstract
As the industry enters the age of chiplets, compute will become modular, accelerating time-to-market and expanding design choice. By breaking monolithic designs into modular, specialized components, chiplets enable new efficiencies, faster innovation cycles, and broader ecosystem participation. Looking across past industrial revolutions, Europe has demonstrated leadership before and it can do so again. Europe’s strengths in research, lithography, and IP design provide a strong foundation, but gaps in fabless capacity, system integration, and value capture remain obstacles. This session will examine how to turn Europe’s technical advantages into leadership in the chiplet era: by driving standards and interoperability, aligning semiconductor R&D with system-maker requirements, and fostering collaboration across startups, foundries, EDA, packaging, and system champions. The goal is clear: convert European strengths into shipping products, revenue growth, and a durable competitive position in the next era of compute.

Biography
Based in Sophia Antipolis France, he has been the **General Manager of Arm France** since 2014. He also serves as **VP of EU Engagements** where he focuses on strengthening Arm’s presence within the European semiconductor ecosystem.

Prior to Arm he has held various roles in design and management at STMicroelectronics in Crolles, France, for 12 years. He contributed to establish the Crolles2 alliance with Philips and Motorola, an experience that led to his first international immersion in Austin Texas.
He then joined the startup SOISIC, where he served as VP of Engineering before the company was acquired by Arm in 2006. At Arm, he has spent four years in Silicon Valley California as VP of Operations.
In 2024 he became an operating Partner at C4 Ventures investment fund, where he brings his 30 years of experience in the semiconductor industry.
He holds a MS degree from PHELMA Grenoble.

References

The EU Chips Design Platform: a catalyst for fabless startups in Europe

R. Hoofman
Strategic Development Director
imec, Leuven, Belgium

Abstract
The EU Chips Design Platform will enable fabless companies to access the resources they need quickly and efficiently via a cloud-based virtual environment, offering chip design resources, training, and capital. Coordinated by imec, twelve key European research players in the semiconductor ecosystem have joined forces in a consortium to create this design platform.
The platform aims to onboard the first startups and small and medium enterprises by early 2026, providing them with low-barrier access to European design capabilities, including route-to-chip fabrication, packaging, and testing. It will offer customized support to access commercial electronic design automation (EDA) tools, intellectual property (IP) libraries, EU Chips Act pilot line technologies, and access to design IP repositories, including open-source options. Additionally, the platform will feature a startup support program with incubation, acceleration, and mentoring activities next to financial assistance to help early-stage companies turn their innovative ideas into reality.

Biography
Romano Hoofman is Strategic Development Director at imec since 2016. He is currently responsible for the innovation programs at IC-Link and for the coordination of both the EU Chips Design Platform and the EUROPRACTICE Service.
He started his career in industry, where he worked as a Principal Scientist at Philips Research and later on NXP Semiconductors. He covered many different R&D topics, ranging from CMOS integration, advanced packaging, thin film batteries, photovoltaics and (bio)sensors.
Romano received his PhD from the Technical University of Delft in 2000, where he investigated charge transport in semi-conducting polymers. He has authored more than 30 publications and holds more than 10 patents in various research areas.

References

Topic Coming Soon

A. Rensink
Senior Director Account Management & Business Development
TSMC, Taipei, Taiwan

Abstract
Coming Soon

Biography
Dr. Alexander Rensink is responsible for account management & business development in the EMEA region at TSMC. Besides HPC, Smartphone and IoT markets, the Automotive semiconductor growth opportunity is one of his focus areas. Prior to joining TSMC, Alexander worked at European semiconductor companies ams and NXP Semiconductors in various strategic & business management roles. Alexander is a Dutch citizen and holds a Ph.D. in Electrical Engineering.

References

RISC-V Meets Brain-Inspired Intelligence

H. Amrouch
Prof. Dr.-Ing.
Technical University of Munich (TUM), Chair of AI Processor Design, Munich, Germany

Abstract
Brain-inspired Hyperdimensional Computing (HDC) offers a compelling alternative to conventional neural networks by leveraging high-dimensional vector algebra for efficient and robust machine learning. We demonstrate that customizing RISC-V to the specific requirements of HDC algorithms enables highly energy-efficient edge training, achieving performance within merely a few microjoules.

Biography
Professor Amrouch is heading the Chair of AI Processor Design at the Technical University of Munich. He is, the head of Brain-inspired Computing at the Munich Institute of Robotics. He is the head of the Semiconductor Test and Reliability at the University of Stuttgart. He is also the Academic Director of TUM Venture. He is the Founding Director of Munich Center for AI Chips.

References

How VSORA Positions Europe at the Forefront of AI

K. Maalej
CEO
VSORA, Meudon La Foret, France

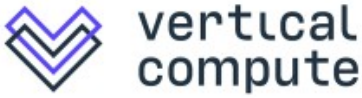
Abstract
The future of Artificial Intelligence will be defined by those who not only push the limits of technology, but who also ensure that innovation serves resilience, sovereignty, and shared prosperity. Europe stands at a turning point: to secure its place as a global leader, it must embrace breakthroughs that combine world-class performance with sustainability and accessibility.
VSORA embodies this vision. Its proprietary architecture achieves what was once thought impossible: four times the application performance of today's leaders, while consuming only half the power. It matches the maximum memory capacity achievable by current technologies, standing shoulder-to-shoulder with Nvidia and AMD, yet it goes further—dramatically reducing the cost per token and the cost of ownership for AI data center inference.
This is not simply a technological advance; it is a strategic leap. By lowering barriers to AI deployment, VSORA makes the tools of the future more affordable, more efficient, and more European. In doing so, it ensures that Europe is not a passenger in the AI revolution, but a driver—shaping the global narrative, setting new standards, and proving that innovation with purpose can power a resilient and competitive economy.

Biography
Khaled Maalej is CEO of VSORA, a provider of ultra-high-performance chip solutions for artificial intelligence in data center and edge applications based in France. Before founding VSORA in 2015 with other DSP engineers, Maalej was CTO - Digital Tuner Business of Parrot, the leading drone provider, and DiBcom, a fabless semiconductor company that designed chipsets for low-power mobile TV and radio reception acquired by Parrot. He graduated from Ecole Polytechnique & Ecole Nationale Superieure des Telecommunications in Paris.

References

Shifting boundaries: Advancing Memory and Compute, Together.

S. Dubois
CEO
VERTICAL COMPUTE, Louvain-la-Neuve, Belgium



Abstract
Compute chip performance has surged over the last decades, but memory performance, using technologies like SRAM, DRAM, and 3D-NAND, has lagged, leading to complex memory hierarchies. The recent rise of Generative AI has pushed memory demands beyond current capabilities, resulting in expensive High-Memory-Bandwidth (HBM) chips and AI systems in the cloud, just as scaling roadmaps for the memory technologies are stalling.
This presents an opportunity for Vertical Compute's integrated memory, which vertically integrates magnetic bit strings directly above transistors. This offers greater density than DRAM (> Gb/mm2) and SRAM-like access latency (~10ns). Direct CMOS integration eliminates data bus bottlenecks, reducing power and enabling high-performance, in-memory compute for LLM inference on a single chip.
This presentation will cover the state of Generative AI hardware, the 100X potential of vertical integrated memories, and the path to industrial production.

Biography
Sylvain Dubois is the CEO and co-founder of Vertical Compute, a hardware semiconductor startup developing a proprietary vertical integrated memory technology, designed to unleash the data flow for data intensive workloads.

He previously worked at Google, in Advanced Technology Sourcing & Partnerships for the Google Cloud Infrastructure group in Sunnyvale, CA. His responsibilities included identifying, analyzing, and developing emerging technology trends, with a focus on Artificial Intelligence hardware acceleration compute chips, memory, and chiplet integration. Prior to his role at Google, he served as Vice-President of Business at Crossbar, a California-based deep tech startup specializing in novel memory development.

References

Arago: Practical Optical Computing

N. Muller
CEO
Arago, Arcueil, France

Abstract
Arago has built an energy-efficient AI chip powered by light, codenamed JEF, designed to run AI workloads with 10x to 30x lower energy and cost overhead. Its mission is to drive the course of history forward. Based in France, North America, and Israel, Arago has assembled a world-class team of engineers, scientists, and operators from leading companies and research labs, and is backed by executives from Apple, Arm, Nvidia, Microsoft, and Hugging Face, as well as prominent deeptech venture firms and exited founders.

Biography
Coming Soon

References

Sovereignty Comes from the Strongest Link in the Chain: Why Europe's technological strategy should be all in on areas of comparative advantage

E. Bithell
Head of Strategy and Sovereign Partnerships
Fractile, London, United Kingdom

Abstract
Technological sovereignty is often discussed in maximalist or minimalist terms, either demanding an entire onshore manufacturing chain or simply stockpiles of end products that rapidly become obsolete. Neither is a credible strategy for Europe: what we need is to focus on areas of competitive advantage which give strategic leverage in the long term, combined with wise partnerships overseas.

The strategic focus should thus be on parts of the supply chain that are ideally placed to maximise value and technological advantage in Europe, without leaning on inputs that are more expensive here. Fabless manufacturing is such a case, with AI making advanced semiconductors more strategically vital than ever before. If Europe succeeds in cutting edge innovation in these areas, the resulting technological advantages will enable global collaborations where Europe is a vital player, boosting European prosperity and resilience.

Biography
Ed Bithell is Head of Strategy and Sovereign Partnerships at Fractile. Prior to this, he was a UK civil servant and diplomat, as well as a policy analyst for emerging technologies such as semiconductors.

Fractile is building the hardware needed to unlock colossal scaling of frontier AI inference compute. The company’s custom silicon and software ecosystem is built around delivering hundreds of times faster access to memory, in turn allowing for extremely low inference latency while maximising throughput and minimising cost.

References

Ubiquitous AI Computing - AI Everywhere

A. Bond
Director - Silicon Verification
Axelera AI, Silicon, Bristol, United Kingdom

Abstract

Artificial Intelligence, Machine Learning, ChatBots, MCPs, and a plethora of other terms associated with the evolution of computing are becoming as ubiquitous as the technology itself. Whether it's asking Alexa for cinema recommendations from the comfort of your sofa, prompting Siri to curate a playlist for your Monday morning commute, or utilizing GitHub Copilot to fix your Python syntax, AI has become an integral part of our daily lives.

Despite this widespread integration, the underlying technology remains largely centralized and cloud-based, leaving edge customers underserved by existing solutions. From security and retail to industrial applications, robotics, automotive, and energy sectors, the demand for AI solutions continues to rise, yet the availability of suitable options lags behind.

The edge space presents a unique challenge due to the contrasting requirements of performance, cost, and power consumption, making it a technically demanding yet ripe area for innovation. When combined with the fragmented nature of these sectors and the diverse range of applications, the prospect becomes even more fascinating and challenging.

This presentation aims to introduce this rapidly evolving landscape and highlight the future challenges ahead. By referencing Axelera's innovative hardware and software approach, we hope to initiate a discussion on how we can progress together.

Biography

Andy has accumulated over 25 years of experience in the semiconductor industry, working across various fields from processors to networking, as well as audio and finance.
His experience covers most aspects of consumer electronics, primarily in the roles of design verification engineer and manager.

Beginning his career at ST Micro, Andy has led teams at Icera Semiconductor, NVIDIA, and Cirrus Logic. Currently, as the Director of Silicon Verification at Axelera AI,
he is applying his expertise to the dynamic field of artificial intelligence.

References

Public funding opportunities for the semiconductors industry in the EU

M. Isabelle
CEO & Founder
European economics, PARIS, France

Abstract
The semiconductors industry is among the highest beneficiaries of public funding in the EU. Grants target R&D activities, first industrial deployment of breakthrough innovations and first of a kind manufacturing facilities. Securing such State aid and EU funding is a highly competitive process which requires a thorough understanding of the numerous opportunities and associated regulations. Based on several use cases, Marc Isabelle's presentation will provide a valuable first dive into public funding opportunities for the semiconductors industry in the EU.

Biography
Marc ISABELLE, engineer & PhD in Economics, is the founder and CEO of european economics.
Marc is a recognised expert in the public funding of strategic projects. Since 2009, he has helped 195 companies secure €43 billion in public funding for 250 major projects. These initiatives tackle key societal challenges - including disruptive innovation, decarbonisation, resilience and infrastructure - across a wide range of industrial sectors including microelectronics, software, telecoms, automotive, energy and environment, batteries, pharmaceuticals and biotech.
Through his extensive work with the European Commission and national authorities, Marc has actively contributed to shaping the methodologies and best practices used to assess public funding applications and their compatibility with EU regulations.
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References