III-V Summit

BTO-enhanced Silicon Photonics for Next-Generation Optical Transceivers

F. Mohn
Reliability and Packaging Lead
Lumiphase AG, Stäfa, Switzerland

Abstract
As global data traffic continues to surge, the demand for faster, more energy-efficient, and scalable optical communication systems is driving the need for innovation in photonic integration. Traditional silicon photonics, while mature, faces limitations in speed, power consumption, and footprint.
Lumiphase addresses these challenges by developing and manufacturing photonic integrated circuits based on a proprietary barium titanate (BTO) technology. This technology uses the Pockels effect and enables true electro-optic modulation, offering significant advantages over conventional silicon-based solutions.
In this presentation, we will introduce our BTO-based photonic integration technology, highlight its advantages for optical data communication, and discuss key challenges and ongoing developments in bringing this technology to scale.

Biography
Fabian Mohn is a Staff Engineer and team lead of the Reliability & Packaging team at Lumiphase. The team is responsible for wafer-to-chip singulation processes, the design and assembly of test vehicles for chip-level performance and reliability evaluation, and the development and execution of accelerated reliability and robustness qualification protocols for Lumiphase's BTO-based silicon photonics devices.
Fabian holds a PhD in Physics, which he earned in 2012 while working at IBM Research – Zurich. Before joining Lumiphase in 2022, he worked on the development of silicon and silicon carbide power semiconductor modules, gaining extensive experience in packaging and reliability engineering.

References

III-V Engineered Substrates, beyond classical SOI substrates

C. Roda Neve
R&D Program Manager
SOITEC, Hasselt, Belgium

Abstract

For the forthcoming generation of wireless communication systems, high-frequency electronics, and advanced radar architectures, there is a pressing need for substrate technologies that surpass the inherent limitations of conventional silicon (Si) and silicon-on-insulator (SOI) platforms. Engineered substrates that incorporate emerging compound semiconductors—most notably gallium nitride (GaN) and indium phosphide (InP)—offer a unique opportunity to harness superior electron transport properties, enhanced thermal conductivity, and scalable integration, while simultaneously enabling precise control over dielectric and thermal management. The successful integration of III–V semiconductors onto advanced engineered substrates relies on a combination of innovative approaches, including direct bonding, layer transfer, and heterogeneous integration strategies. These techniques not only pave the way for optimized RF device performance but also address critical challenges associated with material availability, manufacturability, and cost competitiveness, thereby accelerating the large-scale commercialization of III–V-based wireless technologies. Particular emphasis is placed on application-driven advances spanning millimeter-wave communications, 5G/6G front-end modules, satellite and aerospace electronics, and high-power amplifier technologies. In this work, we provide an overview of the most recent developments in the design and fabrication of III–V engineered substrates, and outline their prospective roadmap toward industrial adoption and widespread deployment in future RF applications.

Biography

Cesar Roda Neve received his Msc. Engineer degree from the ICAI Universidad Pontificia de Comillas, Madrid, Spain, in 2000. In 2004 he joined the University Carlos III of Madrid where he worked on optoelectronic devices for ROF links. In 2006 he joined the Microwave Laboratory of the UCLouvain, Belgium, where he specialized on the use of Si-based substrates for RF applications, in particular trap-rich HR-SOI. He received his Ph.D. degree by UCLouvain in engineering sciences in 2010. Since then, he has worked on R&D and new technologies development at several companies and for a wide variety of topics, from RF and large signal characterization, 2.5D/3D integration, to GNSS and UAV/satellite communications. In 2021 he joined Soitec as R&D Program Manager, working on strategic research applications and emerging technologies, focusing on quantum technologies and applications, as well as on RF, 6G, and advanced CMOS technologies.

References

Silicon Carbide in AC Motor Drives

J. Puukko
Senior Field Application Engineer
Semikron Danfoss, Helsinki, Finland

Abstract
With recent technological advancements, silicon carbide is becoming the first choice for enabling energy savings and increasing power density. However, motor drives and silicon carbide MOSFETS are two topics that seemed impossible to combine: high costs, fast switching transitions, lack of short circuit capability, and reliability concerns were all persistent roadblocks, preventing a tangible return on investment. But it is time to rethink. By merging state of the art packaging technology with the latest generation of SiC MOSFETs, we provide a totally new degree of design freedom to motor drive design engineers.

Biography
biography

References

Strategic advances in III-V RF Technologies for energy-efficient 5G infrastructure

G. U'Ren
Senior Technical Expert
United Monolithic Semiconductors (UMS),
Villebon-sur-Yvette, France

Abstract

III-V semiconductor technologies, including GaAs and GaN/SiC, are at the core an effort lead by UMS to strengthen European sovereignty in advanced rf components for terrestrial and non-terrestrial 5G due to their unrivaled performance in high-frequency, high-power, and high-linearity applications. This talk will highlight the strategic role of III-V technologies in enabling energy-efficient RF front-ends and system-in-package (SiP) solutions, addressing the growing demands of 5G and SATCOM networks. By combining advancements in MIMC device technology, innovative device architectures, and heterogeneous integration, the ambition is to realize a 40% reduction in power consumption across the full radio link. Efficiency gains in the network reduce operating costs from the combination of reduced energy consumption and reduced thermal management.

Biography

Dr. Gregory U'Ren is presently with United Monolithic Semiconductors (UMS) leading strategic innovation initiatives. He has held both leadership and individual roles contributing to the advancement of a broad range of specialty technologies including SiGe BiCMOS, RF-SOI, MEMS, and GaN. He is a senior member of IEEE, presently also serving on the advisory board at the Fraunhofer Institute for Applied Solid State Physics, a member of American Physics Society, and holds over 30 patents. He completed his Ph.D. and MS at the University of California Los Angeles.

References

JePPIX: The joint European platform for photonic integrated components and circuits

K. Williams
Professor
Technical University Eindhoven, Eindhoven, The Netherlands

Abstract
Integrated photonics offers us the way to a faster, more precise and more energy efficient future. The sustained growth of the internet is already critically dependent on photonic integrated circuits. Photonic integrated circuits (PICs) are now emerging in industry labs for imaging and metrology with precision, size, and they are showing efficiencies which can be orders of magnitude beyond non-integrated technologies. Supply chains are now aligning to support product developments across many market sectors.

JePPIX - the Joint European Platform for Photonic Integrated Components and Circuits - is a vibrant community of foundries, software vendors, testing experts, packaging companies, technology innovators, equipment suppliers and PIC-enabled module developers. Together they play a key role in defining the road to commercialization in new and emerging sectors. JePPIX is a pioneer of the open-access foundry model for integrated photonics - specifically indium phosphide but also heterogeneous approaches - enabling the end-user to drive product development. Companies and researchers have already been prototyping using commercial JePPIX services for more than a decade. Product developers are focussing on metrics critical to quality, reproducibility, reliability and the seamless interconnection of accelerated design-fab-test cycles which are required to prepare a design for production.

Going forwards, strategies are being developed to accelerate design through the delivery of manufacturing excellence within sustainable commercial value chains. The telecommunications sector has already shown how premium PIC technology can be delivered. The next wave of product innovation is more diverse in terms of platforms, components, and circuits. Foundry manufacturing offers a compelling route to accelerated deployment of products across multiple sectors. We will elaborate the future challenges and perspectives for research and innovation for PIC technologies.

Biography
Kevin Williams is full professor and chair of the Photonic Integration research group at Eindhoven University of Technology (TU/e). He has extensive experience in the design, fabrication and measurement of InP based photonic devices and integrated circuits, including semiconductor lasers, amplifiers, high speed modulators and photonic switches. Kevin was coordinator for the EC JePPIX Pilot Line which matured the full supply chain from software, design, production and test for foundry based PIC manufacturing. The team has played a key role in establishing the Photonic Integration Technology Centre and plays an active role in the Chips JU PIXEurope project.

References

Photonic Integrated Circuits (PIC) – Unique PVD solutions helping turn cost effective high volume manufacturing into reality

M. Tschirky
Senior Manager Strategic Marketing, VP
Evatec AG, Trübbach, Switzerland

Abstract
The growing need for Photonic Integrated Circuits requires breakthroughs in manufacturing in order to go into high volumes. While various deposition technologies are state-of-the-art in institutes and R&D, the industry needs scalable and robust solutions to fulfill the demands given by the massive increase of computation and communication.
Evatec – The Thin Film Powerhouse – has a long history in both Semiconductor and Photonic Industries and is able to combine the best of these worlds.
By analyzing the materials of interest and evaluating their desired properties, we are able to combine specific tool features and material behaviors and offer PVD-solutions for most of the common materials used for active and passive building blocks of PICs. Waveguides from Silicon Nitride and Aluminium Nitride as well as modulators from Lithium Niobate and Barium Titanate can now be deposited reliably in high volumes on industry-proven platforms for substrates up to 300mm.

Biography
Maurus Tschirky is Senior Strategic Marketing Manager and Vice President at Evatec. He is globally responsible for Strategic Marketing and Business Development across the entire portfolio of market segments. His genuine interest in deposition technology and its applications for more than Moore typologies emphasizes his dedication to the 3D Heterogeneous Integration market in particular. Over 20 years, Maurus had a number of positions in the PVD-equipment industry (Balzers, Unaxis, Oerlikon and now Evatec) ranging from Application Engineer, System Engineer, Project Manager to Product Manager over the years and also spent 3 years leading a research section at CSEM in Landquart, Switzerland. He has a first Degree in Control Electronics from the University of Applied Sciences in Buchs, followed by a Master in Business Engineering / International Marketing from the Hochschule für Wirtschaft und Technik in Zurich, Switzerland.

References

Title: Designing Chiplets & 3DIC for Silicon Lifecycle Management

Y. Zorian
Technical Fellow
Synopsys, Inc., Sunnyvale, United States of America

Abstract

Recent advances in Artificial Intelligence accelerators, automotive systems, and high-performance computing (HPC) in data centers have led to an acceleration in the adoption of advanced chiplets and 3DIC packaging technologies. This course will present today's trends in high-end electronic systems and their needs for advanced chiplets and 3DIC systems and concentrate on the resiliency challenges and solutions for such chiplets and 3DIC systems. It will introduce the key concepts and terminology concerning the above issues, summarizing the main solutions adopted to minimize the probability of faulty circuits to reach the operational phase, and to mitigate the effects of possible faults affecting the circuits in the field.

Biography

Dr. Yervant Zorian is a pioneering engineer and technology leader renowned for his contributions to the fields of electronic design automation and test technologies. With a distinguished career that spans academia and industry, Dr. Zorian has made significant contributions to the development and implementation of innovative testing techniques for complex integrated circuits. As a prolific author and inventor, he has contributed to numerous publications and patents in the field. Dr. Zorian has also served in various leadership roles within professional organizations, furthering the advancement of technology and knowledge in his areas of expertise. Zorian won the 2005 Hans Karlsson Award and is a Chief Architect and Fellow at Synopsys.

References