Innovation Showcase (pre-recorded)

High Throughput Thin Film Coatings combining Maximal Uniformity and Minimal Defects for the Future of Acoustic Wave applications

D. Pereira
Bühler Alzenau GmbH, Semiconductor, Alzenau, Germany

Abstract
The evolution of RF filters for 5G has driven significant advancements in acoustic wave filter design and manufacturing, with several structures now widely tested and adopted in mass-market applications. The more recent trend is towards building Surface Acoustic Wave (SAW) filters on Piezo-on-Insulator (POI) wafers, a technology that extends performance into higher frequency bands essential for 5G. Challenges arise on the production of defect-free, high density oxides that couple to the piezoelectric materials (like $LiTaO_3$ or $LiNbO_3$) or on the supersmooth surfaces required for the production of the devices, particularly as pitch sizes decrease to accommodate higher frequencies.
In this presentation, we explore the challenges associated with the manufacturing of SAW filters on POI substrates. We focus on how Bühler Leybold Optics' Semiconductor portfolio leverages decades of expertise in optics thin-film processing to address the complexity of next-generation RF devices. With emphasis on advanced thin-film deposition and planarization methods - including Magnetron Sputtering, Ion-Beam Assisted Deposition, and Ion Beam Trimming - these ensure mass-production solutions for the creation of consistent, high-quality films with minimal defects and maximal uniformity. These techniques not only enhance the performance and reliability of acoustic wave filters but also enable efficient processes such as wafer-to-wafer bonding, a critical requirement for POI technology.

Biography
Daniel Sá Pereira joined Bühler Leybold Optics in 2021 working on the Semiconductor Market Segment as a technical Sales Manager. Daniel is a Microelectronics Engineer from the New University of Lisbon, Portugal (2015) and a PhD in Physics from the University of Durham, United Kingdom (2019). His research focused on the characterization of organic materials for application in organic light emitting diodes (OLEDs). Since leaving academia, Daniel has joined Business Unit Optics at Bühler Alzenau GmbH to focus on emerging applications that combine the worlds of Optics with Semiconductor like Augmented Reality, RF Communications, Photonic Integrated Circuits, Ambient Light Sensors, etc.

References

Strategic Raw Materials and Sustainability: The Importance of Hyperpure Silicon.

M. Bünnig
Wacker Chemie AG, Burghausen, Germany

Abstract
WACKER Chemie AG is the global market, technology and quality leader for hyperpure silicon. Hyperpure silicon is the enabling material for silicon wafers. In 2023 Wacker started to invest once more in our hyperpure silicon capacities and capabilities. Therefore, Wacker is part of the public funded IPCEI ME/CT (Important Project of Common European Interest for Microelectronics and Communication Technologies) program with our strategic investment project "**Etching Line Next**" in Germany, Burghausen. Within this project, WACKER develops and deploys an innovative etching process for hyerpure silicon combined with a novel pre-treatment via thermal crushing and an innovative automated morphology sorting. This will result in an innovative silicon that will specifically meet future technical requirements to allow production of future leading-edge devices. We want to talk about the innovations of the project and in general about sustainable and challenging production of hyperpure silicon.
These includes:

- How to improve product quality and enabling the production of hyperpure silicon at constant level,

- why hyperpure silicon enables the production of 300 mm wafers and why it is essential for future microelectronic applications,

- how to face cost challenges e.g. energy costs with a high degree of automation and enhances sustainability in several respects.

With hyperpure silicon being a strategic key raw material for semiconductors we are going to showcase how our investment project will contribute to a resilient European semiconductor supply chain while further supporting sustainability strategies and green technologies in the industry and therefore how hyperpure silicon in general contributions to a sustainable future.
As hyperpure silicon for semiconductor application is the indispensable base for the global electronic value chain and the continuously growing market pushed by digitalization and decarbonization and ever tighter technical requirements trigger the same trend on the silicon supply side – growing demand and increasing technical requirements while also focusing on sustainability. All these challenges will be addressed in our pre-recorded talk.

Biography
Professional Career
Since March 2023 back with WACKER
Senior Marketing Manager for Polysilicon

Wacker Chemie AG, 2011 - 2021
Sales Manager Silicones for Customers in Energy Sector in DACH-Region

Walter De Gruyter, 2021 - 2022
Senior Manager Book Production and Team Lead

Education
Humboldt-Universität zu Berlin, 2020 - 2023
Master of Arts - MA, Philosophie

Steinbeis University, 2014–2016
Master of Business Administration (M.B.A.), Marketing

University of Applied Sciences, 2005 - 2011
Diploma Industrial Engineering

References

Rethinking Chip Design with Open Source EDA

C. Alexandre
keplertech.io, Paris, France

Abstract
The rise of open source hardware, driven notably by RISC-V adoption, is generating growing interest in more open and flexible Electronic Design Automation (EDA) tools. Despite this momentum, the EDA landscape remains largely proprietary — with critical stages of both digital and physical design flows controlled by a small group of vendors. This limits reproducibility, collaboration, accessibility, and innovation.
Unlike cloud or AI software stacks — where open source has become foundational — semiconductors and EDA have remained predominantly closed. But that paradigm is beginning to shift. A growing community of contributors and increasingly capable open source EDA projects are forming a viable ecosystem with real-world applicability.
This talk will explore how open source EDA can be effectively leveraged today — not as a full replacement for industrial tools (at least not yet), but as a complementary layer that provides value in specific, practical contexts:
- CI/CD for open hardware projects, enabling community-driven regression testing with license-free flows.
- Early-stage architecture exploration and prototyping for SMEs, academic teams, startups, and newcomers — without requiring access to commercial toolchains.
- Cloud-native flow scaling, where open licensing enables elastic, parallel experimentation on standard compute infrastructure.
We will also highlight the contribution of keplertech.io, and introduce Naja — a modular C++/Python framework for post-synthesis netlist analysis, optimization, and EDA tool development.
I will also consider the strategic relevance of open source EDA in the European context — how it can reduce dependency, foster innovation, enable reproducible flows, and support skills development, all of which are critical to Europe’s pursuit of greater semiconductor sovereignty.

Biography
Christophe Alexandre, Keplertech.io
With 20 years of experience in Electronic Design Automation (EDA), I began my journey with a PhD in microelectronics from Sorbonne University (2008). In 2009, I co-founded Flexras Technologies, a startup specializing in FPGA prototyping tools, which was acquired by Mentor Graphics (now Siemens EDA) in 2015. There, I served as Chief Software Architect, leading global R&D teams and helping evolve our technology into a widely adopted commercial product.
In 2022, I co-founded a new venture: keplertech.io, an EDA startup built on the belief that Open Source can unlock innovation in one of the most closed and complex industries—semiconductors, integrated circuits, and the tools used to design them. In a space dominated by a handful of major players, we aim to create meaningful opportunities for smaller, agile actors to thrive.
I’m passionate about building complex systems from scratch and bringing ideas to life in the real world.
LinkedIn: https://www.linkedin.com/in/christophe-alexandre-634bb36
Mastodon: https://mastodon.social/@xtofalex
naja GitHub: https://github.com/najaeda/naja

References

Innovative Etching Gas Development using Digital Twin

N. Ichikawa
Daikin Industries, Ltd., Chemicals Division,
Product R&D Department, Settsu,Osaka, Japan

Abstract

Author**:** Natsumi Ichikawa[1], Hisataka Hayashi[1], Simon Pelz[2], Julian Rechman[2]
[1]Daikin Industries, Ltd. and [2]Daikin Chemical Europe GmbH

In the semiconductor industry, advancing device miniaturization and integration demands improved performance. The stringent requirements for dry etching, crucial to device function, pose technical challenges. As a chemicals manufacturer, we address these with gases, but exploring optimal process conditions (applied power, gas flow rate, pressure) is time-consuming. To approach these issues, we adopted inductively coupled plasma etcher and capacitively coupled plasma etcher mirroring those in the 300mm mass production process. These etchers allow replication of issues using latest pattern wafers from client, alongside the ability to rapidly evaluate multiple gases due to the tool's stand-alone nature and user-friendly gas cylinder replacement. Leveraging this equipment and digital twin technology, we've innovated a method to optimize new gas capabilities. Utilizing Design of Experiments (DOE) and Machine Learning (ML), we've created a precise model predicting etching characteristics (profile and depth). Digital twin technology facilitates virtual experiments to find optimal conditions. In developing a C_4F_8 (GWP: 10300) alternative for the Bosch process, DOE shortlisted 19 conditions from 54. The digital twin, simulating 1960 conditions, identified $CH_2{=}CF_2$ (GWP: 0.052) as a promising alternative in a region distinct from C_4F_8's conditions, achieving optimal results for $CH_2{=}CF_2$.

To construct a more accurate prediction model, we also focused on plasma physical quantities such as electron and ion density, which represent the plasma state during etching. Unlike traditional ML that uses only process conditions incorporating plasma physical quantities significantly improved model precision. In optimizing conditions where SiO_2 etching rate exceeded 400 nm/min and SiO_2/Si selectivity reached 4 via CF_4 with H_2 incorporation, ion density inclusion, measured via quadrupole mass spectrometry, cut prediction error from 7.4% to 1.9%. These findings, presented at conferences such as DPS2024, are widely acclaimed. Our ongoing mission is to swiftly and effectively contribute to the semiconductor sector by developing new gases and process conditions using digital twin technology.

Biography

Natsumi Ichikawa is currently a chemical researcher at Daikin Industries. She holds a Master's degree in Catalytic Chemistry. She has strengths in synthetic and complex chemistry. Currently involved in semiconductor dry etching process, speciallizing Bosch Process and digtal twins.

References

Unlocking the potential of GaN-Si: Advancing 5G+/6G communication and power electronics

N. Collaert
Imec, Leuven, Belgium

Abstract
Gallium Nitride on Silicon (GaN-Si) has emerged as a transformative technology for next-generation communication and power applications, offering a compelling balance between performance, cost, and scalability. In the realm of 5G+/6G communication infrastructure and handset applications, GaN-Si demonstrates significant promise with its ability to achieve high power density, efficient amplification, and compatibility with existing silicon manufacturing processes. Its scalability to larger wafer sizes provides a cost-effective alternative to GaN-SiC, particularly for base station infrastructure requiring operation at 28V and 48V. However, challenges such as thermal management, substrate losses, and achieving enhancement-mode (E-mode) devices for handset applications necessitate continuous innovation in materials and device architectures.

For power electronics, GaN-Si has transitioned to mass production, delivering breakthroughs in efficiency and performance across a broad voltage range. Yet, as the technology matures, the research community is addressing critical challenges to expand its voltage range, improve integration levels, and enhance reliability under real-world conditions. This presentation outlines our roadmap for addressing these challenges through novel device designs, advanced substrates, and integration of new components. By balancing short-term industrial needs with long-term innovation, we aim to unlock the full potential of GaN-Si technology, driving advancements in high-frequency communication systems and energy-efficient power solutions.

Biography
Dr. Nadine Collaert is an imec fellow and part-time professor at the Vrije Universiteit Brussel (VUB). She is currently responsible for the advanced RF program looking at heterogeneous integration of III-V/III-N devices with advanced CMOS to tackle the challenges of next generation mobile communication. Before that, she was program director of the LOGIC Beyond Si program focused on the research on novel CMOS devices and new material-enabled device and system approaches to increase functionality. She has been involved in the theory, design, and technology of FinFET devices, emerging memories, transducers for biomedical applications and the integration and characterization of biocompatible materials. She has a PhD in electrical engineering from KU Leuven and she holds more than 500 publications and more than 15 patents in the field of device design and process technology.

References

Fabrication of Recrystallized SiC Wafer Carriers via Additive Manufacturing and CVI

Y. Jung
MADDE Inc., Seoul, Republic of Korea (South Korea)

Abstract

To address the limitations of conventional silicon carbide (SiC) manufacturing—such as high-temperature sintering, significant shrinkage, and restricted geometry—we present a novel process that enables the production of high-performance recrystallized SiC (R-SiC) components for semiconductor equipment. This approach combines binder jetting additive manufacturing (BJAM) with chemical vapor infiltration (CVI) to rapidly produce complex wafer carriers (baffle boats) with excellent thermal stability and dimensional accuracy.

The process begins with the fabrication of porous green bodies using a custom-developed BJAM system tailored for SiC powders. These printed parts feature complex internal geometries and are subsequently densified through vapor-phase SiC deposition via CVI. Unlike conventional R-SiC fabrication that relies on high-temperature processing and mold-based shaping, this method achieves densification under lower thermal conditions while enabling precise control over residual porosity. The result is improved mechanical strength, reliable shape retention, and minimized material waste.

Using this approach, we successfully manufactured wafer carriers in a fast and cost-effective manner. The printed R-SiC components demonstrated strong thermal shock resistance and dimensional stability under repeated exposure to high-temperature process environments. By combining the geometric freedom of additive manufacturing with the functional reliability of R-SiC, this process offers a scalable and economically viable pathway for next-generation ceramic components in semiconductor manufacturing.

Biography

Youngsuk Jung is the CTO and co-founder of MADDE, a company developing advanced additive manufacturing technologies for both ceramics and metals. He holds a Ph.D. in Automotive Engineering with a specialization in structural design optimization. Prior to founding MADDE, he conducted research on design for additive manufacturing at Hyundai Motor Company. His current work focuses on the development of customized 3D printers and design methodologies optimized for the additive manufacturing of high-performance industrial components.

References

Driving ICT Decarbonisation: Unlocking the Power of Product Carbon Footprint Insights

A. Yague
Manager
Carbon Trust, London, United Kingdom

Abstract

As 2030 approaches and ICT sector confronts mounting climate pressures, hyperscalers are increasingly requesting Product Carbon Footprints (PCFs) from their semiconductor and component suppliers. While this growing demand can pose a challenge for semiconductor companies—many of which have complex supply chains—it also represents an opportunity. This presentation will explore why product-level carbon insights are becoming essential, and how they can unlock new paths to decarbonisation, innovation, and competitive advantage.

Focusing on both the semiconductor industry and the broader ICT sector, the Carbon Trust will explain how PCFs can be robustly calculated, clearly communicated, and effectively leveraged. We will explore how high-quality, transparent PCFs can drive emissions reductions, inform better design and procurement decisions, and align with evolving regulatory and customer expectations.

This session is both a call to action and a practical guide. Attendees will gain insight into starting, or strengthening, their PCF journey, whether to ensure compliance, enhance corporate sustainability strategies, or contribute meaningfully to the sector's collective decarbonisation goals.

Biography

Andrew is the European ICT Regional Practice Area Head for the Carbon Trust, a global climate consultancy with the mission to accelerate the move to a decarbonised future. He primarily supports clients in the ICT and technology sectors set science-based targets, develop decarbonisation strategies and roadmaps and look beyond their value chain at how their products and services are driving emission reduction impacts more globally.

Andrew leads Carbon Trust's work in the semiconductor sector, which covers work with semiconductor industry associations, equipment manufacturers, chip design, foundries and IDMs. Andrew graduated from Trinity College Dublin with a degree in Computer Science and Language. He has spent the majority of his career in Technology and Renewable Energy. He is also fluent in English, Spanish and French.

References

Hybrid flexible electronics for Smarter, Safer Electrification with Battery Systems

R. Pedroso
Researcher
CeNTI, Smart Materials, Vila Nova de Famalicão, Portugal

Abstract
As electric vehicles continue to drive demand for high-power fast-charging infrastructure, the energy storage systems that support these chargers are subjected to increasing thermal and electrical stress. While traditional low-voltage storage remains common in residential applications, fast chargers require more advanced battery systems with precise and responsive thermal management. A persistent challenge in these systems is accurate temperature sensing at the cell level. Conventional thermal sensors are often sparsely placed and loosely integrated within battery modules, resulting in limited spatial resolution and delayed thermal response. This compromises the performance of battery management systems (BMS), impeding their ability to monitor critical cell conditions and assess battery health in real time.
One promising solution developed within this project is a **hybrid temperature sensor** that combines printed conductive paths with NTC thermistors. The developed approach leverages the **flexibility and scalability of printed electronics** to distribute sensing across multiple cells **with reduced number of readings** while maintaining the **precision and reliability** established for battery systems. By minimizing the number of measurement points while improving coverage and integration, this hybrid sensor system offers enhanced thermal insight with minimal disruption to module design. The result is a safer, smarter, and more responsive energy storage platform tailored for the demanding conditions of fast-charging applications.
This work was developed within the scope of the project “NGS – New Generation Storage” [C644936001-00000045], financed by PRR – Plano de Recuperação e Resiliência under the Next Generation EU from the European Union.

Biography
Rúben Pedroso holds a Master's degree in Physics from the Faculty of Sciences of the University of Porto (FCUP). He is currently a researcher in the Smart Materials department and is responsible for projects, numerical analysis, and electrical characterization of systems. He works on R&D projects (both national and European), focusing on the research and development of electrical systems for sensing, energy generation, and energy storage. Nowadays he is responsible for the Thin Films and Microfabrication team, which works with vacuum desposition techniques and microfabrication of systems and devices in a cleanroom environment.

References

Empowering Next-Gen Semiconductor Innovation with the 3DEXPERIENCE Platform

S. Joshi
Technical Solution Senior Manager for
Semiconductor Industry (High-tech)
Dassault Systemes, Velizy, France

Abstract

The semiconductor industry plays a pivotal role in enabling the adoption of new technologies and addressing bottlenecks in their implementation. This industry is currently experiencing rapid growth and technological innovation, driven by increasing demand in sectors such as AI, automotive (especially electric and software-defined vehicles), 5G, and consumer electronics. The complexity of advanced technologies needs the collaboration across the entire ecosystem, from materials and equipment suppliers to design and manufacturing partners. This collective effort drives innovation and ensures that the increasing demands of the digital world are met. This type of collaboration goes beyond the semiconductor fab, bringing together designers, OEMs, and foundries—all of whom gain from a platform that offers distinct value.

In this talk, we introduce a model-based systems engineering approach-based platform i.e; 3DEXPERIENCE platform. It addresses key challenges in semiconductor development by enabling the design and manufacturing of complex, multi-domain chips through cloud collaboration, virtual twin simulations, and streamlined workflows. This comprehensive platform helps overcome growing design complexity, silos, and supply chain inefficiencies—ultimately supporting faster innovation, improved performance, and reduced time-to-market for next-generation semiconductor solutions.

Biography

Smriti is currently working as a Technical Solution Senior Manager for Semiconductor Industry (High-tech) with Dassault Systèmes. She is responsible for understanding, consolidating and driving semiconductor technical solutions. She develops new solutions and provide enablement worldwide for semiconductor customers. She has over 15 years of R&D experience working with different foundries ST Microelectronics, Altis Semiconductor, X-FAB and research lab like CEA –LETI and Lip6 (U.P.M.C.).She received her **Doctoral (Ph.D) degree** in **Nanoelectronics and Nanotechnolgy** from Institut Polytechnique de Grenoble (France) in 2013.

References

New Semiconductor-Plattform for Resource-efficient Neuromorphic Computing – the TiF Transistor and the TiF Memristor

H. Krüger
Friedrich-Schiller Universität Jena, Institut für Festkörperphysik, 07743 Jena, Germany

Abstract
Energy consumption of classical ICT systems in von-Neumann architecture is expected to rise from 1500 TWh (8% of global electricity consumption) in 2010 to 5700 TWh (14% of global electricity consumption) in 2030 [Andrae2020]. New ICT systems, which are inspired by the structure and function of the human brain are needed, so-called neuromorphic architecture. A key aspect of engineering electronic devices for ICT systems in neuromorphic architecture is understanding how the analog plasticity of individual neurons and synapses in the human brain affects the representation and processing of information during learning and development. However, so far only artificial neurons and artificial with digital plasticity could be realized.

TECHiFAB has developed the TiF material platform for building electronic devices which merge data storage and data processing and reveal analog plasticity. In the TiF transistor and in the TiF memristor the threshold voltage and the memristance can be reconfigured in an analog manner, respectively. Apart from TiF transistors, there are no transistors worldwide whose threshold voltage can be configured in an analog manner. For transistors based on other material platforms, e.g. ferroelectric transistors, the threshold voltage can only be configured in a discrete manner. And apart from TiF memristors, there are no memristors worldwide whose memristance can be configured in an analog manner [Schmidt2024]. For memristors based on other material platforms, the memristance can only be configured in a discrete manner.

The reconfiguration of the electronic properties of the TiF transistor and of the TiF memristor can be repeated any number of times (endurance of the write process). The reconfigured electronic TiF device can be operated in the "configured state" for any length of time (retention of the "configured state") without the "configured state" itself changing. The reconfiguration time is in the µs range. Operation in the "configured state" occurs in real time.

The goal of neuromorphic computing is not to perfectly mimic all the function of the human brain, but instead to extract what is known of its structure and operations to be used in a practical computing system. We expect that having artificial neurons and artificial synapses with analog plasticity at hand, the function of the human brain will not be completely mimicked but will be replicable in more details.

Biography
About Prof. Dr. Heidemarie Krüger:

Prof. Dr. Heidemarie Krüger (formerly Schmidt), born on May 17, 1972, is a distinguished physicist specializing in solid-state physics with a focus on quantum detection. She holds a W3 professorship at the Friedrich Schiller University Jena and serves as the Head of the Department of Quantum Detection at the Leibniz Institute of Photonic Technology in Jena, Germany. In 2021, she also founded and became Managing Director of TECHiFAB GmbH.

Prof. Krüger completed her studies in physics at the University of Leipzig, where she earned her diploma in 1995. She went on to obtain her Ph.D. in physics in 1999 under the supervision of Prof. Dr. K. Kreher. Her academic career progressed with a habilitation in experimental physics completed in 2008, mentored by Prof. Dr. M. Grundmann. She was awarded the venia legendi (teaching license) in experimental physics in 2013.
Her professional journey reflects a consistent focus on nano-spintronics and quantum technologies. After several years as a postdoctoral researcher and junior group leader at the University of Leipzig and

Helmholtz-Zentrum Dresden-Rossendorf, she led research groups at Technische Universität Chemnitz and Fraunhofer ENAS. Since 2017, she has held her current dual leadership roles at FSU Jena and the Leibniz-IPHT.

Prof. Krüger has received numerous prestigious awards and grants, including a Heisenberg Fellowship from the German Research Foundation (DFG) in 2011 and the Fraunhofer ATTRACT Grant in 2016, worth €2.1 million. Earlier in her career, she won the BMBF's NanoFutur Prize in 2002 for her groundbreaking work in nanoelectronics.

An accomplished researcher, Prof. Krüger has authored over 220 peer-reviewed scientific publications, accumulating more than 4,500 citations and achieving an h-index of 35. She is also a prolific inventor, holding multiple patents in areas such as memristive devices, non-volatile memory, and biochip technology. Her academic mentorship includes supervising over 40 Bachelor's, Master's, and doctoral theses, contributing significantly to the training of the next generation of scientists.
Prof. Krüger has been an active member of several professional organizations, including the Deutsche Physikalische Gesellschaft (since 1995), the Materials Research Society, and various interdisciplinary advisory committees. Her work is characterized by a unique integration of materials science, device physics, and applied quantum detection technologies, often with biomedical or neuromorphic computing applications.

In addition to her scientific achievements, Prof. Krüger is a mother of four and has balanced a demanding research career with family responsibilities, having taken parental leave in 1993, 1995, 1998, and 2008.

About TECHiFAB GmbH:

Techifab was founded in 2021 by Prof. Dr. Heidemarie Krueger and Stephan Krueger and develops the platform technology for neuromorphic chips based on a novel semiconductor material (TiF platform technology). The start-up from Germany's Silicon Saxony region addresses key weaknesses in traditional semiconductor architectures and offers a new, highly energy-efficient alternative for AI, robotics, cyber security and communication technologies.
Techifab currently employs around 50 people at its Dresden headquarters. With 24 registered patents and over EUR 20 million in investments to date, the company is one of the most promising representatives of the European DeepTech scene. The first memristor components, including administration software, have been available as a proof of concept since 2024.

Sources for Abstract:

[Andrae2020] A. S. G. Andrae, Eng. Appl. Sci. Lett. 3, 19–31 (2020)

[Schmidt2024] H. Schmidt, Prospects for memristors with hysteretic memristance as so-far missing core hardware element for transfer-less data computing and storage, J. Appl. Phys. 135, 200902 (2024)

References

The Relevance of Metrology & Inspection in Advanced Packaging of Devices for AI applications

D. Alliata
Sr. Director of Applications
Merck Electronics, Metrology & Inspection,
Montbonnot-Saint-Martin, France

Abstract
The complexity of the last generation AI devices requires non-conventional fabrication approaches. With the explosion of cost at the most advanced front-end part of the manufacturing process, advanced packaging (AP) has become a key differentiator for achieving next-generation requirements, and thereby continued sustainability, in the semiconductor industry. Cost leveraging is now reachable with the integration of multiple dies in the same package, each one fabricated to handle specific functionalities with the most cost-effective technology node, which is a form of heterogeneous integration. Within the advanced packaging realm, platforms such as fan-out wafer-level packaging (FOWLP) and enabling technologies such as Through Silicon Via (TSV), fine pitch micro-bumping, and ultra-thin wafer thinning, are gaining momentum due to their high integration, extreme flexibility, performance enablement and solution cost advantages, compared to more conventional assembly technologies. In addition, in an effort of improving the efficiency of the manufacturing process and reduce the waste of materials, the semiconductor packaging community starts to adopt square carriers at the place of traditional round wafer substrates. This session deeply discusses some examples of metrology and inspection solutions aimed at securing the manufacturability of devices for High Computing Power fundamental for AI applications. More in detail, it explores the challenge of the fabrication of chip-to-chip interconnections that are key for the heterogeneous integration of active components with vertical stacking like DRAM for High Bandwidth memories, where process tolerances are increasingly narrow and conditions to measure more and more extremes

Biography
Dr. Dario ALLIATA joined Unity-SC, now EMD Electronics, the Electronics business of Merck KGaA, Darmstadt, Germany in the U.S. and Canada. In 2016 as product manager and is now Sr. Director of Applications with focus on Advanced packaging and Specialty substrates & devices. He worked in the semiconductor industry for more than 25 years, initially in R&D centers and later in equipment makers. He spent his entire career developing process control solutions for securing the manufacturing chain in the semiconductor industry. He received a MD in Physics from the University of Milan (Italy) and hold a Ph.D. in Physics & Chemistry from the University of Berne (Switzerland)

References