Advanced Packaging Conference

Welcome Remarks

L. Altimime
President
SEMI Europe, Berlin, Germany

Abstract
Welcome Remarks

Biography
Laith Altimime, as President of SEMI Europe, leads SEMI's activities in Europe and the Middle East and Africa (EMEA). Altimime has P&L responsibility as well as ownership of all Europe region programs and events, including SEMICON Europa. He is responsible for establishing industry standards, advocacy, community development, expositions, and programs. He provides support and services to SEMI members worldwide that have supply chain interests in Europe. He manages and nurtures relationships with SEMI members in the region and globally as well as with local associations and constituents in industry, government, and academia. Altimime has more than 30 years of international experience in the semiconductor industry. Prior to joining SEMI in 2015, He held senior leadership positions at NEC, KLA-Tencor, Infineon, Qimonda, and imec. Altimime holds an MSc from Heriot-Watt University, Scotland.

References

Europe’s Position in Advanced Packaging: Market Dynamics, Technology Trends, and Strategic Outlook

R. Fraux
Chief Research Officer
Yole Group, Nantes, France

Abstract

Advanced packaging has become a key differentiator in semiconductor performance and system integration. By enabling higher density, lower power consumption, and improved thermal management, technologies such as 2.5D and 3D integration, chiplet architectures, and heterogeneous packaging are reshaping both product design and manufacturing strategies across the global semiconductor industry.

Based on Yole Group’s continuous market monitoring activities, this presentation provides an updated view of the advanced packaging market and Europe’s position within it. Global packaging revenues are expected to exceed $140 billion by 2030, driven by computing, AI, and automotive applications that increasingly rely on system-level integration. Europe currently represents about 8% of the total market, with strong industrial bases in automotive, telecom, industrial, and defense sectors. However, most packaging production remains concentrated in Asia, highlighting both structural dependencies and opportunities for European investment and collaboration.

The analysis reviews key technology trends, including hybrid bonding, fan-out, and system-in-package solutions, and their adoption potential across different European ecosystems. It also discusses the strategic factors shaping Europe’s competitiveness, such as the role of IDMs, OSAT partnerships, materials and equipment suppliers, and public support mechanisms aimed at reinforcing local value creation.

Ultimately, the presentation shows how advanced packaging is not only a technological enabler but also a strategic lever to strengthen Europe’s contribution to global semiconductor performance and innovation.

Biography

Romain Fraux serves as the Chief Research Officer at Yole Group, leveraging his extensive expertise in the semiconductor industry to lead the development of the organization’s global operations.

He oversees a team of analysts dedicated to exploring the semiconductor landscape, encompassing leading edge and specialty technologies as well as semiconductor manufacturing, with the goal of identifying innovations and business opportunities.

Under Romain’s leadership, Yole Group’s international team delivers comprehensive services, including market research, technology and strategy analysis, reverse engineering and cost assessment. These insights empower Yole Group’s clients to make informed decisions about their future business and manufacturing strategies in the semiconductor, photonics, and electronics sectors.

In his cross-functional executive role, Romain represents Yole Group during key client engagements and regularly shares the organization’s strategic vision at leading international conferences. With over 15 years at Yole Group, he has been instrumental in shaping its position as a thought leader in the industry.

Romain holds a bachelor’s degree in Electrical Engineering from Heriot-Watt University in Edinburgh (Scottland), a master’s degree in Microelectronics from the University of Nantes (France), and an MBA (IEMN – IAE, France).

References

The APECS pilot line is powering the evolution of chiplet technologies

R. Aschenbrenner
Director Deputy
Fraunhofer IZM, Berlin, Germany

Abstract
The pilot line for »Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems« (or APECS in brief) is a key part of the EU Chips Act, as it will propel innovation in chiplet technology and enrich the semiconductor research and production capacities in Europe. The institutes cooperating in the Research Fab Microelectronics Germany (FMD) are working closely with other European partners to complete the APECS line and contribute substantially to making Europe more technologically resilient and competitive in the global semiconductor industry. The pilot line will give large industry players and SMEs or smaller start-ups easier access to cutting-edge technology and feed into more reliable and resilient semiconductor value chains.
The presentation will discuss the role of Fraunhofer IZM in the APECS pilot line with its expertise for the hardware integration of chiplet systems. With its access to individual chiplet components, the institute can cover the entire process flow needed to create fully functioning systems. Its researchers are working on modern 300mm interposer technologies, high-density substrates, advanced assembly technologies, and the necessary processes for the advanced heterointegration of highly integrated systems. Fraunhofer IZM is establishing itself as a key partner for system-level heterointegration in Europe with several focus innovations.

Biography
Rolf Aschenbrenner received the B.S. degree in mechanical engineering from the University for Applied Science, Gießen, Germany in 1986 and the M.S. degree in physics from The University of Gießen, Germany, in 1991. Since March 1994 he has been employed at the Fraunhofer Institute for Reliability and Microintegration (IZM), where he is presently the deputy director and head of the Business Development Team.

References

Leveraging Virtual Twins and AI/ML in semiconductor industry using 3DEXPERIENCE platform

S. Joshi
Senior Manager Technical Solution -
Semiconductor Industry
Dassault Systèmes, High Tech, Velizy, France

Abstract

Semiconductor companies optimize every stage of their operations—from research and chip design to production and supply chain—by leveraging a combination of multi-scale virtual twins and artificial intelligence. It helps reducing, downtime, enhance scalability, and improve resource efficiency, contributing to sustainable design and production practices.In this talk, we will present different virtual twins and AI/ML experiences for semiconductor industry. We will present how it can visualize, model and simulate the entire environment of sophisticated experience on a single platform known as **3D**EXPERIENCE. This platform facilitates sustainable business innovation across the full product lifecycle from materials to process to equipment to fab virtual twins.Virtual twins replicate physical objects just like digital twins do, but they take it further, simulating the processes and interactions within an entire system or ecosystem. This could be a game-changer for the semiconductor industry and beyond, offering a more holistic approach to understanding and solving complex challenges. By incorporating real-world data in real-time, virtual twins can support various stages of semiconductor development, from product introduction to end-of-life, by optimizing and streamlining design, manufacturing, and testing processes. It can also accurately model and predict electrical and thermal behavior, and mechanical performance characteristics of the semiconductor device using simulation virtual twins. These simulations can be used to fine-tune designs for optimal performance. Simulation plays a significant role in the virtual twin, allowing companies to test product designs virtually, avoiding the need for costly prototypes. This accelerates development and ensures higher product performance. Additionally, simulation virtual twins can be used to predict real-world performance and understand failure modes, leading to design improvements over time.Along with creating virtual twins, it is very important to have AI-driven chip design and analysis. AI in chip design involves using artificial intelligence techniques, particularly machine learning, to improve the design, verification, and testing of semiconductor devices.

Biography

Smriti is currently working as a Technical Solution Senior Manager for Semiconductor Industry (High-tech) with Dassault Systèmes. She is responsible for understanding, consolidating and driving semiconductor technical solutions. She develops new solutions and provide enablement worldwide for semiconductor customers. She has over 14 years of R&D experience working with different foundries ST Microelectronics, Altis Semiconductor, X-FAB and research lab like CEA –LETI and Lip6 (U.P.M.C.).She received her **Doctoral (Ph.D) degree** in **Nanoelectronics and Nanotechnolgy** from INP Grenoble (France) in 2013.

References

Glass Core Substrates: Driving Scalability for HVM Through A Versatile Process Control Solution

W. Y. Han
Product Marketing Director
Onto Innovation, Wilmington, United States of America

Abstract
Heterogeneous integration packaging technologies have seen increased adoption driven by the rapidly growing demand for advanced end applications like artificial intelligence (AI) and high-performance computing (HPC). Research and development of glass core substrates are gaining momentum due to their superior mechanical stability and ability to enable the fabrication of high-density metal interconnects and the integration of optical interconnects. However, due to the brittle and rigid nature of glass, their adoption also poses significant manufacturing challenges. Stringent process control is required starting from the bare glass panel and throughout the entire glass core fabrication and buildup process to ensure high manufacturing yield and product reliability.

In this presentation, we will present the integration of a high throughput and multifunctional process control solution starting from the fabrication of through glass vias (TGV) in the glass core. Real-time process control of the laser modification and wet etching process is made possible through the ability to inspect and perform CD measurements across 100% of the panel surface. Besides CD monitoring, we will also demonstrate the ability to detect missing and abnormal TGV as these defects can directly impact the electrical performance of the product. Glass is brittle and prone to cracking or chipping during handling and processing. Microcrack detection before and after metallization is crucial to help detect the mechanical damage early to avoid for downstream yield loss.

With its unique integrated metrology and inspection capability, the same in-line process control solution can also be applied throughout the buildup process. From monitoring the defectivity and CD of the traces post-patterning and metallization, to the 3D measurement of RDL/bump height and panel warpage. This enables for real-time response to variations in material, equipment and process conditions and ensure high productivity and manufacturing yield.

To realize the full benefits of glass as a core material for advanced IC substrate to enable high density interconnects, an advanced inspection and metrology solution is vital. Its multi-functionality and flexibility to handle a wide range of panel sizes up to 650mm x 650mm provides the industry a scalable path to bring glass core substrate from research and development to high volume manufacturing by the end of this decade.

Biography
Woo Young Han is a product marketing director for the inspection group at Onto Innovation. He has been with the company since 2000, serving in roles across applications engineering and marketing. Prior to his current position, he led the Applications Engineering group for the inspection business. He holds a degree in Electrical Engineering from the University of Toronto.

References

Advancing Failure Analysis with microPREP® PRO: High-Precision, Automated Laser Sample Preparation for Complex System-Level Analysis

M. Clair
Head of Process Development
3D-Micromac AG, Team Leader Technology and Innovation Management, Chemnitz, Germany

Abstract
The microPREP® PRO system revolutionizes failure analysis by integrating femtosecond laser technology to enable precise, athermal sample preparation at complex system levels. This capability addresses critical challenges in semiconductor and advanced packaging workflows, featuring multi-layered structures composed of heterogeneous materials, such as silicon, polymers, metals, and ceramics, along with dense interconnects, including copper pillars, through-silicon vias (TSVs), and fine-pitch solder bumps. By enabling the preparation of samples that encompass multiple interconnected components or layers within a single preparation step, microPREP® PRO supports comprehensive system-level analysis that captures failure mechanisms spanning diverse materials and interfaces. This enhanced sample handling capability improves defect localization, accelerates root-cause identification, and enhances quality control in high-volume manufacturing environments.
Equipped with advanced automation features, including CAD-based navigation and integrated cleaning systems, microPREP® PRO increases throughput, reproducibility, and reliability, reducing manual intervention and shortening preparation times from hours to minutes. Additionally, its compatibility with correlative workflows enables seamless integration of complementary analytical techniques, fostering a more holistic understanding of device performance and failure mechanisms.
Demonstrated through proof-of-concept and demo deployments, microPREP® PRO offers a scalable, future-ready approach to sample preparation that empowers failure analysis teams to meet the demands of next-generation semiconductor devices and complex systems with unprecedented speed and precision.

Biography
Maurice Clair studied Mechanical Engineering at the University of Technology Chemnitz (Germany). He joined 3D-Micromac in 2005 as a development engineer and is now team leader of the technology and innovation management department. In his current role, he serves as the technical lead for ohmic contact formation on SiC (silicon carbide) materials, a critical area in advancing semiconductor technologies.

Through his expertise in laser technologies, he has been instrumental in the development of innovative laser micromachining processes, including: laser trimming techniques for fine-tuning electronic components with both digital and analogue approaches and beam shaping for ultra-short pulsed lasers.

References

Production-Proven Chemical-Free Green Alternative to Solvent and Piranha Wafer Processing using Ozone

P. Sundin
Business Development Manager
Shellback Semiconductor Equipment,
Coopersburg, United States of America

Abstract
Efforts to implement green technologies in semiconductor manufacturing have historically been slow with acceptance, blocked by perceived concerns over performance risk, operational disruption, and cost. Nowhere is this more apparent than in photoresist stripping, where aggressive chemistries like sulfuric-peroxide mixtures and hazardous solvents like NMP and DMSO remain standard, despite their well-documented environmental burdens. This paper presents a comprehensive assessment of a novel process that offers a rare and timely exception: chemical-free resist removal using ozone gas diffused through heated deionized water.

Unlike ozone-dissolved water systems this method operates in a high-temperature, ozone-rich gas environment. The result is rapid, surface-driven chemical deconstruction of the resist polymer, eliminating the need for persistent oxidizers or solvents, while producing minimal downstream contamination. Comparative lifecycle analysis across chemical input, energy use, waste generation, worker exposure, and effluent treatability reveals a substantial reduction in environmental burden—without compromising technical requirements. Measured CO_2e emissions per wafer are reduced by over 70% relative to sulfuric-peroxide and solvent-based strip methods. Tool-level performance data confirms comparability with common process chemistries, complete resist removal, and throughput on par with legacy methods.

The maturity of this process approach marks a departure from previous “green tech” proposals that failed to meet manufacturability thresholds. At a time when fabs face mounting pressure from hyperscaler customers, EU carbon regulation, and Scope 3 accounting mandates, this process uniquely aligns technical performance with immediate sustainability impact. Its adoption represents a meaningful step forward in closing the longstanding gap between sustainability goals and operational realities.

The paper will first substantiate its environmental advantages through modeled CO_2e comparisons per wafer, based on documented chemical usage rates for conventional and ozone-based strip processes. It will then confirm the technical soundness of the method—grounding its effectiveness in known reaction pathways and supporting it with fab-level data on resist removal, compatibility, and defectivity. Together, these findings show that the process can be deployed now—without tradeoffs—to meet rising green manufacturing demands.

Biography
Phillip Sundin
Business Development Manager at SHELLBACK Semiconductor Technology

Phillip Sundin is a seasoned professional in the semiconductor equipment industry with over 3-decades of experience with wet-processing equipment. He is currently serving as the Business Development Manager at

SHELLBACK Semiconductor Technology. In this role, he plays a pivotal part in driving the company's expansion and customer engagement efforts.

At SHELLBACK, Phillip has been instrumental in the company's global growth initiatives. A notable focus is the increased awareness and adoption of the Torrent Eco-Clean system, which incorporates SHELLBACK's award-winning HydrOzone chemical-replacement technology. This environmentally safe surface preparation system can reduce or eliminate the need for traditional chemicals, aiding clients in achieving their greenhouse gas reduction goals. The Torrent system is particularly significant in supporting the semiconductor industry's projected expansion to a $1 trillion valuation by 2030.

Phillip's expertise lies in identifying and capitalizing on emerging market opportunities within the semiconductor sector, particularly involving wet-processing equipment. His strategic insights, leadership and passion have been critical in positioning SHELLBACK as a key player in the semiconductor equipment industry.

References

A Sustainable Dicing Innovation for Cutting-Edge Semiconductor Challenges

C. Keil
Director Business Development & Sales
Lidrotec Gmbh, Bochum, Germany

Abstract
The production of semiconductor components (chips) is realized on thin wafers and is an energy and resource-intensive process that can take up to 12 weeks. Before the chips can be further processed, they must be separated on the wafer by the so-called dicing - a critical process step that introduces considerable damage to the chip frontside, backside and sidewalls.
The market development of recent years combined with the AI boom leads to a high demand for computing power and data storage, e.g., for training of AI models. In consequence this growing demand leads to a steady increase in energy consumption.
To counteract rising energy consumption, innovative, more efficient product designs, e.g., HBM, are required. These are mostly achieved by a broader use of modern packaging methods, e.g., Advanced Packaging and Hybrid Bonding.
Unfortunately, these modern packaging and bonding methods lead to an increasing demand on chip quality and cleanliness, which cannot be achieved with most of the currently used dicing methods.
As a result, semiconductor manufacturers have to utilize complex multi-step separation processes, including plasma dicing, which are not only expensive but also consume a large amount of chemical process gases.
Our innovative LidroCUT process, based on ultrashort pulse laser in liquid overcomes these challenges. The liquid cools down and binds the emerging nano particles into the liquid, leading to a debris free surface and contamination free sidewalls, enabling hybrid bonding without additional cleaning steps, proven by optical inspection.
Meanwhile, the cooling capacity of the liquid allows for a precise laser power use, leading to high quality, burr free, edges and high break strength.

LidroCUT is literally cutting edge.

Biography
Christian Keil graduated with a Master of Science in Mechanical Engineering from the Ruhr University Bochum in 2017. He gained his first professional experience as a process engineer commissioning machines and training customer employees all over the world. After half a decade as a process engineer he reoriented himself and moved into the sales departments. He joined Lidrotec as Sales Manager in 2023 and is today Director of Business Development & Sales at Lidrotec.

References

High speed oxide reduction and large die capillary underfill wettability improvement by ICP downflow plasma treatment

R. Furukawa
Panasonic Connect Co., Ltd., Circuit Formation Processes Business Division, Osaka, Japan

Abstract

Plasma cleaning technology has been widely used in microelectronics assembly processes. In the case of lead frames and power modules for automotive devices, the oxidation of Cu can easily occur through multiple heat processes, and this Cu oxide is detrimental to molding adhesivity.
This poor moldability often causes delamination issues and the 'popcorn effect' in packages.
Until recently, H_2/Ar mixed gas plasma treatment has been used to remove such oxides in order to eliminate poor moldability issues, but in this case, undesirable cross-contamination of Ag from pad material can occur due to physical ion bombardment effects.
In addition, the oxide removal rate of H_2/Ar plasma treatment with a Reactive Ion Etching (RIE) parallel-plate configuration is quite slow and not uniform on the entire substrate.
In order to realize a high-speed oxide reduction rate and no cross-contamination etching, Panasonic has developed a water vapor plasma treatment with an Inductive Coupled Plasma (ICP) downflow configuration.
More than 100 nm/min oxide reduction rate was achieved, with excellent etching uniformity using this ICP downflow plasma treatment.
In this case, oxide removal is almost completely achieved by OH and H radicals' chemical reaction, so there are no cross-contamination issues.
Plasma cleaning has also been used to improve capillary underfill wettability in flip-chip packaging.
Delamination, crack, and void issues were avoided by utilizing oxygen-based plasma treatments after flip-chip bonding.
However, recently, die sizes for advanced 2.5D/3D packages have increased, which has caused conventional parallel-plate RIE oxygen-based plasma treatment to have insufficient surface modification effect on the chip and substrate surfaces, as the oxygen radicals cannot reach the center part of the large dies.
In this case, also, ICP downflow plasma treatment offers a solution.
ICP plasma has double-digit higher plasma density than conventional parallel-plate RIE plasma systems, enabling high-density oxygen radicals to penetrate into the narrow gap between the chip and the substrate, and offers excellent surface modification effects, even at the center of large 80 mm square dies, for example.
As a result, Panasonic is able to achieve high-speed oxide reduction processes without cross-contamination by water vapor plasma treatment, and large die capillary underfill wettability improvement by oxygen-based plasma treatment, with ICP downflow configuration plasma systems.

Biography

Ryota Furukawa is a staff engineer at Panasonic Connect Co., Ltd, currently in charge of plasma cleaning process development and sample builds.
In 1990, he joined Kyushu Matsushita Electric Co., Ltd as a process engineer. Since then, he has been in charge of R&D activities and product development, and the development of plasma cleaning processes and dry etching processes.
He received a master's degree of radio chemistry from Kyushu University, Japan.

References

Advances in Wafer-Level MEMS Packaging: From Harsh Environment Sensors to Quantum Applications

A. Roshanghias
Head of Research Unit for Heterogeneous Integration Technologies
Silicon Austria Labs GmbH, Heterogeneous Integration Technologies (HIT), Villach, Austria

Abstract
Advanced packaging are key to unlocking the full potential of MEMS sensors, particularly in applications requiring miniaturization, robustness, and extreme environmental tolerance. This talk will focus on recent innovations in wafer-level integration and packaging of MEMS sensors at Silicon Austria Labs, highlighting their critical role in enabling high-performance sensing systems.
We will present two recent success stories that demonstrate the capabilities of advanced wafer-level packaging approaches. The first involves the integration and hermetic packaging of MEMS sensors designed for harsh environments exceeding 250 °C, addressing challenges such as material compatibility, thermal stress, etc. The second case explores the development of a chip-scale quantum sensor achieved through wafer stacking and heterogeneous integration, showcasing the potential of MEMS technologies in emerging quantum applications.

Biography
Dr. Ali Roshanghias is the head of the research unit for heterogeneous integration technologies (HIT) at Silicon Austria Labs (SAL). He received his Ph.D. in materials science and technology in 2012. He pursued his career as a post-doc researcher in Japan and Austria in the fields of electronic materials and advanced microelectronics packaging. In 2015 he joined Silicon Austria Labs (formerly known as CTR Carinthian Tech Research AG). His research interests include heterogeneous integration technologies, interconnect materials, hybrid flexible electronics, and 3D integration

References

Scaling Intelligent Compute Through Topology-Agnostic Fabric IP for Chiplet Integration

J. Aldis
Baya Systems, Chief Hardware Architect, Santa Clara, United States of America

Abstract

As the semiconductor industry embraces advanced packaging to unlock higher integration and performance, it faces growing complexity in designing systems with chiplets and heterogeneous components. The demand for bandwidth, compute density, and energy efficiency, is outpacing what traditional SoC integration can support, particularly for AI and high-performance computing workloads. At the same time, next-generation platforms must deliver consistent performance while reducing time-to-market, thermal impacts of data movement, and the resultant total system cost.

This paper addresses the integration and data movement challenges at the heart of advanced packaging by introducing a new class of chiplet-ready fabric IP optimized for modular architectures. Developed to simplify multi-die system designs, the proposed solution supports both coherent and non-coherent communication under a unified architecture, enabling seamless on-die and die-to-die data movement.

Unlike traditional and resource-intensive custom hardware design techniques, this fabric IP is software-defined, topology-agnostic, correct-by-construction, and highly scalable—accommodating diverse compute needs, memory, and accelerator elements within a single package. It delivers low-latency, high-throughput communication across scalable chiplet topologies, maintaining robust data movement even in complex multi-die configurations using 2.5D and 3D integration. By abstracting interconnect complexity and providing data-driven design capabilities, this approach helps teams ensure performance guarantees early in the design cycle, meeting both functional and thermal goals while accelerating system integration.

The presentation will cover integration strategies, benchmarks demonstrating throughput and latency performance, and implications for heterogeneous packaging and chiplet-based deployment. It will also explore how this approach accelerates advanced packaging adoption through simulation-driven design, software-defined system fabrics, and intelligent chiplet partitioning enabled by data movement optimization.

Biography

Dr. James Aldis has been working in on-die and inter-die networking since the early 2000s, for Texas Instruments, Imagination Technologies, Intel Corporation and others. He has built chips using all the important independent NoC technologies of the last 20 years as well as many proprietary interconnect technologies. Additionally, he has made many contributions to industry ecosystem development in the areas of SystemC-TLM, OCP-IP, AMBA and HSA. James has a PhD in electronic engineering from the University of York and a BSc in pure mathematics from the University of Liverpool.

References

Stitching-Based Resolution Enhancement in Wavefront Phase Measurement of Silicon Wafer Surfaces

M. Jiménez-Gomis
Application Engineer
Wooptix S.L., Application Engineering, San Cristóbal de La Laguna, Spain

Abstract

The increasing demand for higher resolution and faster machinery in silicon wafer inspection is driven by the rapid rise in electronic device production and the continuous miniaturization of microchips. As feature sizes shrink and wafer sizes grow, there is a critical need for precise and efficient surface characterization tools. To address these challenges, this paper presents the design, development, and implementation of a novel measurement device capable of accurately characterizing the surface of silicon wafers through the stitching technique. We propose an advanced optical system architecture specifically optimized for evaluating the surface profile of silicon wafers, with particular emphasis on measuring roughness and nanotopography. The developed device achieves a lateral resolution of 7.56 µm and an axial resolution of 1 nm, enabling high-precision metrology. It is capable of scanning and analyzing an entire 300-mm wafer in approximately 60 minutes, while acquiring and processing approximately 400 million data points. The core methodology utilizes a wavefront phase sensor, which reconstructs the wafer's surface geometry by analyzing two images displaced at carefully determined distances from the conjugate plane within the image space of a 4f optical system. The study further details the comprehensive calibration procedure and introduces a robust algorithm for transforming local measurement coordinates into global wafer coordinates. Quantitative phase imaging is obtained through the application of a wavefront intensity image reconstruction algorithm. Experimental validation demonstrates the system's ability to differentiate between thinned dies bonded onto carrier wafers, detect variations in coplanarity, and identify bonding defects. Additionally, the residual stress in thin films deposited over the dies is quantified using the Stoney model, underscoring the system's potential for comprehensive wafer inspection and advanced process monitoring in semiconductor manufacturing.

Biography

Miguel is Wooptix's application engineer and Phd candidate in the University of La laguna. His research is centered around finding novel use cases for semiconductor metrology technology in close collaboration with industry partners. With a background in consulting and computer science, Miguel bridges the gap between technology development and business use cases.

References

Breakthrough advanced packaging technology - enabling high-resolution copper interconnects by combining patterning & deposition.

S. Muller
Head of Sales & Business Development
Syenta, Eveleigh, Australia

Abstract
The interconnect requirements required by the rapid growth of artificial intelligence (AI) and high-performance computing (HPC) are driving the advanced packaging industry to focus on performance, cost, and sustainability of packaging innovations to meet these looming needs. In parallel, the broad proliferation of chiplet architectures and heterogeneous integration creates additional requirements for flexibility, not just performance.

Syenta's breakthrough technology is a process called localized electrochemical modeling (LEM). LEM combines patterning and electroplating into one process, thus replacing the photoresist application, lithography, and metal plating steps of conventional processes. This simplification reduces infrastructure cost in many ways – equipment acquisition, facility space, energy, staffing, material cost, waste streams – while also reducing the recurring cost with a shorter process time and often a lower layer count and simplified design enabled by finer pitch interconnect.

Biography
The key innovation of LEM is microscale plating, which uses localized electric fields created by a precision stamp acting as a plating electrode. The fine features in the stamp create miniature electrochemical cells that allow for very fine control of the plating process. With this approach, both the linewidth and spacing can be reduced. The seed layer for the plating can also be thinner, which is another factor that decreases geometries and reduces process time and cost.

The stamp consists of a conductive electrode with a dielectric layer on the surface, patterned in the shape of the interconnect to be fabricated. The deposition process consists of the following sequence of steps:
Stamp preparation: After the stamp is fabricated, the material to be deposited is pre-plated onto the stamp's conductive surface, between the dielectric pattern's features. The lower the aspect ratio of the structure to be deposited, the more depositions can be completed before this step must be redone.
Ink delivery: Electrolyte is added to the conductive substrate, to act as a transfer medium.
Stamp alignment and positioning: The stamp electrode is aligned to optical fiducials on the substrate, and then lowered into position, until it is contact with or close proximity to the substrate.
Deposition: Once in position, an electrical potential is applied to the stamp and the substrate to electrochemically move material from the stamp to the substrate. The dielectric pattern forms the walls of nearly enclosed electrochemical cells, restricting the spatial pattern of deposition to only below the exposed stamp electrode.
Removal and washing: After deposition, the stamp is raised up from the substrate, and the excess ink is washed away.
Etching: Any remaining thin metal deposition outside the target area is removed with a wet etch.
Ultimately, there are three main features of the process enabling the leading-edge capabilities of LEM:
Electrochemical deposition vs. other deposition => high material quality
Localised [JG1] electric fields vs. bulk area process => precise, high-speed deposition
Stamp electrodes vs. masks and lithography => large area, high-resolution patterning

Interconnect Capabilities Pushing the Roadmaps
Fine feature size is the primary metric for any interconnect technology. Syenta has demonstrated 4 mm lines in a lab version of the process, which was limited only by the electrode fabrication process, and expects to reach 1µm in the next demonstration
LEM is able to achieve **high material quality** while depositing at high speed due to the localised electric

field. Measured conductivity of copper and silver deposited by LEM is 80-90% of the bulk metal without any post-processing. This material quality is comparable to established metallisation processes, including thermal evaporation and PECVD. A high-quality surface is also a feature of LEM. With the localised electrochemical process, a surface roughness below 4nm is possible with copper structures. This is a critical capability since bonding to microbumps can be a strong function of the material roughness. LEM has the capability for ultra-smooth surfaces or features tailored to a particular bonding process.

Manufacturing Advantages

An important advantage of Syenta's LEM process is that several manufacturing advantages come in conjunction with the leading-edge process. A trade-off of performance and manufacturability – and therefore cost – is unnecessary. Some of these advantages are:

Simplified fabrication: The traditional method for fabricating RDL or any patterned layers is the dual damascene process. This consists of 18 major steps, 14 of which are associated with photolithography, which is the rate limiting and most expensive step in the process. LEM combines the deposition and patterning of metal layers into a single process, eliminating all steps associated with photolithography. This reduces the total number of steps by 60%, with the remaining steps all being high speed and low cost. Figure 3 illustrates recurring cost benefits of LEM vs. dual damascene and a conventional semi-additive process.

High-speed fabrication: LEM has a unique combination of high throughput while delivering high resolution features. The deposition time for a structure deposited with LEM is simply the structure height divided by the vertical deposition speed. LEM has demonstrated vertical deposition speeds above 100 nm/s, and total deposition times can be measured in only seconds. Independent of the processing speed, LEM is a technology compatible with large area, even panel-level processing. Ultra-short deposition time combined with large area parallel processing results in an unparalleled throughput for the semiconductor industry, and exceptional capital productivity. Together, these scalability benefits result in a method that has the potential to be 100x faster and more capital efficient than the status quo of photolithography-based fabrication of advanced packaging.

Energy efficiency: By eliminating many inefficient steps, LEM technology enables a >90% reduction in energy use than traditional processes. Subtractive processes like photolithography require many material processing steps per layer, each of which can be extremely energy intensive, and as a subtractive method, waste a huge amount of material. Manufacturing 1 kg of microelectronics with photolithography consumes between 300 and 30000 kWh, and energy consumption can be 5-20% of a fab's total operating budget. In comparison, LEM can use as little as 10 kWh/kg, close to that of fabricating bulk copper from raw precursors. LEM saves further energy by avoiding high vacuum and high temperature processes. LEM is also a reversible process: unused electrolyte can be recycled, reducing waste to an absolute minimum.

References

High Throughput Digital Lithography Development for 3D Device Integration

K. Varga
EV Group, Business Development, St. Florian am Inn, Austria

Abstract
The development of high throughput maskless exposure technology for 2.5D and 3D integration has been a subject of considerable R&D efforts in recent years. The newly development system, with a proven technology for UHD FO WLP, was utilized for the digital lithography patterning of redistribution layer (RDL) and VIA structures for application in Fan–out panel level packaging (FO PLP). This strategic shift from WLP to PLP is motivated by the objective to maximize the efficiency of the multi-die packages and to optimize the cost of ownership (CoO). The digital lithography patterns were applied to a substrate dimensions, 300×300 mm², glass and silicon respectively, by using high resolution PI dielectric material. The spray coating process was applied for the square substrates using ultrasound spray nozzles technology to ensure the homogenous distribution of the dielectric materials resulting in ±8.3 % non-uniformity. The relative Critical Dimensions Uniformity, evaluated as Michelson contrast yielded ±1.83 % and stayed below 150 nm in all but two locations on the panel–edge. The SEM cross–session images revealed <5 µm, qualifying the process for the high-density advanced packaging applications. The utilization of advanced software constitutes a pivotal element in the operation of the Zero Stitch feature and the dynamic "on–the–fly" compensation that is imperative in heterogeneous integration processes. Despite this challenge the exposure did not indicate any visible alterations from the intended profile. To prove the image and resist performance the 'Siemens Stars' were applied during the processing challenging the exposure process literally in all directions. The central resolution breakdown circle at the 2 µm-L/S level shows that the L/S-ratio becomes biased towards the intrinsic resist behavior. The straight side wall profiles of the Siemens Starts proved the homogenous patterning in all arbitrary directions. Innovative processes overcome the limitations of legacy exposure technology, especially for large die sizes interposer patterning, as required for current, and future AI and HPC devices.

Biography
Dr. Ksenija Varga is the business development manager at EV Group, where she is responsible for the new applications development of the lithography technologies. In her role, Ksenija is responsible for the new product launches and global product positioning. Additionally, Ksenija is involved in strategic technology roadmaps focusing on the next generation EVG’s lithography equipment development.
Ksenija holds a doctorate degree in chemistry from the University of Innsbruck in Austria. Prior to joining EV Group, Ksenija accumulated professional experience in the chemical industry, holding a variety of roles. The roles encompassed R&D, innovation project leadership, business development and global key account management.

References

First open Fan-Out Wafer Level Package (FOWLP) Manufacturing in Europe

D. Lieske
Senior Expert Advanced packaging
AEMtec GmbH, Advanced Packaing, Berlin,
Germany

Abstract
A high number of companies are developing products in the field of microelectronics and seek for an industrial volume production partner for advanced packaging technologies (e.g. FI-/FOWLP, WLP, CSP, SiP), these are relatively new compared to classic wire-bonded dies on organic substrates. Some reasons for introducing new advanced packaging options are obvious and performance driven. There is typically the need for a rising number of interconnects per area, smaller package size without losing interconnects, faster signal speed equivalent to higher frequencies and thermal aspects in order to facilitate high density integration. AEMtec Berlin is focusing on filling this gap by offering FOWLP technology to the market. The traditional Fan-Out package features embedded dies with a thin-film Cu Redistribution Layer (RDL) for signal routing in a substrate-less package, making an organic Flip-Chip substrate obsolete. Lines and Spaces of RDL can be as small as 5µm and therefore the number of layers, that are needed to route interconnects from IC-chip to a solder ball is reduced.
First Fan-Out packages have been built and electrically tested from DC to 16 GHz at AEMtec. It could be proven, that the performance is superior to available products on the market and therefore a first step has been made to offer Fan-Out package development and production to the industry in small and medium volumes now.

Biography
Daniel Lieske is Senior Expert for Advanced Packaging Technologies at AEMtec in Berlin.
He supports product development and process development teams. Daniel advises the sales department on new customer projects and his focus is on new technology developments like Fan Out WLP, RDL, Flip Chip and Photonics packaging to meet the market demand for now and in future.
He holds a diploma in Microelectronics and Microsystems from the Brandenburg University of Technology in Cottbus. Daniel started his career as a Process Engineer for Infineon Technologies Dresden and Qimonda in the Backend for development, production and process transfer to volume sites of Multi-Chip Modules. As a Project Engineer at Freudenberg Mechatronics he developed and improved production equipment for automotive lighting applications.
As a Process Engineer at AEMtec he was responsible over the last 12 years for wafer level solder ball attach, printing technologies, solder reflow and failure analysis.

References

Innovative Materials Addressing Thermal Management in Advanced Packaging

R. Trichur
Global Head of Semiconductor Packaging Market Segment
Henkel Corporation, Irvine, United States of America

Abstract
The rapid adoption of AI applications powered by large language models (LLMs) is driving unprecedented demand for computational performance. This demand is accelerating the adoption of heterogeneous integration — including advanced 2.5D/3D chiplet architectures, high-density fan-out packaging, and co-packaged optics — as a means to extend Moore's Law beyond traditional transistor scaling. At the same time, the growing use of AI at the edge and within mobile devices is placing new performance demands on application processors, prompting the industry to explore novel package architectures and enhanced thermal management solutions to sustain performance within the constrained form factors of mobile platforms.

However, as device performance scales, so does power consumption. Logic, memory, optical components, power-delivery controllers, and other chiplets collectively generate significant heat, resulting in a tight thermal budget for the entire package. Effective thermal management has therefore become critical to maintaining system performance, reliability, and energy efficiency. This creates a unique opportunity for materials innovation: every material in the package stack that interfaces with the die can play a role in reducing hotspots, spreading heat, and efficiently extracting it. In this presentation, we introduce a suite of next-generation materials designed to address these thermal challenges.

* High-thermal-conductivity liquid-molded underfills and encapsulants (>2 W/m·K) with sub-micron fillers for fine-pitch, void-free gap filling and excellent warpage control — ideal for 3D-stacked memory (HBM), TSV bridge dies, and wafer-/panel-level interposer builds with embedded passives and power components.
* Sinterable and high-performance adhesive TIMs for side-by-side mobile application processor packages, and low-impedance phase-change TIMs supporting AI/HPC cloud processor cooling needs.
* High-thermal capillary underfills (1.5 – >2 W/m·K) that protect first-level interconnects and mitigate localized hotspots in AI/HPC devices featuring co-packaged optics.

We will share key innovations and performance data demonstrating how these materials significantly lower thermal impedance, improve heat spreading, and enhance device reliability across a range of heterogeneous integration platforms.

Biography
Ram Trichur is the global head of semiconductor packaging market segment at Henkel. He is responsible for the key strategic and financial objectives for this segment. He has more than 20 years of experience in the microelectronics industry covering both the front-end manufacturing and backend assembly processes. He has 3 patents and has published more than 50 publications and articles in leading conferences and industry magazines. He received his master's degree in Electrical Engineering from University of Cincinnati and completed his executive education in business management from Stanford University's Graduate School of Business.

References

Inkjet Printing for Advanced Semiconductor Manufacturing: A Scalable and Material Saving Solution

D. Volk
Product Manager
SUSS MicroTec SE, Product Management,
Garching bei München, Germany

Abstract
Inkjet printing is gaining traction as a scalable, additive technology for semiconductor manufacturing, particularly in advanced backend processes. It enables precise, digital deposition of functional materials such as photoresists and polyimides—offering a compelling alternative to traditional spin coating and photolithography.
Photoresist deposition via inkjet allows selective coating of complex topographies, including cavities and edges, which are challenging for conventional methods. This approach significantly reduces material consumption and waste, especially for expensive resists, and supports multi-material deposition in a single process step. The ability to print only where needed, with variable thickness, real-time image adjustment, and enhances process control opens new possibilities for device customization. Printing and exposure results from a variety of resists will be presented.

Other key applications that will be presented cover MEMS and power semiconductors, where inkjet-deposited resists support patterning without photolithography. This not only simplifies process flows but also aligns with ESG goals by minimizing chemical usage and energy consumption.
The system architecture supports flexible substrate formats, ranging from wafers to large IC substrates, and integrates advanced motion systems, substrate handling, and ink supply modules.

The SUSS inkjet technology addresses industry demands for additive manufacturing, digital transformation, and sustainability. By enabling selective, high-precision photoresist deposition, it contributes to cost-effective, flexible, and environmentally responsible semiconductor production.

Biography
David studied Printing Technology in Stuttgart and graduated as Ph.D. in 2014 at the Institute of Microsystems Engineering of the University of Freiburg, Germany. He worked in different roles leading application development activities in the field of functional inkjet printing. Since 2022 he is working for SUSS as product manager. His focus is on establishing inkjet printing as manufacturing technology for the semiconductor industry.

References

Sub-THz HR SOI interposer with integrated hybrid thermal TSV and liquid micro-cooling

E. Novoselov
Process Integration Engineer
imec VZW, Leuven, Belgium

Abstract
The increasing demand for miniature, high-frequency devices in millimetre-wave applications such as 6G communications, next-generation radar, and sensing has uncovered inherent limitations in current packaging technologies. RF signal integrity, thermal challenges, and integration of dissimilar materials are among the issues that need to be addressed for enabling scalable and reliable high-performance modules. To solve these challenges, we designed a silicon (Si) interposer platform to enable the heterogeneous integration of an Indium Phosphide (InP) chip with a 94 GHz RF antenna, monolithic microwave integrated circuit (MMIC) structures, and integrated microfluidic cooling.
Our interposer features a multifunctional embedded Cu layer that serves as a ground plane for MMICs, an antenna radiation efficiency reflector, and thermal spreader for enhanced thermal dissipation. In addition, the interposer features dense arrays of 20 × 100 µm Cu TSVs with vertical RF signal routing and low resistance, as well as efficient thermal conduction from active areas to the backside heat sink. Wafer level oxide-oxide fusion bonding was used to integrate top RF part with bottom microfluidic cooling part.
InP chip is bonded with Cu/Ni/Sn micro-bumps, offering high-density low-resistive electrical interconnects and structurally reliable bonding. A mechanical test vehicle has been implemented to test bump quality, alignment precision, and structural strength, with inspection results to be presented.
To further improve high-frequency signal routing, the interposer also features coplanar waveguide (CPW) traces optimized for low insertion loss at 94 GHz. Further, monolithically integrated microfluidic channels in the Si substrate enable active, localized cooling right below high-power components, further enhancing system thermal performance under load.
We present RF measurements like S-parameters of CPW structures and antenna structures with effective transmission and impedance matching at 94 GHz. Thermal testing confirms the efficiency of combined microfluidic and Cu-based thermal management.

Biography
Evgenii Novoselov was born in Saint Petersburg, Russia, in 1988. He received his B.Sc. in Photonics and M.Sc. in Optoinformatics (summa cum laude) from ITMO University in 2009 and 2011, respectively. In 2017, he earned his Ph.D. from Chalmers University of Technology, Gothenburg, Sweden, with a dissertation on MgB2 hot-electron bolometer mixers for sub-mm wave astronomy.
After completing his Ph.D., Evgenii joined the Microwave Electronics Laboratory at Chalmers as a postdoctoral researcher, where he worked on W-band graphene FET-based resistive mixers. Since 2019, he has been with imec in Leuven, Belgium, where he currently holds the position of Senior Process Integration Engineer. His work focuses on heterogeneous component integration, including BEOL, MEMS, RF systems, and hyperspectral imaging technologies.

References

Enhancing Low-Temperature Hybrid Bonding through Copper Microstructure Engineering

J. Stubbe
Global Application Manager
MKS, Atotech Deutschland GmbH & Co. KG,
Berlin, Germany

Abstract
The increasing need for advanced high-density interconnect packaging technologies underscores the demand for reliable hybrid bonding solutions. Traditional copper-to-copper bonding techniques based on coarse-grained copper (cg-Cu) typically require temperatures exceeding 300 °C, which can be detrimental to device performance and integration due to the risk of IC damage. To mitigate these risks, both industry and academia are exploring alternative materials and processes, such as nanotwinned copper (nt-Cu) and metastable fine-grained copper (fg-Cu). While nt-Cu enhances atomic diffusivity and enables bonding at reduced temperatures, it shows limitations in terms of via filling capability. In contrast, optimized fine-grain copper deposits have the ability to recrystallize, enabling high copper diffusivity during annealing. This generally allows more reliable bonding results by improving the Cu-to-Cu bond interface. However, stabilization of the fine-grain crystal structure during wafer holding times remains challenging.

In this work, we demonstrate a promising pathway for enabling low-temperature hybrid bonding through fg-Cu deposition by a next-generation ECD copper electrolyte. Its deposits maintain their structural stability during queue times and can promote recrystallization upon thermal annealing. Moreover, via filling capability of the electrolyte allows to process typical W2W and D2W substrates.
Methods for microstructural characterization were employed to investigate differences in fine grain stability and related impacting parameters. Based on optimized additives, metastable fine-grain copper deposits remain stable for more than four weeks under ambient conditions. The findings support the viability of fine-grain copper as a key enabler for next-generation, low-temperature hybrid bonding, aligning with the integration needs of cutting-edge 3D-stacked devices.

Biography
Dr. Jessica Stubbe is Global Application Manager in Semiconductor at MKS' Atotech in Berlin, where she leads the application team for electrochemical deposition in advanced packaging. She holds a PhD in coordination chemistry with a focus on electrochemistry and has developed a strong expertise in linking fundamental material behavior with process performance. Over the past years, she has focused on the development and optimization of plating processes for semiconductor applications, supporting global customer projects and bridging R&D with high-volume manufacturing. Her role combines technical expertise, customer collaboration, and strategic project leadership.

References

Driving Heterogeneous Integration for AI and Beyond

H. Oetzlinger
Vice President and Head of the Panel Product line
Lam Research, Salzburg, Austria

Abstract
The semiconductor industry is undergoing a transformative shift, with advanced packaging emerging as a critical enabler of performance, scalability, and cost-efficiency in the post-Moore era. Heterogeneous integration (HI), which combines diverse chiplets with varying process nodes and functionalities into a single package, addresses technical challenges such as shrinking transistor sizes, increasing interconnect density, and optimizing power efficiency. The surge in demand for artificial intelligence (AI) applications, particularly high-performance computing (HPC) and data center AI chips, has further accelerated the need for innovative packaging solutions like 2.5D/3D ICs, fan-out wafer-level packaging (FOWLP), and panel-level packaging (PLP). These technologies enable higher bandwidth, lower latency, and compact form factors essential for AI-driven workloads. Recent product developments, including chiplet-based architectures and high-bandwidth memory (HBM) integration, underscore the industry's focus on powering next-generation AI systems.

This presentation explores the technical imperatives and market dynamics driving advanced packaging, with a deep dive into panel-level packaging (PLP). PLP offers significant cost advantages by processing multiple packages simultaneously on larger panels, enhancing economies of scale compared to traditional wafer-level packaging. However, both the substrate and PLP markets face challenges, notably the lack of standardized panel sizes, which complicates equipment design and increases costs. PLP's economic viability is further constrained by its suitability primarily for high-volume devices, limiting its total market size. Despite these hurdles, the convergence of technology and equipment requirements between substrate and PLP markets is fostering a more robust equipment supplier ecosystem, potentially unlocking greater scalability and innovation.

The presentation will also highlight Lam Research's cutting-edge solutions for advanced packaging, focusing on its advancements in chiplet-to-chiplet and chiplet-to-substrate heterogeneous integration. By addressing warpage, electroplating uniformity, and other manufacturing challenges, Lam Research is enabling scalable, high-performance packaging solutions tailored for AI, 5G, automotive, and consumer electronics applications. This convergence of market needs and technological innovation positions advanced packaging as a cornerstone of the semiconductor industry's future.

Biography
Herbert Oetzlinger graduated from HTL Braunau in 1987 with a specialization in high-power electronics and electrotechnics. With over 30 years of experience in the semiconductor industry, he has built deep expertise in wet processing, particularly in advanced packaging technologies involving electroplating, wet etching, and wafer/substrate cleaning.

Herbert held the role of Vice President of Business Development at Semitool Inc., where he was recognized for his deep process and hardware knowledge. During his tenure, he collaborated with leading global companies on innovations such as Fan-Out, Embedded Wafer-Level Ball Grid Array (E-WLB), and other cutting-edge developments in wafer-level advanced packaging.

In 2012, he founded Semsysco GmbH and served as its CEO. Under his leadership, Semsysco became a global leader in high-speed electrochemical deposition, known for its comprehensive capabilities in wet processing for both wafer and panel-level applications.

Following Lam Research's acquisition of Semsysco in 2022, Herbert joined Lam as Vice President and Head of the Panel Product Line, where he continues to drive innovation in advanced packaging solutions.

References

Beyond Moore's Law: How Advanced Packaging and Silicon Photonics Extend Scalability

H. Kamineni
Director, Advanced Packaging
GLOBALFOUNDRIES, Advanced Packaging,
Central R&D, Malta, United States of America

Abstract
As traditional transistor scaling approaches its physical and economic limits, the semiconductor industry is increasingly turning to advanced packaging and silicon photonics to sustain performance growth and system scalability—ushering in a new era beyond Moore's Law. This presentation will explore how heterogeneous integration (HI) and silicon photonics are redefining compute and interconnect paradigms. We will examine the role of high-density photonic packaging in enabling energy-efficient, high-bandwidth data transfer, and discuss innovations such as passive V-groove fiber attach and detachable fiber couplers that address the challenges of optical I/O scaling for artificial intelligence (AI) and data center applications. This talk will also highlight the emergence of foundry solutions like GF Fotonix™, which combine advanced modulators, photodiodes, and SiN waveguides to deliver scalable, high-performance optical systems. The session will highlight the critical role that packaging and test will play in the adoption and scaling of silicon photonics. By bridging the gap between photonics and electronics, these technologies not only extend the trajectory of Moore's Law but also lay the foundation for next-generation computing architectures.

Biography
Dr. Himani Suhag Kamineni is currently the Director of Advanced Packaging and a Distinguished Member of Technical Staff (DMTS) at GLOBALFOUNDRIES. She holds a Ph.D. in Nanoscale Science from CNSE (Albany, NY). After graduation, she joined GLOBALFOUNDIRES where she held several roles in the Packaging organization. She then joined PSIQUANTUM, a silicon-photonics based quantum computing start-up, to drive the advanced packaging efforts to build a scalable photonic quantum computer. She rejoined GLOBALFOUNDRIES in 2023 where she served a one-year leadership assignment as the Chief of Staff to the CTO. She now leads a diverse team of engineers who drive the advanced packaging R&D efforts that support all product lines.

References

Heterogeneous Integration and Photonic Packaging of a PIC-Based Sensing Platform for Environmental Applications

A. Sundararajan
Project Leader - Photonics Packaging
PHIX Photonics Assembly, Enschede, The Netherlands

Abstract
As part of the EU-funded COMPAS program, PHIX is leading the efforts in advanced photonic packaging and heterogeneous integration for the development of a compact, low-cost, and ultrasensitive PIC-based sensing platform for air and water monitoring. The platform is based on an Aluminium Oxide (Al_2O_3) photonic integration technology, selected for its low-loss waveguiding and wide spectral transparency. It supports interferometric sensing principles integrated with selective layer to enable high-resolution detection of environmental parameters.
A key responsibility of PHIX is the assembly and integration of PCSELs (Photonic Crystal Surface Emitting Lasers) fabricated within the project onto the Al_2O_3-based PIC using high-precision flip-chip bonding and scalable packaging techniques. This presentation will focus on the packaging architecture, optical and electrical interfacing strategies, and the challenges of aligning and integrating active components with the interferometric PIC platform, highlighting how PHIX's assembly technologies enable the realization of a robust, miniaturized, and field-deployable sensing solution.

Biography
Anneirudh Sundararajan is a Project Leader at **PHIX Photonics Assembly**, where he leads several **EU-funded initiatives** as well as **customer-driven projects**. He specializes in **flip-chip bonding technology** and the **advanced packaging of photonic integrated circuits (PICs)**. Anneirudh **pursued his PhD at the University of Twente**, where his research focused on the **integration of optical components with MEMS-based microfluidic systems**. His work involved the development of **Coriolis mass flow sensors** and **spectroscopic techniques** for **multiparameter fluid characterization**. Prior to joining PHIX and pursuing his PhD, Anneirudh worked in Germany as a **Process Development Engineer** at a photonic packaging company, gaining hands-on experience in scalable photonic assembly processes. With a strong interdisciplinary background in **optics, microfluidics, and photonic packaging**, he is actively contributing to the development of next-generation photonic sensing platforms.

References

Adhesives for highly efficient optical coupling of Photonic Integrated Circuits

A. Hartwig
Team Leader Business Development Engineering
Delo Industrial Adhesives, Engineering, Windach, Germany

Abstract
The emergence of 5G technology and artificial intelligence (AI) has significantly accelerated the demand for high-speed data communication, leading to the development of advanced packaging solutions such as 2.5D/ 3D packaging for AI applications. Silicon photonics packaging has emerged as a promising alternative to traditional copper-based electronics, offering faster data transmission with lower power consumption.

Yet, the packaging of photonic integrated circuits (PICs) still faces challenges in achieving high performance and reliability. Key hurdles include the need for precise optical coupling with minimal loss, as well as maintaining reliability through reflow processes and environmental stress.

Adhesives are crucial in overcoming these challenges at various stages of the packaging process. Understanding the necessary properties of adhesives - such as bond strength, optical transmission, and resistance to environmental stresses - is critical for successful packaging applications.

This presentation explores active alignment strategies for optical coupling involving the use of adhesives. It discusses methods such as direct butt-coupling of fiber array units (FAUs) to PICs, surface coupling, and employing microlens arrays (MLAs) that allow for more relaxed alignment tolerances. Emphasis is placed on the adhesive requirements needed to ensure efficient coupling.
Experimental data on coupling efficiency, tested under conditions like reflow and 85°C/85% relative humidity, are presented to demonstrate these approaches' robustness. These findings underscore the crucial role of adhesives in enhancing the performance and reliability of advanced photonic systems.

Moreover, a novel approach will be presented, that preserves optical properties following wafer-level processing steps, such as sawing and grinding, by selecting materials with distinctive optical characteristics.

Biography
Dr. Alexander Hartwig, who holds a PhD in Physics, is a seasoned professional in the fields of solid state physics and adhesive technology. He is currently a Teamleader for Business Development Engineering at DELO Industrial Adhesives, where he focuses on developing innovative adhesive solutions for various applications.

With many years of industry experience, Dr. Hartwig combines his deep scientific knowledge with practical engineering skills to support business growth and technological advancements. His expertise makes him a valuable voice at industry conferences and events, where he shares insights on the latest trends and developments in adhesive technology.

References

Some Material-Related Reliability Challenges that go with Package Roadmap Needs

A. Mavinkurve
Director Materials and Labs Package Innovation, CTO
NXP Semiconductors, Nijmegen, The Netherlands

Abstract
As the usage of electronics keeps increasing and taking over or enabling or facilitating many tasks in our daily lives, society is becoming increasingly dependent on the useful life validation and related to that reliability and safety. To accurately predict this, it is of the utmost importance to understand the most relevant failure mechanisms in packaging. This presentation will elaborate on some failure mechanisms in packaging materials and interconnects that become steadily more relevant with the ongoing trend towards miniaturization, heterogenous integration and advanced requirements. On one hand, some examples of extrinsic failure mechanisms will be given, impacting yield, and potentially increasing the risk of high impact customer returns. On the other hand, some wear-out failure mechanisms related to interconnect and material degradation will also be presented, towards approaches to increase robustness and predictability of these degradation mechanisms using metrics that can efficiently be monitored using AI techniques.

Biography
Dr. Amar Mavinkurve leads the Global Materials Team within Package Innovation (Core Technologies) at NXP. He completed his PhD in Polymer Science from the University of Groningen in the Netherlands in 1996. This was followed with a stint at Philips Research working on various topics like polymer-metal interfaces, polymer processing and textiles. He joined NXP Semiconductors in 2004 (at that time still Philips) and has worked mainly on packaging materials and reliability with specific interest in interconnect systems and aging behaviour of packaging materials.

References

From Silicon to Systems: Optimizing Advanced Packaging for High-Performance Integration

C. Zinck
Director of Technical Program Management
ASE Group, Paris, France

Abstract
Advanced packaging is becoming a cornerstone in the progression of semiconductor technology, particularly as the traditional scaling benefits of Moore's Law approach their physical and economic limits. In this presentation, Christophe Zinck will examine recent innovations in advanced packaging architectures that enable higher functional density, heterogeneous integration, and extreme miniaturization — all while maintaining stringent reliability standards.
Using automotive applications as a representative case, he will address the multifaceted challenges associated with thermal management, electrical performance, and long-term reliability in harsh environments. The discussion will also highlight cross-industry collaboration aimed at developing integration strategies that deliver optimal performance, power efficiency, and scalability — extending from the silicon level through to complete system solutions.

Biography
Dr. Christophe Zinck is Director of Technical Program Management at ASE Europe, where he leads technology teams focused on advanced assembly processes for high-performance digital, power, RF, and MEMS & sensor devices.
He began his more than 20-year career in semiconductors in Grenoble, France, holding various roles at CEA-Leti and STMicroelectronics, where he specialized in lithographic process development. He later joined TriQuint Semiconductors in the United States, driving innovation in advanced packaging for RF devices. Upon returning to France, he contributed to Yole Développement and subsequently managed silicon sourcing activities at SOITEC.
Dr. Zinck has co-authored more than 50 publications, holds several U.S. patents, and is a frequent speaker at international industry conferences. He earned his Ph.D. from the Institut National des Sciences Appliquées (INSA) de Lyon.

References

Digital Twin-Enabled Heterogeneous Package Assembly: AI-Driven Yield Optimization Through Early Design and Equipment Modeling

H. Dudek
Siemens EDA, Muenchen, Germany

Abstract
As heterogeneous integration and advanced packaging technologies become crucial enablers for next-generation electronics, manufacturing yield optimization presents unprecedented challenges. This paper introduces an innovative approach that bridges the gap between package design and manufacturing through advanced digital twin modeling of assembly equipment, enabling predictive yield optimization at the design stage which ultimately will decrease time to market by reducing the number of prototypes required. Our methodology implements a comprehensive Assembly Design Kit (ADK) framework that incorporates both physical equipment constraints and process variations.

Biography
Heiko Dudek joined Siemens Digital Industries in 2021, and holds a M.Sc. in Electrical Engineering from University of Applied Science, Munich. He is in EDA for 27 years, holding various positions, including application engineering, R&D, services and technical sales. These days his is looking after solutions around 3D-IC & Heterogeneous Advanced IC Packaging within Europe.

References

The Acceleration of Test Requirements Driven by Advanced Packaging

F. Pizza
Business Segment Manager
Advantest Europe, V93000 Product Unit
Marketing, Vimercate, Italy

Abstract

The growing complexity of systems, enabled by advanced packaging, is driving an unprecedented increase in test requirements.

Key challenges - such as faster signal speeds, higher integration, power demands, thermal dissipation, limited access to critical test nodes, and early detection of failures - are driving new semiconductor test strategies. Trends and directions for the future of test are described.

In particular, the advent of generative AI has significantly **accelerated complexity challenges in test automation.**

To meet the ever-growing demand for computing power in HPC, graphics, gaming, AI, and ADAS applications, the semiconductor industry is rapidly adopting advanced packaging solutions at scale. This trend enables new approaches, such as **multi-vendor and multi-chip integration** for large SoCs.

Testing across all stages of the manufacturing process is now a **critical enabler of both quality and cost efficiency**.

At the **wafer level**, Automated Test Equipment (ATE) must provide system-level test coverage to prevent the costly packaging of defective silicon.

At the **package level**, ATE faces increasing challenges, including managing large volumes of test data through limited access ports while also controlling power and thermal conditions.

Innovative test strategies and technologies are required to address these demands, particularly those that manage thermal issues throughout the entire test flow. Effective **thermal control solutions**, from wafer to singulated die and from package to system-level test, are becoming essential for efficiently testing advanced 2.5D and 3D package assemblies.

As a result, the role of the **ATE-based test cell** is evolving—from pure defect detection to **complex system-level validation** and **optimized yield ramps** for each new technology node and integration approach.

Biography

Fabio Pizza is a Business Segment Manager at Advantest Europe, within the V93000 Product Unit Marketing organization. Based in the Advantest Italy office, he is responsible for developing and executing strategies to protect and grow the V93000 market share in the Performance Digital segment — including HPC/AI, Mobile/Automotive Application Processors, and ADAS.

In his role, Fabio drives the definition of competitive solutions and product roadmaps aligned with customer requirements for performance, cost of test, and innovation.

He holds a Master’s degree in Electronics Engineering from Politecnico di Milano (Italy) and brings over 20 years of experience in the semiconductor industry.

References

High-End Dose Management: X-ray Inspection protecting Next-Generation Advanced Packaging

D. Stickler
Director X-Ray Technology & Components
Comet AG, X-ray System Division, R&D X-Ray Technology & Components, Hamburg, Germany

Abstract
As semiconductor devices grow smaller, denser, and more complex, advanced packaging demands inspection solutions that deliver both clarity and care. Traditional X-ray approaches often struggle to balance image quality with sample integrity — a challenge magnified in fragile next-generation packages. Comet Yxlon is changing the game by pioneering real-world dose management studies and introducing next-generation inspection technologies that minimize radiation exposure without compromising resolution. This presentation will explore how advanced dose optimization not only safeguards sensitive components but also unlocks new levels of reliability, speed, and insight for semiconductor manufacturers. By adding intelligent dose control to X-ray inspection, Comet Yxlon is helping the industry move faster, with greater confidence, into the era of heterogeneous integration and 3D architectures.

Biography
Dr. Daniel Stickler is Director X-ray Technology & Components at Comet AG, X-Ray System Division. Based in Hamburg, Germany, he holds a PhD in Physics from the University of Hamburg and has extensive experience in X-ray imaging, semiconductor X-ray applications and product innovations.

References

X-ray CT scanning inspection for advanced semiconductor packaging

T. Kumazawa
General Manager
Techno Horizon Co., LTD, Robotics Innovation Sales, Nagoya, Japan

Abstract

In cutting-edge semiconductor packaging, X-ray CT scanning inspection is recognized as an effective method for ensuring the quality of bumps and substrates. However, with the trend toward larger chips and smaller bumps, there is a growing demand for even faster inspection speeds.
Furthermore, there is a trend shifting from substrate materials made of silicon to those made of glass. To establish new processing technologies and ensure quality, high-speed X-ray CT scanning inspection is required.
Techno Horizon is addressing these new demands in X-ray CT scanning inspection for cutting-edge semiconductor packaging by applying AI technology to reduce imaging time, enhance automated inspection programs, accommodate larger object sizes, and adopt vacuum suction mechanisms.
Furthermore, we are developing a new CT scanning method to enable 100% inline inspection.
We will provide details for the conference.

Biography

Takashi Kumazawa has over 25 years of experience in the industrial and medical imaging industries, as well as more than 20 years of experience in international business. He is currently **General Manager of the Robotics Innovation Business Unit at Techno Horizon Co., Ltd.**, leading global initiatives in semiconductor X-ray inspection, PCB AOI, machine vision, optics, and soldering systems. With extensive experience in sales & marketing, R&D, and manufacturing, he combines strong leadership and technical expertise to drive innovation and business growth.

References

High-Resolution Inspection of Hybrid Bonds, Microbumps, and TSVs - Are X-ray Methods Ready for the challenges of Advanced Packaging?

B. Hansson
Excillum AB, Kista, Sweden

Abstract
The push for higher performance, lower power consumption and smaller form factors combined with lower cost per function is driving the shift from 2D scaling to heterogeneous integration and advanced packaging methodologies. As advanced packaging grows in complexity, ensuring the yield and reliability of the intricate interconnects becomes increasingly challenging, necessitating the requirement for improved high-precision inspection methods from off-line failure analysis to at- and in-line inspection. X-ray nano-computed tomography (nano-CT) and X-ray laminography addresses this challenge by offering 3D X-ray imaging with sub-micron resolution, enabling precise visualization of critical internal features.

While traditional X-ray imaging has been limited by resolution and throughput constraints, recent breakthroughs in nano-focus X-ray sources now enable true sub-micron 3D inspection at improved measurement times. X-ray imaging techniques must however always balance resolution, speed and if any sample preparation can be performed. To illustrate these enhancements this communication present case studies from two different cutting edge devices.

First a comprehensive 3D X-ray imaging evaluation of an HBM memory stack connected by ~20 µm microbumps was performed. Using nano-CT, we demonstrate that a 30-second scan provides sufficient resolution for initial structural assessment—from redistribution layers (RDLs) and vias in the substrate and interposer to the intricate micro-bumps within the stack. By increasing scan time, more detailed features—such as voids and internal defects—can be revealed. For non-destructive inspection of full-sized packages, X-ray laminography offers significant advantages. Here we demonstrate laminography scans of the HBM microbumps acquired in just a few minutes and discuss the benefits and trade-offs of longer exposure times on image quality and resolution.
Second, in addition to HBM microbumps, we present measurements from an AMD Ryzen 7 5800X3D processor, featuring hybrid copper bonding with 1.5 µm vias at 9 µm pitch. Here, individual bond pads are clearly resolved, enabling analysis of planarity information that typically has seemed to difficult for 3D X-ray imaging.

Together, these results highlight that X-ray nano-CT and laminography are now practical, high-value tools for R&D, failure analysis, and yield ramp-up in advanced packaging.

Biography
Björn Hansson has been working with advanced X-ray sources at Excillum AB since 2011, serving as Director of Sales and Marketing, CEO and now CTO. Prior to Excillum AB, Björn was involved in early development of laser plasma sources for EUV lithography at the Royal Institute of Technology in Stockholm, as a Co-Founder of Innolite AB and finally as a Senior Scientist at Cymer, Inc. (now ASML). He holds a Ph.D. in applied physics from KTH Royal Institute of Technology, Stockholm.

References

C. Scanlan
Senior Vice President Technology
Besi, Steinhausen, Switzerland

Biography
Moderator

References