Advanced Packaging Conference

Welcome Remarks

L. Altimime
President
SEMI Europe, Berlin, Germany

Abstract
Welcome Remarks

Biography
Laith Altimime, as President of SEMI Europe, leads SEMI's activities in Europe and the Middle East and Africa (EMEA). Altimime has P&L responsibility as well as ownership of all Europe region programs and events, including SEMICON Europa. He is responsible for establishing industry standards, advocacy, community development, expositions, and programs. He provides support and services to SEMI members worldwide that have supply chain interests in Europe. He manages and nurtures relationships with SEMI members in the region and globally as well as with local associations and constituents in industry, government, and academia. Altimime has more than 30 years of international experience in the semiconductor industry. Prior to joining SEMI in 2015, He held senior leadership positions at NEC, KLA-Tencor, Infineon, Qimonda, and imec. Altimime holds an MSc from Heriot-Watt University, Scotland.

References

The APECS pilot line is powering the evolution of chiplet technologies

R. Aschenbrenner
Director Deputy
Fraunhofer IZM, Berlin, Germany

Abstract
The pilot line for »Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems« (or APECS in brief) is a key part of the EU Chips Act, as it will propel innovation in chiplet technology and enrich the semiconductor research and production capacities in Europe. The institutes cooperating in the Research Fab Microelectronics Germany (FMD) are working closely with other European partners to complete the APECS line and contribute substantially to making Europe more technologically resilient and competitive in the global semiconductor industry. The pilot line will give large industry players and SMEs or smaller start-ups easier access to cutting-edge technology and feed into more reliable and resilient semiconductor value chains.
The presentation will discuss the role of Fraunhofer IZM in the APECS pilot line with its expertise for the hardware integration of chiplet systems. With its access to individual chiplet components, the institute can cover the entire process flow needed to create fully functioning systems. Its researchers are working on modern 300mm interposer technologies, high-density substrates, advanced assembly technologies, and the necessary processes for the advanced heterointegration of highly integrated systems. Fraunhofer IZM is establishing itself as a key partner for system-level heterointegration in Europe with several focus innovations.

Biography
Rolf Aschenbrenner received the B.S. degree in mechanical engineering from the University for Applied Science, Gießen, Germany in 1986 and the M.S. degree in physics from The University of Gießen, Germany, in 1991. Since March 1994 he has been employed at the Fraunhofer Institute for Reliability and Microintegration (IZM), where he is presently the deputy director and head of the Business Development Team.

References

Leveraging Virtual Twins and AI/ML in semiconductor industry using 3DEXPERIENCE platform

S. Joshi
Senior Manager Technical Solution -
Semiconductor Industry
Dassault Systèmes, High Tech, Velizy, France

Abstract

Semiconductor companies optimize every stage of their operations—from research and chip design to production and supply chain—by leveraging a combination of multi-scale virtual twins and artificial intelligence. It helps reducing, downtime, enhance scalability, and improve resource efficiency, contributing to sustainable design and production practices.In this talk, we will present different virtual twins and AI/ML experiences for semiconductor industry. We will present how it can visualize, model and simulate the entire environment of sophisticated experience on a single platform known as **3D**EXPERIENCE. This platform facilitates sustainable business innovation across the full product lifecycle from materials to process to equipment to fab virtual twins.Virtual twins replicate physical objects just like digital twins do, but they take it further, simulating the processes and interactions within an entire system or ecosystem. This could be a game-changer for the semiconductor industry and beyond, offering a more holistic approach to understanding and solving complex challenges. By incorporating real-world data in real-time, virtual twins can support various stages of semiconductor development, from product introduction to end-of-life, by optimizing and streamlining design, manufacturing, and testing processes. It can also accurately model and predict electrical and thermal behavior, and mechanical performance characteristics of the semiconductor device using simulation virtual twins. These simulations can be used to fine-tune designs for optimal performance. Simulation plays a significant role in the virtual twin, allowing companies to test product designs virtually, avoiding the need for costly prototypes. This accelerates development and ensures higher product performance. Additionally, simulation virtual twins can be used to predict real-world performance and understand failure modes, leading to design improvements over time.Along with creating virtual twins, it is very important to have AI-driven chip design and analysis. AI in chip design involves using artificial intelligence techniques, particularly machine learning, to improve the design, verification, and testing of semiconductor devices.

Biography

Smriti is currently working as a Technical Solution Senior Manager for Semiconductor Industry (High-tech) with Dassault Systèmes. She is responsible for understanding, consolidating and driving semiconductor technical solutions. She develops new solutions and provide enablement worldwide for semiconductor customers. She has over 14 years of R&D experience working with different foundries ST Microelectronics, Altis Semiconductor, X-FAB and research lab like CEA –LETI and Lip6 (U.P.M.C.).She received her **Doctoral (Ph.D) degree** in **Nanoelectronics and Nanotechnolgy** from INP Grenoble (France) in 2013.

References

Glass Core Substrates: Driving Scalability for HVM Through A Versatile Process Control Solution

M. Pau
Strategic Marketing Director for Advanced Packaging
Onto Innovation, Wilmington, United States of America

Abstract
Heterogeneous integration packaging technologies have seen increased adoption driven by the rapidly growing demand for advanced end applications like artificial intelligence (AI) and high-performance computing (HPC). Research and development of glass core substrates are gaining momentum due to their superior mechanical stability and ability to enable the fabrication of high-density metal interconnects and the integration of optical interconnects. However, due to the brittle and rigid nature of glass, their adoption also poses significant manufacturing challenges. Stringent process control is required starting from the bare glass panel and throughout the entire glass core fabrication and buildup process to ensure high manufacturing yield and product reliability.

In this presentation, we will present the integration of a high throughput and multifunctional process control solution starting from the fabrication of through glass vias (TGV) in the glass core. Real-time process control of the laser modification and wet etching process is made possible through the ability to inspect and perform CD measurements across 100% of the panel surface. Besides CD monitoring, we will also demonstrate the ability to detect missing and abnormal TGV as these defects can directly impact the electrical performance of the product. Glass is brittle and prone to cracking or chipping during handling and processing. Microcrack detection before and after metallization is crucial to help detect the mechanical damage early to avoid for downstream yield loss.

With its unique integrated metrology and inspection capability, the same in-line process control solution can also be applied throughout the buildup process. From monitoring the defectivity and CD of the traces post-patterning and metallization, to the 3D measurement of RDL/bump height and panel warpage. This enables for real-time response to variations in material, equipment and process conditions and ensure high productivity and manufacturing yield.

To realize the full benefits of glass as a core material for advanced IC substrate to enable high density interconnects, an advanced inspection and metrology solution is vital. Its multi-functionality and flexibility to handle a wide range of panel sizes up to 650mm x 650mm provides the industry a scalable path to bring glass core substrate from research and development to high volume manufacturing by the end of this decade.

Biography
Monita Pau currently serves as the Strategic Marketing Director for Advanced Packaging at Onto Innovation. With over 15 years of experience, she has held various positions in applications engineering, marketing and strategic business development in both semiconductor capital equipment and electronic materials companies. Her expertise spans across frontend and backend of line process control solutions as well as materials for advanced packaging and assembly. Monita holds a Ph.D. degree in Chemistry from Stanford University.

References

Laser-based Annealing of Nickel Contacts for SiC Devices: Towards Thermally Robust Power Interfaces in 3D Integration

M. Clair
Head of Process Development
3D-Micromac AG, Team Leader Technology and Innovation Management, Chemnitz, Germany

Abstract
Thermal management and electrical integrity are critical bottlenecks in 2.5D/3D packaging, particularly for wide-bandgap semiconductors such as silicon carbide (SiC), which enable next-generation power-dense systems in the automotive and high-performance computing sectors. In this context, Ohmic contact formation (OCF) for SiC must evolve beyond conventional rapid thermal processing (RTP) to meet the demands of thin substrates, reduced thermal budgets, and higher integration density.
This contribution explores a laser-based approach for localized OCF on SiC using diode-pumped solid-state lasers (DPSSL) with UV wavelengths. The study investigates the effect of varying laser fluence, pulse duration, and beam overlap on the formation of nickel silicide (Ni_xSi_y) contacts on 350 µm-thick 4H-SiC wafers with 70 nm NiAl metallization. Qualitative process trends are derived based on structural, electrical, and chemical performance indicators, with an emphasis on suppressing carbon-rich interfacial layers – a key factor in interface reliability under high thermal and electrical loads.
Key findings show that:
(1) Laser-based OCF enables electrically stable contact formation even under high laser fluences, indicating robustness and process tolerance;
(2) laser energy density controls Ni_xSi_y thickness and uniformity in a predictable manner;
(3) Optimized pulse overlap below 30% mitigates the formation of carbon accumulation at the metal/SiC interface.
This laser-driven method represents a promising alternative to RTP, particularly where localized processing and reduced thermal budgets are required. By minimizing global substrate heating and enhancing interface stability, the approach facilitates improved thermal integration compatibility for SiC-based power devices in 2.5D/3D packaging environments.

Biography
Maurice Clair studied Mechanical Engineering at the University of Technology Chemnitz (Germany). He joined 3D-Micromac in 2005 as a development engineer and is now team leader of the technology and innovation management department. In his current role, he serves as the technical lead for ohmic contact formation on SiC (silicon carbide) materials, a critical area in advancing semiconductor technologies.

Through his expertise in laser technologies, he has been instrumental in the development of innovative laser micromachining processes, including: laser trimming techniques for fine-tuning electronic components with both digital and analogue approaches and beam shaping for ultra-short pulsed lasers.

References

Production-Proven Chemical-Free Green Alternative to Solvent and Piranha Wafer Processing using Ozone

P. Sundin
Business Development Manager
Shellback Semiconductor Equipment,
Coopersburg, United States of America

Abstract
Efforts to implement green technologies in semiconductor manufacturing have historically been slow with acceptance, blocked by perceived concerns over performance risk, operational disruption, and cost. Nowhere is this more apparent than in photoresist stripping, where aggressive chemistries like sulfuric-peroxide mixtures and hazardous solvents like NMP and DMSO remain standard, despite their well-documented environmental burdens. This paper presents a comprehensive assessment of a novel process that offers a rare and timely exception: chemical-free resist removal using ozone gas diffused through heated deionized water.

Unlike ozone-dissolved water systems this method operates in a high-temperature, ozone-rich gas environment. The result is rapid, surface-driven chemical deconstruction of the resist polymer, eliminating the need for persistent oxidizers or solvents, while producing minimal downstream contamination. Comparative lifecycle analysis across chemical input, energy use, waste generation, worker exposure, and effluent treatability reveals a substantial reduction in environmental burden—without compromising technical requirements. Measured CO_2e emissions per wafer are reduced by over 70% relative to sulfuric-peroxide and solvent-based strip methods. Tool-level performance data confirms comparability with common process chemistries, complete resist removal, and throughput on par with legacy methods.

The maturity of this process approach marks a departure from previous “green tech” proposals that failed to meet manufacturability thresholds. At a time when fabs face mounting pressure from hyperscaler customers, EU carbon regulation, and Scope 3 accounting mandates, this process uniquely aligns technical performance with immediate sustainability impact. Its adoption represents a meaningful step forward in closing the longstanding gap between sustainability goals and operational realities.

The paper will first substantiate its environmental advantages through modeled CO_2e comparisons per wafer, based on documented chemical usage rates for conventional and ozone-based strip processes. It will then confirm the technical soundness of the method—grounding its effectiveness in known reaction pathways and supporting it with fab-level data on resist removal, compatibility, and defectivity. Together, these findings show that the process can be deployed now—without tradeoffs—to meet rising green manufacturing demands.

Biography
Phillip Sundin
Business Development Manager at SHELLBACK Semiconductor Technology

Phillip Sundin is a seasoned professional in the semiconductor equipment industry with over 3-decades of experience with wet-processing equipment. He is currently serving as the Business Development Manager at

SHELLBACK Semiconductor Technology. In this role, he plays a pivotal part in driving the company's expansion and customer engagement efforts.

At SHELLBACK, Phillip has been instrumental in the company's global growth initiatives. A notable focus is the increased awareness and adoption of the Torrent Eco-Clean system, which incorporates SHELLBACK's award-winning HydrOzone chemical-replacement technology. This environmentally safe surface preparation system can reduce or eliminate the need for traditional chemicals, aiding clients in achieving their greenhouse gas reduction goals. The Torrent system is particularly significant in supporting the semiconductor industry's projected expansion to a $1 trillion valuation by 2030.

Phillip's expertise lies in identifying and capitalizing on emerging market opportunities within the semiconductor sector, particularly involving wet-processing equipment. His strategic insights, leadership and passion have been critical in positioning SHELLBACK as a key player in the semiconductor equipment industry.

References

A Sustainable Dicing Innovation for Cutting-Edge Semiconductor Challenges

C. Keil
Director Business Development & Sales
Lidrotec Gmbh, Bochum, Germany

Abstract
The production of semiconductor components (chips) is realized on thin wafers and is an energy and resource-intensive process that can take up to 12 weeks. Before the chips can be further processed, they must be separated on the wafer by the so-called dicing - a critical process step that introduces considerable damage to the chip frontside, backside and sidewalls.
The market development of recent years combined with the AI boom leads to a high demand for computing power and data storage, e.g., for training of AI models. In consequence this growing demand leads to a steady increase in energy consumption.
To counteract rising energy consumption, innovative, more efficient product designs, e.g., HBM, are required. These are mostly achieved by a broader use of modern packaging methods, e.g., Advanced Packaging and Hybrid Bonding.
Unfortunately, these modern packaging and bonding methods lead to an increasing demand on chip quality and cleanliness, which cannot be achieved with most of the currently used dicing methods.
As a result, semiconductor manufacturers have to utilize complex multi-step separation processes, including plasma dicing, which are not only expensive but also consume a large amount of chemical process gases.
Our innovative LidroCUT process, based on ultrashort pulse laser in liquid overcomes these challenges. The liquid cools down and binds the emerging nano particles into the liquid, leading to a debris free surface and contamination free sidewalls, enabling hybrid bonding without additional cleaning steps, proven by optical inspection.
Meanwhile, the cooling capacity of the liquid allows for a precise laser power use, leading to high quality, burr free, edges and high break strength.

LidroCUT is literally cutting edge.

Biography
Christian Keil graduated with a Master of Science in Mechanical Engineering from the Ruhr University Bochum in 2017. He gained his first professional experience as a process engineer commissioning machines and training customer employees all over the world. After half a decade as a process engineer he reoriented himself and moved into the sales departments. He joined Lidrotec as Sales Manager in 2023 and is today Director of Business Development & Sales at Lidrotec.

References

Sub-THz HR SOI interposer with integrated hybrid thermal TSV and liquid micro-cooling

E. Novoselov
Process Integration Engineer
imec VZW, Leuven, Belgium

Abstract
The increasing demand for miniature, high-frequency devices in millimetre-wave applications such as 6G communications, next-generation radar, and sensing has uncovered inherent limitations in current packaging technologies. RF signal integrity, thermal challenges, and integration of dissimilar materials are among the issues that need to be addressed for enabling scalable and reliable high-performance modules. To solve these challenges, we designed a silicon (Si) interposer platform to enable the heterogeneous integration of an Indium Phosphide (InP) chip with a 94 GHz RF antenna, monolithic microwave integrated circuit (MMIC) structures, and integrated microfluidic cooling.
Our interposer features a multifunctional embedded Cu layer that serves as a ground plane for MMICs, an antenna radiation efficiency reflector, and thermal spreader for enhanced thermal dissipation. In addition, the interposer features dense arrays of 20 × 100 µm Cu TSVs with vertical RF signal routing and low resistance, as well as efficient thermal conduction from active areas to the backside heat sink. Wafer level oxide-oxide fusion bonding was used to integrate top RF part with bottom microfluidic cooling part.
InP chip is bonded with Cu/Ni/Sn micro-bumps, offering high-density low-resistive electrical interconnects and structurally reliable bonding. A mechanical test vehicle has been implemented to test bump quality, alignment precision, and structural strength, with inspection results to be presented.
To further improve high-frequency signal routing, the interposer also features coplanar waveguide (CPW) traces optimized for low insertion loss at 94 GHz. Further, monolithically integrated microfluidic channels in the Si substrate enable active, localized cooling right below high-power components, further enhancing system thermal performance under load.
We present RF measurements like S-parameters of CPW structures and antenna structures with effective transmission and impedance matching at 94 GHz. Thermal testing confirms the efficiency of combined microfluidic and Cu-based thermal management.

Biography
Evgenii Novoselov was born in Saint Petersburg, Russia, in 1988. He received his B.Sc. in Photonics and M.Sc. in Optoinformatics (summa cum laude) from ITMO University in 2009 and 2011, respectively. In 2017, he earned his Ph.D. from Chalmers University of Technology, Gothenburg, Sweden, with a dissertation on MgB2 hot-electron bolometer mixers for sub-mm wave astronomy.
After completing his Ph.D., Evgenii joined the Microwave Electronics Laboratory at Chalmers as a postdoctoral researcher, where he worked on W-band graphene FET-based resistive mixers. Since 2019, he has been with imec in Leuven, Belgium, where he currently holds the position of Senior Process Integration Engineer. His work focuses on heterogeneous component integration, including BEOL, MEMS, RF systems, and hyperspectral imaging technologies.

References

Driving Heterogeneous Integration for AI and Beyond

H. Oetzlinger
Vice President and Head of the Panel Product line
Lam Research, Salzburg, Austria

Abstract
The semiconductor industry is undergoing a transformative shift, with advanced packaging emerging as a critical enabler of performance, scalability, and cost-efficiency in the post-Moore era. Heterogeneous integration (HI), which combines diverse chiplets with varying process nodes and functionalities into a single package, addresses technical challenges such as shrinking transistor sizes, increasing interconnect density, and optimizing power efficiency. The surge in demand for artificial intelligence (AI) applications, particularly high-performance computing (HPC) and data center AI chips, has further accelerated the need for innovative packaging solutions like 2.5D/3D ICs, fan-out wafer-level packaging (FOWLP), and panel-level packaging (PLP). These technologies enable higher bandwidth, lower latency, and compact form factors essential for AI-driven workloads. Recent product developments, including chiplet-based architectures and high-bandwidth memory (HBM) integration, underscore the industry's focus on powering next-generation AI systems.

This presentation explores the technical imperatives and market dynamics driving advanced packaging, with a deep dive into panel-level packaging (PLP). PLP offers significant cost advantages by processing multiple packages simultaneously on larger panels, enhancing economies of scale compared to traditional wafer-level packaging. However, both the substrate and PLP markets face challenges, notably the lack of standardized panel sizes, which complicates equipment design and increases costs. PLP's economic viability is further constrained by its suitability primarily for high-volume devices, limiting its total market size. Despite these hurdles, the convergence of technology and equipment requirements between substrate and PLP markets is fostering a more robust equipment supplier ecosystem, potentially unlocking greater scalability and innovation.

The presentation will also highlight Lam Research's cutting-edge solutions for advanced packaging, focusing on its advancements in chiplet-to-chiplet and chiplet-to-substrate heterogeneous integration. By addressing warpage, electroplating uniformity, and other manufacturing challenges, Lam Research is enabling scalable, high-performance packaging solutions tailored for AI, 5G, automotive, and consumer electronics applications. This convergence of market needs and technological innovation positions advanced packaging as a cornerstone of the semiconductor industry's future.

Biography
Herbert Oetzlinger graduated from HTL Braunau in 1987 with a specialization in high-power electronics and electrotechnics. With over 30 years of experience in the semiconductor industry, he has built deep expertise in wet processing, particularly in advanced packaging technologies involving electroplating, wet etching, and wafer/substrate cleaning.

Herbert held the role of Vice President of Business Development at Semitool Inc., where he was recognized for his deep process and hardware knowledge. During his tenure, he collaborated with leading global companies on innovations such as Fan-Out, Embedded Wafer-Level Ball Grid Array (E-WLB), and other cutting-edge developments in wafer-level advanced packaging.

In 2012, he founded Semsysco GmbH and served as its CEO. Under his leadership, Semsysco became a global leader in high-speed electrochemical deposition, known for its comprehensive capabilities in wet processing for both wafer and panel-level applications.

Following Lam Research's acquisition of Semsysco in 2022, Herbert joined Lam as Vice President and Head of the Panel Product Line, where he continues to drive innovation in advanced packaging solutions.

References

Topic Coming Soon

H. Kamineni
Director, Advanced Packaging
GLOBALFOUNDRIES, Advanced Packaging,
Central R&D, Malta, United States of America

Abstract
Coming Soon

Biography
Coming Soon

References

Adhesives for highly efficient optical coupling of Photonic Integrated Circuits

A. Hartwig
Senior Strategic Business Development Engineer
Delo Industrial Adhesives, Engineering, Windach,
Germany

Abstract
The emergence of 5G technology and artificial intelligence (AI) has significantly accelerated the demand for high-speed data communication, leading to the development of advanced packaging solutions such as 2.5D/ 3D packaging for AI applications. Silicon photonics packaging has emerged as a promising alternative to traditional copper-based electronics, offering faster data transmission with lower power consumption.

Yet, the packaging of photonic integrated circuits (PICs) still faces challenges in achieving high performance and reliability. Key hurdles include the need for precise optical coupling with minimal loss, as well as maintaining reliability through reflow processes and environmental stress.

Adhesives are crucial in overcoming these challenges at various stages of the packaging process. Understanding the necessary properties of adhesives - such as bond strength, optical transmission, and resistance to environmental stresses - is critical for successful packaging applications.

This presentation explores active alignment strategies for optical coupling involving the use of adhesives. It discusses methods such as direct butt-coupling of fiber array units (FAUs) to PICs, surface coupling, and employing microlens arrays (MLAs) that allow for more relaxed alignment tolerances. Emphasis is placed on the adhesive requirements needed to ensure efficient coupling.
Experimental data on coupling efficiency, tested under conditions like reflow and 85°C/85% relative humidity, are presented to demonstrate these approaches' robustness. These findings underscore the crucial role of adhesives in enhancing the performance and reliability of advanced photonic systems.

Moreover, a novel approach will be presented, that preserves optical properties following wafer-level processing steps, such as sawing and grinding, by selecting materials with distinctive optical characteristics.

Biography
Dr. Alexander Hartwig, who holds a PhD in Physics, is a seasoned professional in the fields of solid state physics and adhesive technology. He is currently a Teamleader for Business Development Engineering at DELO Industrial Adhesives, where he focuses on developing innovative adhesive solutions for various applications.

With many years of industry experience, Dr. Hartwig combines his deep scientific knowledge with practical engineering skills to support business growth and technological advancements. His expertise makes him a valuable voice at industry conferences and events, where he shares insights on the latest trends and developments in adhesive technology.

References

Some Material-Related Reliability Challenges that go with Package Roadmap Needs

A. Mavinkurve
Principal Materials & Process Devt Engineer
NXP Semiconductors, Nijmegen, The Netherlands

Abstract
As the usage of electronics keeps increasing and taking over or enabling or facilitating many tasks in our daily lives, society is becoming increasingly dependent on the useful life validation and related to that reliability and safety. To accurately predict this, it is of the utmost importance to understand the most relevant failure mechanisms in packaging. This presentation will elaborate on some failure mechanisms in packaging materials and interconnects that become steadily more relevant with the ongoing trend towards miniaturization, heterogenous integration and advanced requirements. On one hand, some examples of extrinsic failure mechanisms will be given, impacting yield, and potentially increasing the risk of high impact customer returns. On the other hand, some wear-out failure mechanisms related to interconnect and material degradation will also be presented, towards approaches to increase robustness and predictability of these degradation mechanisms using metrics that can efficiently be monitored using AI techniques.

Biography
Dr. Amar Mavinkurve leads the Global Materials Team within Package Innovation (Core Technologies) at NXP. He completed his PhD in Polymer Science from the University of Groningen in the Netherlands in 1996. This was followed with a stint at Philips Research working on various topics like polymer-metal interfaces, polymer processing and textiles. He joined NXP Semiconductors in 2004 (at that time still Philips) and has worked mainly on packaging materials and reliability with specific interest in interconnect systems and aging behaviour of packaging materials.

References

Droplet assisted D2W bonding – introducing fluidics for improved bond front control for low-defect sequential D2W hybrid bonding

T. Schmidt
Product Manager
SUSS MicroTec SE, Product Management,
Garching bei München, Germany

Abstract
Increased control of bond front propagation using DIW droplets dispensed prior to actual die placement could be a powerful approach to reduce the risk of bond voids caused by entrapped air and make thin and also large die handling less complex regarding the bond head design. The technique has the potential to support future D2W bonding with die thicknesses <30µm at improved yield.

Biography
Thomas Schmidt is Product Manager within the Bonder product line of SUSS in Sternenfels. After graduating with a degree in microsystems engineering from the University of Applied Sciences Kaiserslautern, Zweibruecken site, he held various positions within the MEMS/semiconductor industry and also taught at the Baden-Wuerttemberg Cooperative State University (DHBW) in Loerrach and at the Albert-Ludwigs-University in Freiburg on the topics of advanced lithography, microsystems technology and CMOS microelectronics.

Since December 2017, Mr. Schmidt has been a member of the bonder team at SUSS, where he is responsible for the permanent wafer bonding product line with a focus on fully automated production systems that enable both established bonding techniques (for MEMS, packaging, etc.) and newer bonding developments such as D2W and W2W hybrid bonding for advanced packaging.

References

Digital Twin-Enabled Heterogeneous Package Assembly: AI-Driven Yield Optimization Through Early Design and Equipment Modeling

H. Dudek
Siemens EDA, Muenchen, Germany

Abstract
As heterogeneous integration and advanced packaging technologies become crucial enablers for next-generation electronics, manufacturing yield optimization presents unprecedented challenges. This paper introduces an innovative approach that bridges the gap between package design and manufacturing through advanced digital twin modeling of assembly equipment, enabling predictive yield optimization at the design stage which ultimately will decrease time to market by reducing the number of prototypes required. Our methodology implements a comprehensive Assembly Design Kit (ADK) framework that incorporates both physical equipment constraints and process variations.

Biography
Heiko Dudek joined Siemens Digital Industries in 2021, and holds a M.Sc. in Electrical Engineering from University of Applied Science, Munich. He is in EDA for 27 years, holding various positions, including application engineering, R&D, services and technical sales. These days his is looking after solutions around 3D-IC & Heterogeneous Advanced IC Packaging within Europe.

References

The Acceleration of Test Requirements Driven by Advanced Packaging

F. Pizza
Business Segment Manager
Advantest Europe, V93000 Product Unit
Marketing, Vimercate, Italy

Abstract

The growing complexity of systems, enabled by advanced packaging, is driving an unprecedented increase in test requirements.

Key challenges - such as faster signal speeds, higher integration, power demands, thermal dissipation, limited access to critical test nodes, and early detection of failures - are driving new semiconductor test strategies. Trends and directions for the future of test are described.

In particular, the advent of generative AI has significantly **accelerated complexity challenges in test automation.**

To meet the ever-growing demand for computing power in HPC, graphics, gaming, AI, and ADAS applications, the semiconductor industry is rapidly adopting advanced packaging solutions at scale. This trend enables new approaches, such as **multi-vendor and multi-chip integration** for large SoCs.

Testing across all stages of the manufacturing process is now a **critical enabler of both quality and cost efficiency**.

At the **wafer level**, Automated Test Equipment (ATE) must provide system-level test coverage to prevent the costly packaging of defective silicon.

At the **package level**, ATE faces increasing challenges, including managing large volumes of test data through limited access ports while also controlling power and thermal conditions.

Innovative test strategies and technologies are required to address these demands, particularly those that manage thermal issues throughout the entire test flow. Effective **thermal control solutions**, from wafer to singulated die and from package to system-level test, are becoming essential for efficiently testing advanced 2.5D and 3D package assemblies.

As a result, the role of the **ATE-based test cell** is evolving—from pure defect detection to **complex system-level validation** and **optimized yield ramps** for each new technology node and integration approach.

Biography

Fabio Pizza is a Business Segment Manager at Advantest Europe, within the V93000 Product Unit Marketing organization. Based in the Advantest Italy office, he is responsible for developing and executing strategies to protect and grow the V93000 market share in the Performance Digital segment — including HPC/AI, Mobile/Automotive Application Processors, and ADAS.

In his role, Fabio drives the definition of competitive solutions and product roadmaps aligned with customer requirements for performance, cost of test, and innovation.

He holds a Master’s degree in Electronics Engineering from Politecnico di Milano (Italy) and brings over 20 years of experience in the semiconductor industry.

References

High-End Dose Management: X-ray Inspection protecting Next-Generation Advanced Packaging

D. Stickler
Director X-Ray Technology & Components
Comet AG, X-ray System Division, R&D X-Ray Technology & Components, Hamburg, Germany

Abstract
As semiconductor devices grow smaller, denser, and more complex, advanced packaging demands inspection solutions that deliver both clarity and care. Traditional X-ray approaches often struggle to balance image quality with sample integrity — a challenge magnified in fragile next-generation packages. Comet Yxlon is changing the game by pioneering real-world dose management studies and introducing next-generation inspection technologies that minimize radiation exposure without compromising resolution. This presentation will explore how advanced dose optimization not only safeguards sensitive components but also unlocks new levels of reliability, speed, and insight for semiconductor manufacturers. By adding intelligent dose control to X-ray inspection, Comet Yxlon is helping the industry move faster, with greater confidence, into the era of heterogeneous integration and 3D architectures.

Biography
Dr. Daniel Stickler is Director X-ray Technology & Components at Comet AG, X-Ray System Division. Based in Hamburg, Germany, he holds a PhD in Physics from the University of Hamburg and has extensive experience in X-ray imaging, semiconductor X-ray applications and product innovations.

References

High-Resolution Inspection of Hybrid Bonds, Microbumps, and TSVs - Are X-ray Methods Ready for the challenges of Advanced Packaging?

B. Hansson
Excillum AB, Kista, Sweden

Abstract
The push for higher performance, lower power consumption and smaller form factors combined with lower cost per function is driving the shift from 2D scaling to heterogeneous integration and advanced packaging methodologies. As advanced packaging grows in complexity, ensuring the yield and reliability of the intricate interconnects becomes increasingly challenging, necessitating the requirement for improved high-precision inspection methods from off-line failure analysis to at- and in-line inspection. X-ray nano-computed tomography (nano-CT) and X-ray laminography addresses this challenge by offering 3D X-ray imaging with sub-micron resolution, enabling precise visualization of critical internal features.

While traditional X-ray imaging has been limited by resolution and throughput constraints, recent breakthroughs in nano-focus X-ray sources now enable true sub-micron 3D inspection at improved measurement times. X-ray imaging techniques must however always balance resolution, speed and if any sample preparation can be performed. To illustrate these enhancements this communication present case studies from two different cutting edge devices.

First a comprehensive 3D X-ray imaging evaluation of an HBM memory stack connected by ~20 µm microbumps was performed. Using nano-CT, we demonstrate that a 30-second scan provides sufficient resolution for initial structural assessment—from redistribution layers (RDLs) and vias in the substrate and interposer to the intricate micro-bumps within the stack. By increasing scan time, more detailed features—such as voids and internal defects—can be revealed. For non-destructive inspection of full-sized packages, X-ray laminography offers significant advantages. Here we demonstrate laminography scans of the HBM microbumps acquired in just a few minutes and discuss the benefits and trade-offs of longer exposure times on image quality and resolution.
Second, in addition to HBM microbumps, we present measurements from an AMD Ryzen 7 5800X3D processor, featuring hybrid copper bonding with 1.5 µm vias at 9 µm pitch. Here, individual bond pads are clearly resolved, enabling analysis of planarity information that typically has seemed to difficult for 3D X-ray imaging.

Together, these results highlight that X-ray nano-CT and laminography are now practical, high-value tools for R&D, failure analysis, and yield ramp-up in advanced packaging.

Biography
Björn Hansson has been working with advanced X-ray sources at Excillum AB since 2011, serving as Director of Sales and Marketing, CEO and now CTO. Prior to Excillum AB, Björn was involved in early development of laser plasma sources for EUV lithography at the Royal Institute of Technology in Stockholm, as a Co-Founder of Innolite AB and finally as a Senior Scientist at Cymer, Inc. (now ASML). He holds a Ph.D. in applied physics from KTH Royal Institute of Technology, Stockholm.

References