SEMICON Europa

Adaptive Probe Card Cleaning: How AI can add value to Smart Factory Automation

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Body

The cleaning of probe cards needles it's a decisive factor in ensuring the wafers testing is performed with high accuracy and precision. The performance and reliability of semiconductor testing equipment, particularly probe cards, are crucial for maintaining optimal manufacturing yield and product quality. However, as semiconductor technology advances, the demand for higher accuracy and increased testing throughput presents challenges in maintaining probe card cleanliness and performance consistency. Traditional cleaning methods (fixed cycle cleaning method usually set to wafer prober) often lack adaptability and struggle to effectively address evolving contamination sources and patterns.

Enter adaptive probe card cleaning, a revolutionary approach leveraging AI/ML techniques and strategies to tackle these challenges head-on. By integrating real-time monitoring, data analytics, proprietary algorithms, and dynamic adjustment of cleaning parameters without the need for human involvement, adaptive cleaning systems optimize probe card performance in semiconductor testing environments. This proactive maintenance approach not only reduces downtime and enhances testing efficiency but also significantly extends the lifespan of probe cards, minimizing the frequency of costly manual cleaning. The adoption of adaptive probe card cleaning technology, and important component for adaptive control systems required for smart factory automation, translates into substantial savings, ensures consistent performance and longevity of probe cards, and provides valuable data-driven insights, giving a competitive edge (it has been proven with customers throughout Asia and Europe that are seeing cleaning cycle times slashed significantly).

This presentation delves into the principles and benefits of adaptive probe card cleaning, drawing on real customer implementation results to demonstrate cost savings while maintaining testing efficiency and performance in semiconductor manufacturing.

Biography

Mr. Nunzio Renzella, the Technical Pre-Sales Engineer of Innovative Test Solutions for Advantest Field Service at Advantest Italy, holds a Bachelor in Electronics Engineering from La Sapienza University (Rome - Italy).

He was a high school teacher before entering the semiconductor industry where he has worked for 30 years. Nunzio has held various roles encompassing program management, Equipment Engineering, Process Engineering, System/Application Engineering. His experience and technical knowledge in testing have given him the right skills to promote innovation.

References

Reduction of NOx Emission from Waste Gas Treatment

G. Davies
Chief Business Development Officer
DAS Environmental Expert GmbH, Management Board, Dresden, Germany

Body

The reduction of nitrogen oxides (NOx) emissions from waste gas treatment represents a critical environmental objective driven by regulatory requirements and sustainability goals across many industrial sectors.

This contribution discusses the mechanisms of NOx formation, emphasizing thermal and fuel-related pathways during combustion processes, and strategies for NOx reduction. These encompass both primary and secondary measures. Primary measures target the optimization of combustion parameters to minimize the formation of thermal NOx, whereas secondary measures involve advanced technologies such as Selective Catalytic Reduction (SCR) for effective NOx and particulate matter abatement.

In response to the need for effective NOx and particulate matter (PM) abatement, DAS EE has developed a novel stand-alone solution, TSUGA. This innovative product incorporates Selective Catalytic Reduction (SCR) with ammonia for NOx reduction and a membrane filter for particulate matter removal.

SCR-DeNOx technology has emerged as a leading solution due to its capability to convert nitrogen oxides into harmless nitrogen and water vapor through catalytic reaction with ammonia or urea. This technology not only reduces NOx emissions but also addresses particulate matter, making it a versatile tool in emission control strategies. Combustion control strategies are also discussed in detail, highlighting their role in mitigating thermal NOx formation by adjusting combustion conditions.

Ongoing research continues to refine these approaches, aiming for greater efficiency and broader applicability across diverse industrial processes. Ultimately, the implementation of these strategies is crucial for minimizing environmental impact while ensuring compliance with evolving regulatory frameworks worldwide.

Biography

Dr. Guy Davies is Chief Business Development Officer and a member of the Management Board of DAS Environmental Expert GmbH. He joined DAS in 2011 and has since focused on the company's strategies for product development, innovation management and internationalization.

References

Virtual twin experiences for sustainability in semiconductor ecosystem

M. Rei
Semiconductor Industry Solution Experience
Director
Dassault Systèmes, High Tech, Velizy, France

Body

Semiconductor devices are becoming smaller and more complex in design, playing a crucial role in the advancement of various technologies. These devices are essential in every industry, including defense, healthcare, computing, communication, automotive, and energy. The design and simulation of such devices are not only complex but also time-consuming and costly. As we are moving ahead with “More than Moore”, semiconductor manufacturing is getting highly complex. The materials used during the manufacturing process, such as silicon, requires extensive extraction and purification processes. Traditional way of manufacturing and packaging are unsustainable, as it depletes natural resources and amplifies the industry's environmental impact. With latest trend of 3D integration and chiplets, industries are trying to lower such impact. Foundries are exploring different ways of sustainable and energy-efficient production methodologies. The main sources of emissions from semiconductor foundries arise from the energy needed to operate their extensive production facilities. Factories, which account for about 80% of semiconductor manufacturing emissions, significantly influence their greenhouse gas profiles. These emissions primarily come from tooling, which includes hundreds of production tools like lithographic equipment, ion implanters, and high-temperature furnaces. Moreover, cleanrooms that require precise climate and humidity control, along with gas abatement facilities, waste pumps, water chillers, and water purification systems, also contribute substantially to the emissions[1].

In this paper, we would like to present our virtual twin approach, which leads us in finding more sustainable solutions for such issues. Virtual twin can help realizing different techniques to reduce the industry's carbon footprint, minimizing waste, and creating processes that align with green technology principles. We provide different virtual twin experiences from equipment, process to clean room, which helps not only in reaching sustainability goal but also helps in training future task force virtually. In this talk, we will present how virtual twin pave the way towards a better ecosystem, which helps to analysis, and evaluate everything in prior and how our virtual twin solutions fill the gap for design and operations agility and resilience.

[1] (Source: McKinsey & Company)

Biography

Manuel joined Dassault Systèmes in 1986 and has over 35+ years of experience supporting high-tech and automotive global companies, including relocations in South Korea and USA for the deployment of Dassault Systèmes solutions within Samsung Electronics, LG Electronics and IBM hardware divisions.

He leads High Performance Semiconductor Industry Solution Experience, leveraging virtual twins to turn semiconductor complexity into business profitability , and deployed at customers such as NXP, Broadcom, Samsung Electronics, Qualcomm and STMicroelectronics.

References

Nano-analysis of optoelectronic materials in structured semiconductors

V. Bonino
Beamline scientist
ESRF, Grenoble, France

Body

Under the impulse of device miniaturization, the size of the active area of devices have been reduced to the micro and sub-micrometric scale. The synthesis of finely tunable structures with defined properties at the nanoscale level becomes therefore fundamental. In this context, some examples of synchrotron characterization will be given to showcase the capabilities of the nanoprobe beamline ID16B of the European synchrotron - ESRF. Examples will mainly focus on the characterization of the composition and the optical properties and their correlation in GeSn and III/V semiconductors materials.

In infrared emitters based on $Ge_{1-x}Sn_x$ micro-disks with Sn concentrations up to 16.9% no metal segregation was observed by annealing at temperatures as high as 400 °C for 20 min, as it was the case for the reference blanket layer. This study demonstrated how microstructuring offer a solution to the instability of high Sn concentration $Ge_{1-x}Sn_x$ layers [1]. This approach enables the use of thermal annealing processes to improve the properties of this alloy. The origin of the optical emission was investigated in multi-quantum well core/shell nanowires of III-V semiconductors [2]. Two emissions peak at about 2.7 and 3.0 eV were shown to be related respectively to lateral facets and to the interphase with the top facets. Fast recombination rates below 400 ps were observed, revealing possible applications for fast on−off operation in light-emitting diodes (LEDs).

These studies highlight the potential of multimodal characterization of semiconducting materials for next-generation nano-optoelectronics.

[1] V. Bonino, ACS Appl. Mater. Interfaces 2022, 14, 22270−22277
[2] J. Segura-Ruiz , Nano Lett. 2021, 21, 9494−9501

Biography

Valentina Bonino received her Ph.D. from the University of Torino, Italy, on the effect of X-ray radiation on cuprates and oxides. After, she worked as Postdoc in the same project, focusing on the thermal effects induced in the time and the space domains. Currently, she is beamline scientist at the nano-analysis beamline ID16B of the European Synchrotron Radiation Facility. She works in the domain of material science and she is interested in the optical properties of semiconductors having related compositional and/or structural non-homogeneities.

References

Future of Energy-Efficient Compute

G. Gupta
VP Analyst
Gartner, Stamford, United States of America

Body

Current compute paradigms are constrained in power-performance efficiency to support rising AI and generative AI applications, further straining energy requirements. This presentation will discuss upcoming disruptions have the potential to disrupt the future of compute so product leaders must prioritize innovation and change.

Biography

Dr. Gaurav Gupta is a VP Analyst in the Emerging Trends and Technologies team. Dr. Gupta's research areas include semiconductor manufacturing process, chip design trends, AI analytics in chip manufacturing, semiconductor equipment spending, and chip industry economics and supply chain. Dr. Gupta also covers emerging areas, such as autonomous vehicles, Quantum Computing, and future of energy-efficient compute.

Prior to joining Gartner, Dr. Gupta worked as a Knowledge Expert at McKinsey & Co. where he advised clients across the globe in the semiconductor and electronics industry with a focus on business transformation (cost, operations, and growth) and product strategy (launch/development/planning). He has a strong technical background in the semiconductor industry in process, yield, R&D, and integration, having worked at Intel, IBM and GlobalFoundries prior to the stint with McKinsey & Co.

References

Closing the Loop: A Circular Economy for the Semiconductor Industry

M. Moran
Vice President - Aftersales Service Practice
Genpact, Atlanta, United States of America

Body

The semiconductor industry, a cornerstone of modern technology, faces mounting environmental challenges due to its traditional linear model of production, consumption, and disposal. This presentation explores the transformative potential of circular economy principles within the semiconductor sector, focusing on resource recovery, product life extension, and responsible end-of-life management.

Our discussion will encompass three critical areas:

1. Strategic implementation of take-back programs and refurbishment initiatives
2. Navigating the complex transition from linear to circular business models
3. The pivotal role of policy frameworks and industry collaboration in accelerating circularity

Through an examination of real-world use cases, we will highlight how industry leaders are successfully integrating circular principles into their semiconductor operations. These examples will illustrate both the challenges and the tangible benefits of adopting circular practices.

The presentation will conclude with an analysis of key obstacles and opportunities for widespread adoption of circular economy principles across the semiconductor industry. We will explore how this paradigm shift could not only mitigate environmental impact but also drive innovation and create new value streams within the sector.

By addressing these crucial aspects, this talk aims to provide a comprehensive overview of the circular economy's potential to revolutionize the semiconductor industry, offering insights valuable to industry professionals, policymakers, and researchers alike.

Biography

Mark Moran leads the Aftersales Service Practice which is part of Genpact’s Supply Chain Service Line. Mark and team are focused on helping clients better service their customers post product sale by improving processes, leveraging digital for enhanced parts management, increasing efficiency for on-site & remote support resources, and delivering analytic insights to promote continuous improvement. Prior to Mark joining Genpact eight years ago, he ran service operations leading remote & field support, service supply chain, and repair operations at Dell, Avaya, and Jawbone in addition to a few smaller enterprises both publicly and privately held. Mark has a passion for leveraging digital innovations to improve results and reducing effort for teams.

References

Smart Design & Construction for the Semiconductor Industry

T. Kreidel
Director
Jacobs, Electronics, Garching, Germany

Body

Topics covered include:

• The need for increased design and construction velocity leads Owners to lean more heavily on repeatable/reference designs. While there are undoubted advantages to utilization of reference designs, project teams must actively track and adjust for required differences and deviations to the established reference design to accommodate local code/jurisdictional and/or climactic differences.

• Market pressures, including competition for labor and material resources point towards off-site-manufacturing (OSM) as a critical lever for projects in the current environment. OSM changes the dynamic of design and construction projects, driving the need for new skillsets within design and construction teams and altering the timing of critical configuration decisions.

• The use of software platforms can provide invaluable assistance to project teams, in promoting shared real-time visibility to critical datasets. Jacobs has developed one such sophisticated and adaptable project execution framework to ensure broad yet tailored access for project stakeholders real-time project data.

• Recent enhancements in 3D/BIM visualization tools allows broader use of rapid-prototyping approaches to more efficiently explore and select design options.

• Semiconductor manufacturers are striving towards creating digital twins of their facilities, with the goal of creating virtual replicas of physical assets, processes and systems. Currently, the more robust datasets made available with the digital twin construct is being leveraged to increase project velocity, allowing optimization within, for example, procurement, planning and construction sequencing realms. The future for Digital twins promises further exciting possibilities, including true integration with operation and maintenance platforms and opportunities for predictive analytics to enhance facility equipment operation and energy management.

Biography

Coming Soon

References

Post plasma dicing clean in batch spray equipment with adapted sulfuric ozone mixtures

M. Mittermayr
Business Development
siconnex customized solution GmbH, Business Development, Hof bei Salzburg, Austria

Body

Semiconductor manufacturers chase the goal of reduced carbon footprints and running cost, which also applies to the topic of die singulation.

The proposed presentation will show how a new approach to the removal of polymers left behind after plasma dicing was found, how the theory was translated into a hardware concept, how the performance and efficiency of this new process was tested, how the results were analyzed and how it will enable the industry to take another step towards eco-friendlier and more sustainable device manufacturing.

VI. Conclusion

The removal of post plasma dice polymers with our adapted sulfuric ozone mixtures was a full success, beating the current standard of O_2 ashing that our results were pitted against by our client in terms of cleaning efficiency, process time and throughput as underlined by the presented SEM pictures and calculations.

Biography

After graduating from secondary higher school for chemical engineering and gaining experience in industrial, analytical laboratories, Moritz started in Siconnex Wet-Process Engineering Department in Austria in March 2020. He switched over to Business Development in the beginning of 2024 and is now focused on market research and fostering relations with existing and new partners.

References

AI powered high sensitivity metrology boost yield

A. Chang
CTO
Angstrom Excellence ltd, Shen zhen, China, People's Republic of

Body

Metrology of semiconductor process characterization is crucial in both the initial process development/ramp-up phases and in-line inspection drives continuous process improvement. Smaller node sizes in Logic, 3D stacking trend in extreme HAR memory, and new materials adoptions continuously demands ultra-high sensitivity metrology with extreme measurement accuracy and reliability. AI and virtual metrology is integrated to assist with wafer metrology and inspection, defect detection, classification, and yield prediction, ultimately enhancing overall performance.

Biography

Dr. Xuena Zhang holds a B.S. in Physics from USTC, and an M.S. and Ph.D. in Physics from the Max Planck Institute in Germany, and she was a postdoctoral Fellow at Stanford University in US. She has extensive experience in optics, Ebeam, X-ray equipment, and is the inventor of a number of U.S. patents. Dr. Zhang has held various roles at KLA, Applied Materials, and other cutting-edge equipment companies, including scientist, R&D leader, and global product director. Her expertise lies in process/device integration, semiconductor metrology, and inspection in R&D, product launch, mass production, and global product management. Currently, she serves as the chairwoman and CTO of Shenzhen Angstrom Semiconductor Technology Co. Ltd., leading the R&D and marketing efforts for semiconductor metrology tools.

References

Proven Strategies to Speed AI Cycles, Delivering Millions in Value to Semiconductor Fabs

M. McDonnell
AI Strategist - Manufacturing
Teradata, Glattpark, Switzerland

Body

AI is being increasingly explored to enhance yield and throughput in semiconductor manufacturing. Due to the lengthy manufacturing processes, where functional testing is not available for weeks, earlier decision-making can deliver large rewards. However, data challenges restrict the number of analytic cycles that can be run, limiting the value AI can deliver.

A semiconductor fab is a challenging environment for process analytics. Wafer fabs and assembly locations produce vast amounts of data at high velocity. In addition, the data associated with a particular product must be knitted together from different formats, attached to different units of measure (e.g. lot, wafer, device) and collected at different times and steps of the process. Early adopters of AI in the fab most commonly site data volume and speed of analytic cycles as two key inhibitors in moving from pilot to full implementation of their algorithms.

The number of analytic cycles can be dramatically improved by bringing the AI to the data instead of taking the data to the AI algorithm. This minimises time consuming data movements and provides an easily auditable path from raw data through data transformations to the AI output. The approach is equally applicable for structured data, time series data and other complex data types such as images or video.

By bringing the AI algorithms to the data, semiconductor companies have experienced significantly faster analytical cycles. Faster analytic cycles can be run more frequently and on larger data sets, removing the need for sampling. The approach has already been proven in practice over multiple use cases in the semiconductor industry, with benefits measured in tens of millions of euros per year.

This talk will outline the principles of bringing AI to the data to speed analytic cycles, discuss the capabilities needed to implement this approach, and present some case studies.

Biography

Monica McDonnell is and experienced consultant in the field of enterprise software, digital transformation, big data, AI and analytics. She has spent her career consulting within the manufacturing industry in various roles. In her current role, Monica focuses on how manufacturers, inlcuding semiconductor companies, can move beyond the hype to deliver measureable business value from AI.

References

Cathodoluminescence analysis of wide-bandgap semiconductors for power electronics

T. Coenen
VP Business Development Materials
Delmic B.V., Delft, Netherlands

Body

Power electronic devices have diversified over the last years, where devices based on novel wide-bandgap materials such as GaN and SiC with superior electrical and thermal characteristics have emerged. Further along the horizon other materials with even wider bandgap such as Ga_20_3 , Diamond, and AlN are being considered and studied for power electronics applications. As these new materials become more mainstream a better understanding of their growth/epitaxy, processing and defect structure is needed in order to have reliable performance in power devices. This requires a proper view of material properties at the nanoscale where materials variations and defects manifest themselves.

Spatially-resolved cathodoluminescence (CL) imaging, in which the electron-beam-induced radiation is collected inside an electron microscope, is a techniques that holds great potential for nanoscale semiconductor materials analysis. The luminescence that is emitted from these semiconductor materials carry a signature of the electronic properties which can be used for characterization. The electron beam can locally excite the material with < 50 nm resolution and it can easily supply the required energy to excite (ultra) wide-bandgap semiconductors making it an ideal nanoscale probe. Here, we will present the latest developments in Cathodoluminescence for power applications. In particular, we will describe how CL can be used for fundamental research/R&D and for specific front-end manufacturing steps, with a particular emphasis on epitaxy. We will demonstrate some of the latest results on GaN and SiC in terms of defect analysis/quantification such as the imaging and compositional analysis of AlGaN in high-electron mobility transistors. We will connect this to some of the latest developments in CL imaging such as time-resolved CL imaging and demonstrate how this could impact the analysis of power semiconductors. We will describe our latest work on creating stable, reliable, high-resolution CL imaging while reaching time-resolutions of <100 ps, needed for wide bandgap materials analysis given their short excited state lifetimes. Our approach is based on a ultrafast blanking system in a scanning electron microscope which is connected to ultrafast CL detection using single-photon detectors as well as a state-of-the-art streak camera system.

Biography

Toon Coenen studied chemistry and physics at Utrecht University where he obtained an MSc degree in 2010. He continued for a PhD at the NWO Institute AMOLF in Amsterdam, the Netherlands, in Professor Albert Polman's group. There he co-developed the first version of the SPARC cathodoluminescence (CL) detection system and used it to investigate the nanoscale optical properties of nanophotonic systems. During his PhD he also was a visiting scientist at Stanford University in the group of Professor Mark Brongersma. Then he moved to Delmic, a Dutch tech company specialized in integrated optical/electron microscopy solutions such as Cathodoluminescence microscopy. There he first worked as an application specialist and product manager, and director of Materials Science further developing the CL technology, including developments in time-and angle-resolved CL microscopy. Currently, he is VP Business development for the Materials Science division at Delmic, where he is responsible for the strategic roadmap and business development for semiconductor applications of cathodoluminescence, focusing on the analysis of next generation compound semiconductor devices for photonics, displays, RF, and power electronics applications.

LinkedIn: nl.linkedin.com/pub/toon-coenen/27/133/46b/
Google scholar account: http://scholar.google.nl/citations?user=N3z1wh8AAAAJ
ResearchGate: https://www.researchgate.net/profile/Toon_Coenen

References