Future Disruptions

S. Raithel
COO
DAS Environmental Expert GmbH, Dresden, Germany

Body
Session Chair

Biography
Stephan Raithel joined DAS in 2016 and since then holds the position of the COO Gas Treatment. In his position he is overseeing all aspects of DAS' gas treatment products, such as development, engineering, product management, procurement, customer care and production.

From 2007 until 2016 he was working for SEMI, the global semiconductor equipment and materials association, where he held various positions within the association – from operations management, SEMI standards and PV Roadmap program to the role of the Managing Director of SEMI Europe.

Before his start in the semiconductor industry, he was employed as a project manager in the financial ,creative services and consumer goods industry.

References

CEE: Future Location of Semiconductor Investments

M. Trunin
Director
Invest in Pomerania, Gdańsk, Poland

Body

The presentation provides a comprehensive exploration of the key factors influencing the decision to locate new semiconductor investments in CEE and Pomerania, taking into account geopolitical, logistical, environmental, and supply chain dynamics.

The CEE countries have stable governments, growing economies, and a strong presence in NATO and the EU, making them attractive for investment. Moreover, the alignment with EU and NATO policies reduces risks associated with instability, making them ideal for long-term investments, especially in manufacturing and tech sectors.

Russia's aggression in Ukraine has raised concerns about the security of supply routes and energy dependence. The CEE countries, Poland in particular, have taken steps to reduce dependence on Russian energy, strengthening energy security and reducing risks for manufacturing.

The importance of coastal access and central positioning is not to be overlooked. Proximity to the sea and ports and international routes reduces the cost and complexity of importing raw materials and exporting finished products, while access to maritime, railway and express routes is crucial for global supply chain integration in the semiconductor industry.

With the EU moving toward stricter regulations on per- and polyfluoroalkyl substances (PFAS) due to their environmental and health risks. Investing in the CEE and Pomerania allows companies to build manufacturing processes that are compliant with future regulations, making the industry more sustainable and future-proof. The availability of green energy (wind farms in the Baltic Sea, for example) further supports sustainable semiconductor production.

Biography

Deputy Director at Invest in Pomerania, a local investment promotion agency responsible for attracting foreign direct investments to the Pomeranian Voivodeship (northern Poland). During over 10 years in the organization, he directly supported investment projects of such companies as Intel, Northvolt, Flex, Alteams, ThyssenKrupp, Siemens Gamesa, Archer, Lacroix Electronics. Thanks to his experience and extensive business knowledge, Mikołaj is able to efficiently support every investment process. As highlighted by investors, it is often the activities of the Invest in Pomerania initiative that have contributed to choosing Pomerania as an investment destination. According to the World Bank analysis, the impact of Invest in Pomerania's activities from 2011 to 2020 on the growth of jobs related to foreign direct investment was 230%.

References

Sustainable by design: How Soitec drives the transition toward a sustainable economy through innovation and operations

F. Bernard
Deputy Sustainability
Soitec, Bernin, France

Body

At Soitec, our products are designed and manufactured to provide greater performance, security and agility, while guaranteeing energy efficiency to the resulting applications. This is the heart of our technology and our value proposition. Sustainability thus integrates Soitec's core business with the energy efficiency of its products. This has naturally inspired and structured the way we conduct our activities.
For several years, we have been constantly innovating to manage our activities more sustainably, with a particular attention to reducing the carbon footprint of the entire microelectronics value chain, reducing our water withdrawals and taking into account environmental criteria in the design of our products.

Biography

Fanny Bernard joined Soitec in 2010 and is currently Deputy of Sustainability Department. She works on issues of impact and responsibility, both on the environmental, societal and territorial aspects.

With more than 10 years of experience in corporate and internal communications in international industrial environments, Fanny specializes in ESG and benefits from expertise around responsibility and sustainability issues. From 2020, as ESG manager, she was responsible for creating and implementing Soitec's ESG strategy in line with the company's strategy. She has coordinated the different stakeholders, set up extra-financial reporting and worked to raise awareness and popularize all of the group's commitments to various audiences such as employees, investors, institutions and the general public.

Fanny graduated from Sciences Po Strasbourg and Grenoble Ecole de Management.

References

Co-Optimized Heterogeneous Augmented Reality Systems Enabled with Wearable and Personalized Artificial Intelligence

S. Kang
Senior Vice President of Semiconductor Strategy
Adeia, Semiconductor Strategy, San Jose, United States of America

Body

The proliferation of AI into new verticals will drive the co-integration of silicon devices, optical devices, and sensors into a unified platform. One can envision an AI-enabled augmented reality system that is always on, wearable, and personalized. This can serve as a flagship heterogeneous system co-optimized for computing, energy efficiency, and seamless user interface, while also prioritizing small form factor, comfort, and trendy design. From a semiconductor hardware perspective, a key enabler is the co-integration of an energy-efficient AI system built on silicon with an ultra-high-resolution III-V display device and state-of-the-art sensors. Such a system must function in all wearable environments, including bright sunlight and extreme weather conditions. Due to the heterogeneous nature and a tiny form factor requirement, this system necessitates an advanced three-dimensional integration. This presentation will provide an overview of such an emerging platform and its key technological attributes from the perspective of heterogeneous semiconductor integration and co-optimization.

Biography

Dr. Seung Kang serves as Senior Vice President of Semiconductor Strategy at Adeia, where he oversees strategic semiconductor programs encompassing technology, design, and system co-optimization. Prior to joining Adeia, Dr. Kang held a distinguished career at Qualcomm Technologies, Inc., where he spearheaded the Advanced Memory Program, pioneering early R&D and IP validation across the semiconductor ecosystem. His leadership also extended to the development of foundational logic IP for semiconductor nodes ranging from 7 nanometers down to 3 nanometers, supporting Qualcomm's flagship mobile, automotive, AI, and IoT products. Before his tenure at Qualcomm, Dr. Kang made significant contributions at Lucent Technologies Bell Laboratories and Lawrence Berkeley National Laboratory. He earned his B.S. and M.S. degrees from Seoul National University, Korea, and a Ph.D. from the University of California, Berkeley. Dr. Kang is a highly accomplished inventor, holding 250 U.S. patents and over 1000 patents granted globally. His research contributions are widely recognized, with over 100 published papers. He served as a Distinguished Lecturer for the IEEE Electron Device Society from 2014 to 2018 and has been a Specially Appointed Visiting Professor at the Center for Innovative Integrated Electronic Systems, Tohoku University, Japan.

References

Jumping the Barriers of Future Lithography

M. van de Kerkhof
Director EUV Research
ASML, Research, Helmond, Netherlands

Body

In the past years, EUV lithography has been adopted for manufacturing of state-of-the-art Integrated Circuits, with critical dimensions down to 10 nm. With the introduction of a larger NA=0.55, these dimensions will become smaller still. This will further tighten requirements on CD and pattern placement control to ensure yielding devices with dimensions below 10 nm, raising questions on the limits of the shrink that may be achieved in manufacturing reality, in terms of both exposures and chemical and etching processes.
At the same time, investigations have started to push these limits even further by increasing the NA even further to NA=0.75 or beyond, or alternatively to lower the wavelength below 13.5 nm.

This presentation will discuss the principles of EUV Lithography, its challenges and limitations for NA=0.33 and NA=0.55, and possible options to jump the barriers holding us back from doing lithography at critical dimensions down to 5 nm.

Biography

Mark A. van de Kerkhof is the Director for EUV Projects at ASML Research, based in Veldhoven, The Netherlands.

He received an M.Sc. in Applied Physics from Eindhoven University of Technology, and a PhD in EUV-induced Plasma, also at Eindhoven University of Technology. He began his career at ODME, working on the development mastering processes for DVD and Blu-Ray. In 1999 he joined ASML as senior designer and later project manager, working on development of miscellaneous sensors as well as projection optics in both DUV and EUV scanners. He currently is Director for EUV projects at ASML Research, as well as assistant professor for Plasma Physics at Eindhoven University of Technology.

He holds over 100 patents and authored or co-authored more than 50 scientific papers. He frequently presents at conferences about both photolithography and plasma physics. He is a Fellow of SPIE.

References

What measures is the semiconductor industry taking to replace PFAS in production processes?

M. Fraunhofer IPMS
Scientific Employee, Clean Room Sustainability Mangager
Fraunhofer IPMS, Dresden, Germany

Body

No microelectronics without PFAS! This has been true for 50 years, but emerging regulation, impulses from industry and the existing environmental risks require rapid and effective action from science and the microelectronics industry. What measures are currently being taken in the research field to develop alternatives. We will give a broad overview of various solutions from lithography to passivation and etching, covering almost the entire manufacturing process of microelectronics.

Biography

Marco Kircher has almost a decade of experience in MEMS development at Fraunhofer IPMS and completed a degree in electrical engineering with focus on biomedical engineering at TUD. He specializes in innovative ultrasonic sensors for medical applications and participates to various industry and EU projects, including e.g. the projects Position II and ThrombUS. His work in the production of MEMS has provided deep insights into process development, now applied to make microelectronics manufacturing process more environmentally friendly. Within the »Green ICT @ FMD« project, Marco is leading all developments in resource-optimized microelectronics and MEMS-production, bundling the know-how in the Research Fab Microelectronics Germany.

References