Future of Work: Skills & DEIB

C. Melvin
Senior Director, Business Development and Operations
SEMI Europe, Berlin, Germany

Biography
Cassandra Melvin received her BS in Business Management and Neuropsychology at Rensselaer Polytechnic Institute and is Director of Operations at SEMI Europe.
For the nine years prior to joining SEMI, she held the position Global Product Manager at Atotech Deutschland GmbH, where she was responsible for managing several hundred electroplating chemistry products in its Semiconductor and Functional Electronic Coatings division. She began her career at the SUNY Polytechnic Institute (formerly the College of Nanoscale Science and Engineering) as a Business Manager focused on strategic and technical programs for semiconductor chemistry and equipment manufacturers. She also held various project and program management roles in clean room operations and IT at SUNY.
Cassandra's written work has been published in leading technical magazines and presented at key conferences globally. As an advocate for diversity and inclusion, she is actively involved in SEMI's efforts to promote diversity within the semiconductor industry.

References

AI – Enabling a Revolution in Chip Design Productivity

T. Bjerregaard
Senior Director of AI
Synopsys, Paris, France

Abstract
AI, and in particularly generative AI technologies, are set to transform entire industries. AI-based chip design flows are yielding better results and improving designer productivity by adding automation capabilities to assist human experts in the design process. In this talk I will look at the history of AI that has led us to this point and outline key uses of AI in EDA. I will look across the EDA stack at where AI-based approaches have made the highest impact and also look at how generative AI technologies can help capture human knowhow and as such help to mitigate the talent gap that the chip design industry is facing.

Biography

Tobias Bjerregaard
MBA in General Management, Copenhagen Business School (2017)
PhD in Asynchronous Circuit Design and Networks-on-Chip, Technical University of Denmark (2005)
MSEE in Solid State Physics, Technical University of Denmark (2000)
CEO and founder of startup Teklatech, acquired by Synopsys in 2018. Currently Sr Director of AI at Synopsys, leading a group of AI R&D teams across the US and Europe that explores, develops and markets new EDA methods and tools based on advanced, state-of-the-art AI technologies

References

AI-Driven 3D X-Ray Inspection: A Game-Changer for Advanced Semiconductor Packages

I. Drolz
Vice President Marketing & Product Strategy
Comet, Hamburg, Germany

Abstract
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Biography
Isabella Drolz is the Vice President Product Marketing at Comet Yxlon, which is the industrial X-ray & CT inspection system division of Comet. Comet Yxlon provides X-ray & CT inspection solutions for R&D labs & production environments, especially for Semiconductor customers to enhance their productivity. In her role, she is responsible for product management, business development, global application solution centers, and marketing at Comet Yxlon. Isabella has next to her industrial engineering education, a Bachelor of Science in International Business Administration, and an MBA degree from Southern Nazarene University in Oklahoma City, USA. She has held several management positions in the mechanical and plant engineering industry driving market-oriented product development.

References

CEE: Future Location of Semiconductor Investments

M. Trunin
Director
Invest in Pomerania, Gdańsk, Poland

Abstract
The presentation provides a comprehensive exploration of the key factors influencing the decision to locate new semiconductor investments in CEE and Pomerania, taking into account geopolitical, logistical, environmental, and supply chain dynamics.
The CEE countries have stable governments, growing economies, and a strong presence in NATO and the EU, making them attractive for investment. Moreover, the alignment with EU and NATO policies reduces risks associated with instability, making them ideal for long-term investments, especially in manufacturing and tech sectors.
Russia's aggression in Ukraine has raised concerns about the security of supply routes and energy dependence. The CEE countries, Poland in particular, have taken steps to reduce dependence on Russian energy, strengthening energy security and reducing risks for manufacturing.
The importance of coastal access and central positioning is not to be overlooked. Proximity to the sea and ports and international routes reduces the cost and complexity of importing raw materials and exporting finished products, while access to maritime, railway and express routes is crucial for global supply chain integration in the semiconductor industry.
With the EU moving toward stricter regulations on per- and polyfluoroalkyl substances (PFAS) due to their environmental and health risks. Investing in the CEE and Pomerania allows companies to build manufacturing processes that are compliant with future regulations, making the industry more sustainable and future-proof. The availability of green energy (wind farms in the Baltic Sea, for example) further supports sustainable semiconductor production.

Biography
Deputy Director at Invest in Pomerania, a local investment promotion agency responsible for attracting foreign direct investments to the Pomeranian Voivodeship (northern Poland). During over 10 years in the organization, he directly supported investment projects of such companies as Intel, Northvolt, Flex, Alteams, ThyssenKrupp, Siemens Gamesa, Archer, Lacroix Electronics. Thanks to his experience and extensive business knowledge, Mikołaj is able to efficiently support every investment process. As highlighted by investors, it is often the activities of the Invest in Pomerania initiative that have contributed to choosing Pomerania as an investment destination. According to the World Bank analysis, the impact of Invest in Pomerania's activities from 2011 to 2020 on the growth of jobs related to foreign direct investment was 230%.

References

Future of Work Panel

D. Collins
General Manager, SPTS Division, KLA Corporation
KLA Corporation, Newport, United Kingdom

Abstract
n/a

Biography
Dan Collins is General Manager of the SPTS Division within KLA Corp. After joining SPTS in 2016 as Supply Chain Director, Dan was promoted to VP Operations in 2019 and has been instrumental in driving the improvements to the company's manufacturing operations. As General Manager he is overseeing the integration of SPTS into KLA, involving new processes, systems and employee culture during a period of significant growth for the business. He has previous operations experience with Edwards and Cooper Tire & Rubber Company with exposure to supply chain management in the semiconductor, automotive, and other industries. He holds a BSc(Hons) in Astrophysics from Queen Mary University of London, and MSc in Technology Management.

References

M. D. Perez
Communications Manager
SEMI Europe, Berlin, Germany

Biography
Maria Daniela Perez is the Communications Manager at SEMI Europe, overseeing regional marketing and communications efforts. With extensive experience working with global teams, Maria excels at crafting strategies that enhance SEMI's visibility and engagement. She is also passionate about workforce development and leads the 20Under30 initiative, which focuses on empowering young professionals in the industry.

References

Topic Coming Soon

A. Iranzadeh
Digital Transformation Program Manager
X-FAB MEMS Foundry Itzehoe, Itzehoe, Germany

Abstract
Coming Soon

Biography
Coming Soon

References

Topic Coming Soon

S. Massar
R&D Engineer
Imec, Leuven, Belgium

Abstract
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Biography
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References

Explore the Journey of a Young Engineer Driving Innovation in the Semiconductor Industry

P. Döll
Phyiscal Implementation Engineer
Racyics GmbH, Dresden, Germany

Abstract
Get an insight to my journey as a SEMI 20 under 30 winner, from early years through university to managing cutting-edge projects in the semiconductor industry. Discover what the workday of a chip designer in a mid-tier business looks like and where the role extends beyond engineering to project management, marketing, and product leadership.

In this talk, I will share my personal experiences and challenges, illustrating how a passion for semiconductors can lead you to diverse and rewarding career paths. Furthermore, together we will explore the world of semiconductor design within Racyics – Europe's leading Design Partner for Integrated Circuits - and highlighting the unique opportunities for growth and innovation. We will also touch on the future opportunities within the company, offering insights into how these roles can evolve and intersect.

Whether you're curious about the life of a chip designer or eager to explore broader opportunities in microelectronics, this talk offers valuable insights and inspiration for anyone at the start of their professional journey.

Biography
Patrick Döll is an experienced Physical IC Design Engineer at Racyics with a master's degree from the RWTH Aachen university, specializing in Micro- and Nanoelectronics. Due to his contribution to numerous tapeouts in advanced nodes, he shows expertise in the entire chip design process, from the initial design stage to the final product, which allows him to manage cutting-edge projects in the semiconductor industry. On top, he actively supports the Design Enablement Service of Racyics by participating in the product development of makeChip - a cloud-based chip design platform - and is involved in the company's marketing efforts.

References

Damage-Free Plasma Enhanced Atomic Layer Deposition of AlOX Dielectrics for Tunable Doping of 2D Materials

A. Esteki
PhD student
RWTH Aachen University, Chair of Electronic Devices, Aachen, Germany

Abstract
Two-dimensional materials (2DMs) such as graphene and transition metal dichalcogenides (TMDs) have great potential for heterogeneous integration with advanced silicon technology for future electronics[1–4]. Most prominently, the latter are considered as channel materials in ultimately scaled metal oxide semiconductor field effect transistors (MOSFETs)[5–9]. Two open challenges toward their application are the damage-free deposition of high-quality high-κ dielectrics on the 2DMs and controllable doping of the channel to adjust threshold voltages[10].
In this work, we deposited a non-stoichiometric aluminum oxide (AlOX) layer using an Oxford Instruments Atomfab™ plasma enhanced atomic layer deposition (PEALD) system. This AlOX layer, containing nitrogen and carbon, differs from stoichiometric Al_2O_3. Short, low-power process steps with remote plasma conditions[11] were used to directly grow a thin layer of AlOX on commercially available graphene and on MoS_2 which was grown in an AIXTRON MOCVD reactor. Raman spectroscopy data showed no discernible deterioration of the 2DM compared to a standard Al_2O_3 process. We further validate the 2DM quality with electrical data from field-effect transistors (FETs) encapsulated with AlOX. The current-voltage measurements were performed in a four-point configuration to avoid a strong influence of the contact resistance before and after dielectric deposition under ambient conditions. The AlOX dielectric passivation improved the carrier mobilities in the devices. In addition, the process allows the tuning of graphene´s Dirac and MoS_2´s threshold voltages proportional to the thickness of the AlOX layer. Our results show that PEALD deposited AlOX provides a promising route for the encapsulation of 2DM-based electronic devices, as it improves device performance and can be used to tune the Dirac or threshold voltages at the same time.
Acknowledgments: This work was funded by the European Union under the Horizon Europe grants 2D-EPL (952792), Graphene Flagship Core 3 (881603), and the German BMBF project GIMMIK (03XP0210).

Biography

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References

Atomic Layer Etching of SiO_2 using SF_6

R. Venugopal
Master's student
Center for Hybrid Nanostructures, University of Hamburg, Hamburg, Germany

Abstract

In the relentless pursuit of advancing semiconductor technologies, the demand for atomic layer processes has given rise to innovative processes. Atomic layer deposition has already played a significant role in the ongoing miniaturization features. In the meantime, atomic layer etching (ALE) is gaining increasing traction which offers better control over material removal at the atomic level. Our research focuses on using Sulfur hexafluoride (SF_6) and Ar Plasma to perform the ALE for etching silicon dioxide (SiO_2). In our ALE loop process, firstly SF_6 is injected to be adsorbed onto the SiO_2 surface. Secondly, Ar plasma is generated, following which, F radicals are produced which react with the surface to modify it into purgeable gaseous products. Here we show our ALE process on silicon dioxide wafer using SF_6 and Ar Plasma, obtaining a constant etching rate of around 0.14 nm/cycle across independent multiple-cycle runs. Combining the systematic exploration on operating pressure, temperature, plasma power, and SF_6 dose, it is confirmed that the SF_6 does not etch surfaces directly but forms a self-limiting layer, with etching initiated only by the presence of Ar plasma and F radicals. Additionally, detailed atomic force microscopy characterization over multiple cycles reveals minimal changes in surface roughness, presenting a conformal surface etching. Our research provides a dependable, reproducible, and highly controlled ALE process for SiO_2 etch-related nanofabrication process.

Biography

I am Rakshith Venugopal, a Master of Physics student at the University of Hamburg. I currently am working on my master thesis at the Center for Hybrid Nanosctructures (CHyN). After completing my Bachelor of Science in India, I started my journey in pursuing a master's in Hamburg. I gained a passion for nanosciences after starting my masters which pushed me into choosing the topic " Atomic Layer Etching of SiO_2 using SF_6" as my Master thesis topic.

Contributing Authors: Prof. Dr. Robert H Blick, Dr. Robert Zierold, Jun Peng
Center for Hybrid Nanostructures, Universität Hamburg

References

Mechanism of antiferroelectricity in polycrystalline ZrO_2

R. Ganser
PhD Student
Munich University of Applied Sciences, Applied Sciences and Mechatronic, Munich, Germany

Abstract

The size and electric field dependent induction of polarization in antiferroelectric ZrO_2 is the key to several technological applications that were unimaginable a decade ago. However, the lack of a deeper understanding of the mechanism hinders progress. Molecular dynamics simulations of polycrystalline ZrO_2, based on machine-learned interatomic forces with near ab initio quality, shed light on the fundamental mechanism of the size effect on the transition fields. Stress in the oxygen sublattice is the most important factor. The so constructed interatomic forces allow the calculation of the transition fields as a function of the ZrO_2 film thickness and predict the ferroelectricity at large thickness. The simulation results are validated with electrical and piezo response force microscopy measurements. The results allow a clear interpretation of the properties of the double-hysteresis loops as well as the construction of the free energy landscape of ZrO_2 grains.

Biography

Dear Ladies and Gentlemen,
My name is Richard Ganser and I work as PhD student at the Munich University of Applied Sciences since February 2021. After my bachelor's degree in technical physics, I decided to deepen my knowledge of semiconductor electronics by studying micro- and nanotechnology. During my studies, I got to know the tools of modern semiconductor research and production from both the theoretical and experimental sides. Inspired by the rapid progress in the field of chip technology, I decided to pursue a PhD in the field of materials science with a focus on ultrathin ferroelectric films for use in state-of-the-art high-performance chips.
The basic idea behind the use of ferroelectric materials is to utilize them as non-volatile random access memory, since the access speed is similar to that of classical RAM, i.e. a working memory that retains its last state when powered off. This development would revolutionize today's computer technology by eliminating the separation between RAM and classic flash memory (hard disk). Even today, the bottleneck in high-performance AI chips is no longer the actual computing power, but the communication speed between RAM and flash, the so-called von Neumann bottleneck, which could be overcome by using FeRAM. FeRAM with ferroelectric PZT as gate layer has been on the market for a long time, but PZT loses its ferroelectric properties below 30nm thickness, which makes the required miniaturization impossible, due to the resulting limited transistor density the devices in question remain uneconomically large and low in performance. Hafnium- and zirconium oxide, introduced 10 years ago, offer an attractive alternative by retaining their ferroelectric properties down to a few nanometers. Much research is being carried out to stabilize and optimize the desired properties, both experimentally and theoretically, as the exact origin of the ferroelectric properties has not yet been conclusively clarified. As part of an international team with groups in France and Portugal, among others, we support our experimental project partners in Dresden with the help of computer simulations. These allow predictions to be made about remanent polarization and phase stability as a function of deformation, doping, and temperature. This requires enormous computing power, which is why we calculate on the SuperMUC in Garching. Despite the use of high-performance computing, conventional ab initio simulations are limited to a few hundred atoms and a few thousand simulation steps. A new method I am using is the use of machine-learned potentials based on ab initio training data. These potentials model the interaction, attraction and repulsion, of the individual atoms among each other and can thus be computed several thousand times larger, up to about 10 cubic nanometers, which corresponds to a realistic grain size in thin films, and several hundred times faster. This allows the investigation of temperature-dependent properties with high statistics and accuracy, such as the change in polarization and even phase transformations down to the smallest atomistic detail. In my work, I also coupled external electric fields to the ions. In this way, I obtained the extensive pyro- and piezoelectric properties of ZrO2 as a function of temperature, which include electrostriction, giant piezoelectric effects at the phase boundary, and negative genuine piezoelectric coefficients. By coupling electric fields into the transient simulation, the ferroelectric switching behavior can be simulated and questions such as the writing speed, which is of enormous

importance for use in high-performance computers, can be answered.
Another question that remains unanswered is how to stabilize the antiferroelectricity in zirconia. While zirconia crystallizes in a weakly dielectric phase, the monoclinic phase, as a bulk material, e.g. used as dental prosthesis, a strongly dielectric phase, the tetragonal phase, is formed in films below 10 nm, which is already used today as a high-k gate material. Ab initio calculations of pure crystals show that the tetragonal phase transitions to the monoclinic phase due to the higher free energy, which is a discrepancy between simulations and experiments in thin films. Using machine-learned potentials with molecular dynamics simulations, we can simulate a polycrystalline ZrO_2 thin film including the grain boundary, stabilize the tetragonal phase at room temperature and investigate the piezoelectric response in direct comparison with experimental piezoelectric force microscopy data. This result represents a breakthrough in solid-state materials simulation and is currently being published in great detail in Advanced Functional Materials. After stabilizing the antiferroelectricity at room temperature in simulations and experiments, the next step in simulation is the addition of hafnium to the machine-learned potential to stabilize the ferroelectric phase over a wider range of film thicknesses and grain sizes, in agreement with experimental results, and to allow a gradual polarization of the films, for example via the grain size distribution. This gradual polarization of the films is of great industrial interest as it allows the modeling of individual synapses. The degree of polarisation and thus the current flowing through the FET is used to store the weight, the strength of the connection between the synapses, in the neuronal network. This hardware approach could enable significant miniaturization of the required computing architecture and lay the foundation for the development of future AI.
Sincerely yours,
Richard Ganser

References

Performance Analysis and Implementation of Automated LLM-basedTechniques for Crosslanguage Code Conversion and Acceleration of HardwareSoC Development

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Anhalt University of Applied Sciences, Electrical engineering, mechanical engineering and industrial engineering, Köthen (Anhalt), Germany

Abstract
Developing complex systems often necessitates collaboration between software and hardware teams using high-level and low-level programming languages. For narrowly focused companies, which typically have fixed sized number of specialists in application design, this programming language barrier can result in code inefficiencies, extended development cycles, a significant number of bugs, and challenges related to efficient architecture design and debugging strategies. Recent advancements in Machine Learning (ML) and Large Language Models (LLM) such as CodeT5, Copilot, GPT-4o, AI-HDLCoder etc. have
opened up new possibilities for automating code generation tasks. However, the proposed models are not cross language based in terms of code programming, and need a short, clear description of a technical task based on Natural Language Processing (NLP) techniques. The proposed work, on the other side, represents the novel instrument demonstrating the AI potential to bridge the gap between python high-level developers and low -level hardware programmers that are using the VHDL language to realize numerous FPGA-based architectures. Exploring different approaches of python instruments and using knowledge of traditional code converters, the proposed work tries to solve the challenges of automated Python to VHDL code generation without additional verification / validation steps and simplify the pitfalls of software obsolescence. Sufficient results or comprehensive approaches need to influence the research and industry application development backgrounds for further matched cooperations and investigations of code generators and compilers, empowering the Industry 5.0 by new generation of code conversion frameworks for rapid prototyping and fast migration of FPGA-based hardware designs, which can lead to planned decrease in additional financial expanses or minimization of development time for a certain project under application development phase.

Biography

Vladyslav Romashchenko

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August 2019 - November 2023
Founder, Development Team Lead

3 CosmoPay/ Odessa (Ukraine)
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References