EU Digital Forum

C. Frieling
Director for Advocacy and Public Policy
SEMI Europe, Brussels, Belgium

Biography
Christopher Frieling is Director for Advocacy and Public Policy at the SEMI Europe Brussels Office. Christopher has a background in EU affairs, innovation, and tech policy. Prior to SEMI he worked at the Brussels office of Fraunhofer in several roles including most recently as Senior Advisor. Christopher holds an MSc in Economics of Science and Innovation and a Bachelor of Business Administration.

References

Horizon Europe ICOS (International Cooperation on Semiconductors): EU and Non-EU Strengths, Weaknesses, Dependencies, Opportunities for International Collaboration

F. Balestra
Director of Research
CNRS-Grenoble INP-Sinano Institute, Grenoble, France

Abstract
This presentation will deal with the ICOS CSA project dedicated to International Cooperation On Semiconductors. International cooperation is key for speeding up technological innovation, reducing cost by avoiding duplicated research, boosting the resilience of the semiconductor value and supply chains, and is one of the objectives of the EU Chips Act. The objectives and first important ICOS results will be highlighted, including the analysis of the semiconductor economic and technological landscapes in Europe and leading semiconductor countries, the identification of areas for potential cooperation and the proposition of opportunities for bilateral or multilateral research collaborations, particularly in the areas of advanced functionalities and computing.

Biography
BALESTRA Francis, CNRS Research Director at CROMA, is Director Emeritus of the European SiNANO

Institute and President of IEEE Electron Device Society France, and has been Director of several Research labs. He coordinated many European Projects (ICOS, NEREID, NANOFUNCTION, NANOSIL, etc.) that have represented unprecedented collaborations in Europe in the field of Nanoelectronics. He founded and organized many international Conferences, and has co-authored more than 500 publications. He is member of several European Scientific Councils, of the Advisory Committees of International Journals and of the IRDS (International Roadmap for Devices and Systems) International Roadmap Committee as representative of Europe.

References

HiCONNECTS Introduction

K. Srivastava
Senior Specialist, Communications
SEMI Europe, Marketing and Communications,
Berlin, Germany

Abstract
Coming Soon

Biography
Kartikey Srivastava is Senior Specialist - Communications at SEMI Europe. A member of SEMI Europe's team since 2023, his focus is on the Dissemination and Exploitation of Erasmus+ and Horizon Europe projects such as HiCONNECTS, ECDA and ECSA.

References

Demonstration of High-Speed Silicon Photonics I/O for Co-Packaged Pilot Line

C.-J. Luo
R&D Engineer
IMEC, Silicon Photonics, Leuven, Belgium

Abstract
The high-level objective of HiCONNECTS project is to support industrial challenges by developing heterogenous integration technology solutions for energy-efficient and high-performance cloud and edge computing. HiCONNECTS pilot lines aim at developing advanced photonic integrated circuits, the tasks involve high-speed optical interconnect, co-packaged optics, and heterogenous integration. In this presentation, we discuss the development of the pilot lines and show the challenges/breakthroughs.

Biography
Cheng-Jhih Luo is the R&D engineer of silicon photonics pathfinding at imec. His works focus on photonic component and micro-optical system design especially aim to advanced co-packaged optics for silicon photonics. He received Ph.D from National Chiao-Tung University Taiwan in 2019 and previously Cheng-Jhih worked as deputy project manager at ITRI for host several technical projects regarding photonic systems.

References

Novel Interconnect Solutions for improved signal Integrity performance

E. Schlaffer
Programme Manager
AT&S AG, Research and Development, Leoben, Austria

Abstract
Title: Novel Interconnect Solutions for improved Signal Integrity performance
5G Telecommunication & High Resolution Radar Applications are pushing RF components into new designs, new materials, new packages, new substrates and improved PCB concepts.
This Abstract addresses the future market requirements and examines the development of novel Interconnect solution, suitable for high-frequency circuits.
Regardless of the application and the product, the aim is to increase the data transfer rate (GB/s). This requirement is implemented by increasing the frequency. Examples include radar systems in the automotive business, but also applications from telecommunications, which are used in Millimeter Wave frequency bands (30-140 GHz) or for signal transmission up to 50 Gbps.
Furthermore, we will propose advanced novel solutions tackling integrity losses & challenges in order to increase signal speeds and thus fulfill demands especially for high-frequency applications.
An additional factor for Signal loss reduction are Design constrains like Miniaturization and Modularization.
One of the key enabling Technologies which is carried out in this Abstract is Embedding of active and passive components in the stack up of an Interconnect Solution. Bare dies are embedded in a multiple layer Stack up of a PCB and interconnected with galvanic copper. Direct copper via connection induces less signal losses as compared with SMT mounted or wire bonded RFICs. The embedded Components can be interconnected single sided or double sided. The double sided method allows a separation of the signal path to the Antenna or other Signal routed elements and the thermal path to the Heat sink. Furthermore, it´s an efficient method to shorten the signal path from the RF IC towards the Antenna and open up the possibility to use the external plane for placing SMT components. Embedding is paving the way to apply vertical integration and reduce the overall footprint and miniaturize the design of an electrical Circuit. Therefore smaller Traces with lower Tolerances are required. A so called modified Semi Additiv Process Structuring method gives the possibility to reduce the width of Signal Traces and the Space in between Traces to approx. 25µm with max. 5% Tolerance.
Less impedance changes due to improved line-width control ensure high level of signal integrity.Because of the manufacturing method more accurate line-shape and smooth copper surfaces reduces losses by minimizing the losses skin effect.

Biography
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Biography
Erich is an Austrian citizen with a technical college for electrical engineering in Kapfenberg. He joined as Process Engineer of AT&S in December 1998 and was responsible as Department Head for mechanical drilling, laser drilling, routing and electrical test.
From 2008 - 2012 he was responsible for the development of a novel Photovoltaic Module Programme.
Since 2012 he is developing Concepts for High Speed and Radio Frequency applications as a Programme

Manager in R&D.

References

Sharper scans, faster ramp up

J. Hållstedt
Head of Segment - Semi and Electronics
Excillum, Stockholm Kista, Sweden

Abstract
High-density interconnects. Micron-scale solder bumps. Sub-micron defects. As semiconductor architecture grows more complex with 3D heterogenous integration and ever decreasing dimensions, critical reliability issues arise with smaller defects. To achieve faster ramp-up with better yield, the next generation of inspection tools need to be faster with a major increase in 3D imaging resolution down to sub-micron level. Whether the aim is to understand failure mechanisms, improve design or increase yield in next-generation 3D heterogenous integration, a new era of nanoscale technologies demands a leap forward in nano-CT and laminography resolution. In this communication we will show how the Excillum NanoTube N3 x-ray source enables the X-ray path forward for advanced packaging metrology.

Biography
Julius Hållstedt has since 2009 worked in global deep/high tech companies with development, implementation and market introduction of various X-ray analysis solutions for both research and industrial applications.
He is currently the head of segment for semiconductor and electronics at Excillum, with the main focus on addressing the metrology challenge the industry is facing due to the increased complexity with smaller dimensions, increased dense packing and 3-dimensional structures causing many existing measurement techniques to run out of steam.
Excillum based in Kista, Sweden develops and manufactures the world's most advanced X-ray sources based on unique technology originally developed by researchers at KTH and Julius' main task now is to create business and partner collaborations with global players to implement Excillum's solutions in the leading electronics and semi R&D and manufacturing sites around in the world.
Julius Hållstedt obtained his Masters of Science degree in materials science in 2002 and his doctorate in solid state electronics in 2007 from the Royal Institute of Technology (KTH), Stockholm.

References