SEMICON® EUROPA CONNECT
14–17 NOV, 2017 MESSE MÜNCHEN, MUNICH, GERMANY

Power Electronics Conference

H. Pairitsch
Senior Manager Technology & Innovation
Infineon Technologies, Villach, Austria

Biography
Herbert Pairitsch holds a degree in electrical engineering from the Graz University of Technology, from where he graduated in the year 1985. In 1986 he started his career at Infineon Technologies Austria AG (former Siemens HL) and held leading positions at various manufacturing and development departments. Since 2014 he serves as divisional Head of R&D Funding PMM (Power Management & Multimarket). His responsibilities include the coordination of national and international research projects in the context of energy efficient electronics like PowerBase (ECSEL Pilot line project).

Power Electronics of highest power density for Automotive Applications

F. Hilpert
Groupleader Aviation Power Electronics
Fraunhofer Institute for Integrated Systems and Device Technology IISB, Vehicle Electronics, Erlangen, Germany

Abstract
Over the last decade new Technologies in power electronics like WBG Devices enabled the development of systems with highest power densities. As volumetric designspace is crucial in the design of Automotive Systems, this opened up a broad field of Automotive Applications especially in power regions above 100kW. Today there is a wide and growing field in Power Electronics for Automotive Applications, ranging from HV DCDC converters and drive inverters for electric vehicles to intelligent power distribution in the LV board grid for fault tolerant E/E architectures in automated driving vehicles.

The presentation will focus on latest research prototype systems developed mainly for Automotive Applications to illustrate the advantages of new WBG technologies together with advanced system design like low inductive module packaging.

The development of systems with highest volumetric power densities also constantly reduced the weight of the power electronics, enabling the development of lightweight Systems with high gravimetric power densities. An Outlook in possible future Power Electronic Applications for the More and All Electric Aircraft will be given.

Biografie

2006-2011
University of Erlangen-Nuremberg, studies of Mechatronic with focus on Power electronics and Electric
Drivetrains

2012-06/2017
Scientific Engineer at Fraunhofer Institute for Integrated Systems and Device Technology IISB, Group Drives and Mechatronics,
Responsible for System Design of Automotive Power Electronic Systems with focus on System-Integration and SiC Drive Inverters

07/2017-now
Groupleader of the Workgroup Aviation Electronics
Focus is to transfer Technologies from Automotive Applications to provide Power Electronic Systems of highest Power Densities for future Aviation Applications like More and All Electric Aircrafts

GaN for a new compact power converter generation

T. Bouchet
Power Electronic Marketing Strategic Manager
CEA LETI, DCOS, grenoble, France

Abstract
Main goal for the next generation of Power converter is miniaturization in order to improve system efficiency at lower cost. Increasing reliability, operation safety and high working temperature (> 300°C) is also expected by end-users. To reach this target, we need to increase the power converter frequency that lead to a reduction of passive devices and contribute to the power converter miniaturization. For low power and medium power applications, GaN/Si technology is the best candidate if we think it at system level. In fact GaN devices allow high frequency capability (>MHz), high current density (at least 10 time higher than silicon) and new integrated functionality (lateral device) at lower cost as technology is CMOS compatible (8 inches GaN epitaxy on a silicon substrate). Power electronics is a key strategic activity of CEA Tech (French CEA institute). CEA TECH value proposition is a complete chain from design to system integration and optimization of Power converter. Our 5 years Power GaN Road map driven by the frequency increase focus on 6 main technological axes: epitaxy, GaN/Si active devices ,HF passive devices, 3D co-integration, GAN IC and new system topologies. 3 main Milestones related to main technology shift are presented to reach in 5 years the System on Chip approach (SOC).

Biografie
Thierry Bouchet earned his PhD in Electrical Engineering in 2001 and went to work for IBS (Ion Beam Services) and then for Atmel, two semiconductor companies. In 2011, Thierry created a fabless start-up (ADIS) in the area of power electronics.
Thierry joined Leti end of 2014 and worked on developing of GaN components before becoming Strategic Marketing manager for energy and power electronics.

1000 V/80 W auxiliary power supply as a demonstration vehicle for Wide Bandgap power electronics system design

X. Wu
Sr Application Engineer
ON-Semiconductors, Application Engineering EU,
Munich, Germany

Abstract
With the emergence of Wide Bandgap (WBG) semiconductors, power electronics are experiencing a renaissance. Many design limitations, such as switching frequency, thermal ruggedness and voltage capability of silicon based power devices are being pushed to new limits with Silicon Carbide (SiC) and Gallium Nitride (GaN) based electronics.
In order to truly make use of this extended operation range, traditional topologies have to be re-imagined. To switch at higher frequencies, for example, new passives are required; using the extended thermal operation point needs a redesign of the cooling and layout of the PCB, this could lead to extensive saving of material costs. The improved switching efficiency, and reduced die footprint, despite blocking voltage capabilities beyond 1200 V, in combination with ultra-low inductive PCB design can greatly improve switching losses.
This paper presents the approach and design considerations needed to turn traditional topologies, such as a quasi-resonant flyback, into WBG optimized systems which can make use of the various added benefits provided by current prototype of ON Semiconductors SiC power MOSFET. The investigations start with a comparison of SiC based power transistors to best in class available 1700 V Silicon MOSFETs, within a non WBG optimized system. Applying a new generation of ON Semiconductor gate drivers, in combination with partnered passives developers we demonstrate how switching frequencies beyond 300 kHz are realizable in high power applications, when using a WBG optimized design and SiC power MOSFETs. To finish the work a functioning demonstrator for a variable range quasi-resonant flyback based on 1700 V SiC MOSFETs is shown and characterized.

Biografie
Bachelor degree of Electrical Engineering and Automation, study in Harbin Institute of Technology university (CN) 2001 – 2005; PSU hardware designer in AcBel Polytech, Hangzhou 2005–2009; PSU hardware designer in Efore (CN & Sweden), 2009- 2011; Senior Simulation Engineer in Grundfos(CN)2011- 2014;
Application Engineer in Fairchild &ON Semi(DE)2015-present

Si vs SiC Power modules in HEV intergration: a cost analysis

E. Barbarini
Senior Cost Engineer
System Plus Consulting, Nantes, France

Abstract
When converting an existing petrol vehicle to a hybrid version, the available space in the engine compartment is often so limited that it is difficult to accommodate a PCU.
Thus it is necessary that the PCU has a higher power density and a smaller size.
To achieve both of these targets, manufacturers have developed different solution for the powers modules of the PCU. Some innovations are on the die point of view such as redesign IGBT structure to decrease the die size (Infineon) and others are on packaging, like eliminates the wire bonding and uses a double-side cooling structure.

These innovations lead to a redesign of the breakdown cost of the modules. The cost of Silicon devices is continuously decreasing until it will reach its lower limit while the new innovations in terms of packaging materials and method shows an increase of the cost of backend.

At the same time, the introduction of WBG materials, such as SiC, offers the possibility to decrease die size while increasing the power density and this is effective for PCU downsizing. However, the new wide-band gap devices still present some technical and economical limitations. The higher breakdown field strength of SiC places greater demands on the package insulation system and the market size of wide band-gap power device is still quite small because of the device cost.

The objective of the presentation is to define which are the cost drivers of the new technologies in Hybrid Electric Vehicles and understand if on the long term SiC devices will substitute Si devices for technical and economic reasons.

Different devices have been opened and analyzed to understand the technology innovations applied in HEV PCU’s inverters and IGBT power modules and a breakdown cost analysis of the manufacturing process has been developed.

Finally, a study of the economic impact of replacement of IGBT with SiC devices in the most innovative automotive PCU’s inverter has been performed.

Biografie
After a bachelor’s degree in Electronic Engineer from Politecnico di Torino, Elena obtained a master's degree in Nanotechnologies for the ICT and a PhD in Electronic Devices at Vishay Semiconductors.
After different experience in research and manufacturing of electronics components, she is actually Activity Leader for Power Electronics and Semiconductor Compounds at System Plus Consulting where she is managing and developing costing models and analyses of power devices.

200mm/8-inch GaN-on-Si CMOS compatible manufacturing technology

D. Marcon
Business Development Manager
imec, Leuven, Belgium

Abstract
Wideband gap technologies (SiC and GaN) are the most promising candidates for performance beyond the Si limits. In particular, GaN combines high performance with a low cost technology thanks to the fact that GaN can be grown on 200 mm/8-inch cheap Si(111) substrates (GaN-on-Si) that can be processed in a high productivity CMOS fab. Imec is world-first to show a normally-off/enhancement mode (e-mode) device technology on 200mm/8-inch GaN-on-Si wafers, which simultaneously achieves a very low dynamic Ron dispersion (below 20%) and state-of-the-art performance and reproducibility. This technology is ready for prototyping, customized low-volume production and technology transfer.

In this talk, we analyze the challenges related to the manufacturing of 200 mm/8-inch GaN-on-Si wafers in a CMOS fab. Firstly, we describe the inherent challenges related to the growth of GaN layers on Si substrates and show our latest results on GaN-based epi-buffers. Secondly, we discuss and show our latest results of imec's 200mm/8-inch GaN-on-Si e-mode device technology for 200V and 650V power switching applications.

Biografie
Denis Marcon received a M.S. degree from the University of Padova in 2006. Subsequently, he received the degree of Doctor in Engineering (Ph. D.) from the Catholic University of Leuven and imec with the thesis entitled "Reliability study of power gallium nitride based transistors" in 2011.He is leading author or co-author of more than 50 journal papers or conference contributions.
Currently, he is in imec, Belgium and he is directly responsible for the partnerships with imec in the field of GaN power electronics and on dedicated development projects of Si-based device and sensors.

T. NEYER
R&D Management
On-Semiconductor SiC Development, R&D,
Munich, Germany

Biography
Dr. Thomas Neyer has received his PhD from University of Technology in Vienna and Cambridge University in 1995. He joined Siemens HL to work on mixed signal Product design and Test. Over the years Dr. Neyer transitioned to high-voltage Technologies at Siemens and Infineon

Technologies and in 2003 he was entrusted to setup Technology Centers of Competence in Malaysia and China. During the PowerFab start and ramp-up in Kulim, Malaysia in 2005, Dr Neyer was building and leading the Fab engineering and manufacturing teams. Subsequently he was appointed as EVP for R&D and Fab Operation of Grace Semiconductors in Shanghai, China - an advanced Foundry for differentiated, analog Technologies.
In 2011, Fairchild Semiconductor founded a R&D center for High Voltage Technologies in Munich and assigned Dr Neyer to spearhead the effort and coordinate all related Silicon and SiC HV development activities covering device design, modeling, application testing and High Power package development. in 2016 ON-Semiconductor bought Fairchild and confirmed Dr. Neyer as the world-wide leader of its SiC development program.

Silicon and Wide bandgap devices in power electronics

F. Udrea
Professor
Cambridge University, Engineering, Cambridge, United Kingdom

Abstract
The view that Silicon will be replaced by wide bandgap materials such as Silicon Carbide and Gallium Nitride is gradually giving way to the idea that Wide bandgap materials will in fact coexist with silicon to address a growing market in power electronics with increasingly more demanding requirements.

Silicon will remain the main material in power electronics for a long time to come. Its strength is not in performance, but in reliability, diversity, cost and smartness. The high end and specific niche markets will however embrace GaN and SiC. GaN is likely to create a larger impact in the lower power range with voltages up to 1.2 kV, while SiC will address the higher voltages (above 1.2 kV) and higher power levels. On paper Diamond is better than any other materials for power electronics and will have its chance in the future provided that there is enough investment from public funds. Its struggle now is to deal with the cost, wafer availability and availability and the lack of shallow dopants.
This presentation will address the strengths and weaknesses of the different materials and technologies and present a view of how this material will play in the power device field in the future

Biografie
Florin Udrea is a professor in semiconductor engineering and head of the High Voltage Microelectronics and Sensors Laboratory at University of Cambridge. He received his PhD degree in power devices from the University of Cambridge, Cambridge, UK, in 1995. Prof. Udrea has published over 450 papers in journals and international conferences. He is the inventor of over 100 patents and co-funded 5 companies, three in power devices and two in sensors. Two have been among the most successful trade exists as Cambridge University spin-offs. For his ‘outstanding personal contribution to British Engineering’ he has been awarded the Silver Medal from the Royal Academy of Engineering. In 2015 Prof. Florin Udrea was elected a Fellow of Royal Academy of Engineering

Silicon Carbide Power devices as enabler for highest power density and efficiency

P. Friedrichs
Senior Director SiC
Infineon Technologies AG, IFAG IPC T, Erlangen, Germany

Abstract
At all recent power semiconductor fairs and conferences the importance of SiC devices as enabling components for new levels of performance in power circuits was more than evident. Considering the commonly accepted cycles in the adoption of new technologies it is visible that after the success of the diode technology meanwhile also the MOSFETs are on the threshold of the hockey stick in adoption. The contribution will discuss the design challenge for SiC MOSFETs and how a device can be operated in order to fulfill the expectations regarding performance and robustness. Special focus will be put onto the question how to build a bridge from the today IGBT dominated world towards unipolar MOSFET based devices. Furthermore, it will be sketched which additional aspects beside the pure availability of a chip technology will be mandatory for a successful Adoption in power electronics applications. Finally, concrete examples will be presented how a new and significantly more expensive technology can bring added value to the user and the community striving for energy saving and low emission levels. A critical assessment will be made for both, automotive and industrial applications.

Biografie
Dr. Peter Friedrichs was born in 1968 in Aschersleben, Germany. After achieving his Dipl.-Ing. in microelectronics from the Technical University of Bratislava in 1993, he started a Ph.D work at the Fraunhofer Institut FhG-IIS-B in Erlangen. In 1996 he joined the Corporate Research of the Siemens AG and was involved in the development of power switching devices on SiC, mainly power MOSFETs and vertical junction FETs. He holds more than 10 patents in the field of SiC power devices and technology and was an author or co-author of more than 50 scientific publications and conference contributions in this field.
Peter Friedrichs joined SiCED GmbH & Co. KG, a company being a joint venture of Siemens and Infineon and originated from the former Siemens research group, on March the 1st, 2000. Since July 2004 he was the managing director of SiCED, responsible for all technical issues. After the integration of SiCED’s activities into Infineon he joined Infineon as Senior Director Silicon Carbide from April 1st, 2011.

Wide Bandgap Power Electronics: What Will it Take for Large Scale Adoption?

D.A. Britz
Business Development Manager
Applied Materials, Office of the CTO, Santa Clara, United States

Abstract
New materials frequently face "the chicken or the egg" problem. Until there is sufficient scale of a material's usage, there is little incentive for supply chain manufacturers to invest in unique process tools. Applied Materials will review our perspectives on barriers to adoption of wide bandgap materials for power electronics and what would be required for large scale adoption of these materials.

Biografie
David Britz is a Business Development Manager at Applied Materials in the Office of the CTO. He has held various roles in the optics, and optoelectronics industry. David received an MBA from MIT Sloan and a D.Phil. in Materials from the University of Oxford.

Energy Filter for Ion Implantation - A Novel Production Technique for SiC-Power Device Technologies

M. Rüb
Head of Strategy and R&D
mi2-factory GmbH, R&D, Jena, Germany

Abstract
mi2-factory GmbH is a high-tech start-up company from Jena (Germany) which develops, distributes and applies a so-called “Energy Filter for Ion Implantation” (EFII). This innovative tool can be beneficially used for the doping of any semiconductor material. Customers use this novel technology as a process step in the production of Silicon Carbide (SiC) power devices. EFII is a major leverage to improve the cost performance of these devices. In today´s chip production the advantages of SiC cannot be fully exploited due to the large doping inhomogeneity (at least +/-20%) [1] of the epitaxially grown drift zone, which is the core element of any vertical SiC power device such as SiC Diodes or MOSFETs. A solution to this problem is found in EFII [1]. This technology is based on ion implantation in combination with a thin, micro-patterned Si membrane which gets inserted into the ion beam. The membrane serves as a filter that enables a highly precise depth-distribution of doping atoms with a very high homogeneity (+/-1%) over the wafer surface. Furthermore, EFII can be combined with masking which allows for trench-like doping structures in SiC and may enable a real SiC-superjunction transistor. It is the only evident technology which is scalable to production volume for precise and flexible adjustment of the patterned or blanket drift-layer doping of SiC power devices. mi2-factory demonstrated the huge potential of this novel technology in a cooperation with an industrial partner in 2015 [2,3] and is now seeking to establish EFII in SiC power device production.

[1] Csato et al.: Energy filter for tailoring depth profiles in semiconductor doping application, Nucl. Instr. Meth. B (2015), Volume 365, Part A, 15 December 2015, Pages 182–186
[2] Rupp et al.: Alternative highly homogeneous drift layer doping for 650V SiC devices, ICSCRM 2015
[3] Rupp et al.: How to further improve the market penetration of SiC power devices?, ECSCRM 2016

Biografie
since 2016 Co-founder of mi2-factory GmbH, Jena
Head of Strategy and R&D

since 2008 Professor for Microtechnology at
University of Applied Sciences Jena

1997-2008 Infineon Technologies Austria AG
Power Device Technology Development

1997 PhD. from Friedrich-Schiller University, Jena

1993 Physics Diploma degree from
Friedrich-Alexander-University Erlangen-
Nuremberg

GaN High Electron Mobility Transistor (HEMT) defect inspection by high resolution quantitative cathodoluminescence

S. Sonderegger
CEO
Attolight AG, Lausanne, Switzerland

Abstract
Gallium nitride based high-electron mobility transistors (HEMTs) face an increasing demand for various applications such as cellular base stations, Lidar, wireless charging and the power supply segment. Gallium nitride has a number of advantages over Silicon such as a wide direct bandgap of 3.49eV, a break down field ten times larger than that of Silicon and a good electron mobility in bulk and heterostructures. These attributes make GaN and related alloys a compelling material for HEMTs.
Nevertheless, integrating GaN based semiconductors on a silicon platform remains challenging due to a large lattice mismatch between GaN and Silicon. This mismatch yields to a high density of defects propagating through numerous layers of the device. These defects need to be analysed and understood during the research and development phase and need to be monitored and controlled during ramp up and production.

We use quantitative cathodoluminescence to analyse a cross-section of a GaN-based HEMT. High spatial resolution spectroscopic information might be acquired by exploiting cathodoluminescence combined SEM. CL provides information about the electronic bandgap, variation of local concentrations of elements, strain and defect states in semiconductor heterostructures and insulators at the nanometer scale.

We gain a direct insight into the presence of defects within the insulating C-doped GaN layer, and the homogeneity of thin AlGaN layers of varying Al content, emitting CL signal in the deep UV range. CL imaging clearly highlights the presence of defects across the insulating C-GaN, as well as highly localized CL emission from AlGaN layers. Further spectral processing allows characterization of local strain between layers with varied Al stoichiometry, determination of bandgap evolution, as well as characterization of Al content in each layer within 1% precision.

Biografie
Samuel studied at EPFL (Swiss Federal Institute of Technology, Lausanne) and Ecole Normale Supérieure de Lyon (France) and obtained a MS of Physics from EPFL. His master thesis on the optical properties of semiconductors was conducted at the Ioffe Physico-Technical Institute (Russia). During his PhD at EPFL, he further developed Attolight's ultrafast cathodoluminescence technology and used this technique to advance the understanding of optical properties of nitride based semiconductors. Samuel decided to jump into the entrepreneurial world after his PhD thesis and co-founded Attolight with Jean Berney. Since then he has headed the business development of the company with a strong focus on developing industrial applications of cathodoluminescence.

Advanced Cu Plating Technology for High Performance Power Devices

K. Suguro
Project Manager and Chief Reasearch Scientist for Advanced Process Development
Toshiba Corporation, Ishikawa, Japan

Abstract
The strong requirements for advanced power devices are lower ON resistance (RON) and more reliability for Ids-Vds characteristics as compared with current power devices. Cu metallization can satisfy both requirements due to lower electric resistivity, higher thermal conductivity and higher yield strength.
In order to obtain better power device performance, it is necessary to plate 10-50 micron on semiconductor substrates. Among Cu film formation methods, newly developed Cu plating is most promising due to lower process cost and higher productivity in mass production. Cu films of 10 micron to 50 micron in thickness can reduce 15% to 40% of the temperature rise of transisters at the timing of high electric current is passed in power devices. However, thicker Cu films cause larger wafer warpage. Therefore, Cu film stress is required to be reduced while keeping lower resistivity of the Cu film. In our study the Cu film stress was successfully reduced to 10MPa or below. Double side Cu plating is more effective to minimize the Si wafer warpage and very thin Si membrane wafer can be successfully metallized with Cu films by controlling Cu thicknesses of frontside and backside by using simultaneously plating (multiplating Cu). In this paper a new Cu plating process and the advantage of Cu plating for power devices are discussed.

Biografie
Dr. Kyoichi Suguro, Chief Research Scientist and Project Leader, Advanced Discrete Development Center, Toshiba Corporation Storage and Electronic Devices Solutions Company, Japan

J. Mai
Managing Director
JEM Europe, Montbonnot, France

Biography
Joe Mai is managing director of JEM Europe, a global leader in wafer-probing technologies. He has been with JEM for over 20 years, playing both technical and business-development roles in the US, Europe and Asia. For more than two decades, he has worked closely with customers around the world to improve their test capabilities and to develop JEM’s technologies.

Wide Bandgap Materials Parametric Test Challenges

C.S. Wilson
Business Manager
Keysight Technologies, Marketing, Edinburgh,
United Kingdom

Abstract
Wide Bandgap Materials Parametric Test Challenges

Stewart Wilson, EMEAI Business Manager at Keysight Technologies

ABSTRACT:
The adoption of new wide bandgap materials such as GaN and SiC has resulted in new Parametric, (Electrical) Test challenges in both device measurement and modelling. These new materials devices are now being manufactured in ever increasing volumes and are quickly becoming mainstream.

This paper discusses how Keysight Technologies extended the measurement range of a standard 4080 series Parametric Test system to 3kV. It considers several of the key challenges which include: operator safety, test system security, probe card design and prober safety and chuck requirements.

Biografie
Dr Charles Stewart Wilson Biography

Stewart Wilson is currently the European Business Manager for Keysight Technologies range of Parametric Test Equipment.
He holds both BSc and PhD degrees in Electronics and Electrical Engineering from the University of Glasgow, Scotland (UK).

Dr Wilson has worked in the field of Semiconductors since 1979. During this time he has worked for several semiconductor manufacturers including Motorola and National Semiconductor. In addition he has worked for Semiconductor equipment manufacturers / suppliers; Eaton Corporation and Hewlett Packard / Agilent Technologies / Keysight Technologies in both Europe and the United States.
Dr Wilson has been employed by Hewlett Packard / Agilent Technologies / Keysight Technologies since 1985 and has held a number of sales and marketing positions. He is currently the European Business Manager for Keysight Technologies range of Parametric Test Equipment.

Addressing challenges testing complex power analog semiconductors

T. Dirscherl
Product Manager Power and Analog
Advantest Europe GmbH, Amerang, Germany

Abstract
Innovation and permanent cost reduction measures are driving steady rising semiconductor content.
At the same time the pin count stays almost constant and therefore drives the need for complex device I/O structures. Various test requirements from analog/power to digital are observed behind such pins which drive the demand for a flexible ATE resource.
High power devices require a careful thermal management to achieve a high measurement stability.
An exact defined and repeatable energy delivery of the ATE High Power VI Sources to the DUT is essential. In addition, the power IC market presumes a significant higher mix of devices compared to prevailing digital centric segments. To test such a diversity of products a universal test system architecture is of benefit.
A major contributor for saving test cost is to increase the number of test sites. As a consequence, there is a need for additional load board circuitry. Moreover, complex power multiplexing schemes are getting introduced due to resource sharing. With rising site counts a high multisite efficiency (MSE) becomes a key element for throughput optimization. A method to increase ATE efficiency is the parallel execution of test sequences on the ATE hardware, rather than constant interaction between the instrumentation and a workstation CPU.

The solution for above challenges is addressed by a universal ATE pin architecture with synchronized pattern based execution for maximum throughput and repeatable setups and measurements.
Powerful software tooling supports the capability of complex routing and multiplexing schemes which are seamless integrated into the main test flow.

Biografie
Toni Dirscherl holds a degree as Electronic Engineer from the University of Applied Science in Munich, Germany and joined SZ Testsysteme as Development Engineer for Analog DSP frontends in 1997. After serving 3 years as Senior Application Engineer for SZ Inc and Credence

in San Jose/California from 2001 to 2003, Toni Dirscherl took over the position as Product Marketing Engineer for Credence-SZ GmbH. Since the acquisition of Credence-SZ by Advantest Europe in 2008, Toni Dirscherl acts as the Product Manager for Advantest’s Analog and Power Solutions. He has published numerous articles.

Contact resistance in pulse conditions

F. Barbon
Development Engineer
Infineon Technologies AG, Neubiberg, Germany

Abstract
The contact resistance tool (CRes) is a laboratory instrument internally developed used for the measurement of the contact resistance which occurs between the probe contact needle, and the contact surface of the device under test. This parameter is very important and has a big impact on semiconductor test yield, because it influences the signal integrity.
The instrument received a hardware upgraded, with a new generator which delivers controlled higher current impulses.
The evaluation of the contact resistance with high current impulses will enable to evaluate the current carrying capability (CCC) on various combination of needles vs pads material, under real-life needle operative conditions.
The new tool and some initial results will be presented.

Biografie
Francesco Barbon in 2011 obtained his Master of Science in Telecommunications at the Department for Electronics and Informatics of the "Università degli Studi di Padova". In 2014, he terminates his contact as Researcher at the Institute for Electronics Engineering of the University Erlangen-Nuremberg, developing new power detector concept for Six-Port interferometers.
At present, he is working at Infineon AG as Development Engineer in the field Test, Technology, and Innovation. His focus is description, verification, and qualification of Probecards used in production for mixed, and analog signals in microwave region.

C. Melvin
Global Product Manager, Semiconductor Advanced Packaging
Atotech Deutschland GmbH, Berlin, Germany

Biography
Cassandra Melvin received her BS in Business Management and Neuropsychology at Rensselaer Polytechnic Institute and is Global Product Manager for Advanced Packaging at Atotech Deutschland GmbH. She is responsible for a rather extensive product portfolio that includes processes for both electrolytic and electroless plating of copper, nickel, tin, palladium, gold,

and indium in advanced packaging applications.

Prior to joining the Atotech team, she held the position of Business Manager at the SUNY Polytechnic Institute *(formerly the College of Nanoscale Science and Engineering)* focusing on Technical Programs for semiconductor chemistry and equipment.

Cassandra has had numerous articles published in leading technical magazines and her work has been presented at key conferences globally. She is a member of the SEMI Materials and Power Electronics Committees.

Additionally, she currently serves as Deputy Country Director, Germany for the Digital Leadership Institute, an international NGO whose global mission is to promote digital inclusion for women.

Direct electroless under bump metallization (UBM) for wire bonding and soldering on next generation power semiconductor materials

A. Walter
Team Manager Electroless Processes
Atotech Deutschland GmbH, Semiconductor Advanced Packaging, Berlin, Germany

Abstract
Direct electroless under bump metallization (UBM) for wire bonding and soldering on next generation power semiconductor materials

The presentation will show benefits and feasibility results for electroless plating direct on GaAs, GaN, SiC for next generation packaging in growing power electronics industry.
Compared to Si and Ge, these wide band gap materials allow the design of smaller and faster power components with higher reliability and more efficiency. Furthermore, they enable operations at higher temperature, voltage and frequencies, which is necessary for many power applications.

Although these materials already gaining more acceptance for new markets, they face some challenges, such as new packaging and design technologies, to become more cost efficient. One solution is to reduce packaging process steps by direct UBM on semiconductor material prior to soldering and wire bonding, which makes sputtering of Al and Cu pads obsolete. Further advantages are 1) higher throughput due to batch and double side processing, 2) self-aligned deposition without patterning and 3) reduced power losses due to low voltage ohmic metal-semiconductor contact after annealing.
We will present our proven results that it is possible to deposit electroless Ni on GaAs or Si with different types and levels of dopings. In addition, we will show the feasibility of direct electroless plating on next generation power semiconductor materials, such as SiC, Ge and GaN.

Biografie
Andreas Walter has more than 18 years’ experience in semiconductor industry and is currently working as head of application for electroless plating processes for Semiconductor Advanced Packaging at Atotech. Before he joined Atotech in 2009 he worked 3 years as an Senior Engineer at Qimonda for process integration for new memory systems and 7 years as a Development Engineer at Infineon, where he was responsible for material development and process integration in 300 and 200mm fab for D-RAM and resistive memories. Andreas received his Diploma and PhD in chemistry at the Martin Luther University in Halle, where he started as a scientist for synthesis of OLED dyes and organic semiconductors

Embedding for Power Application and Fan-out Packaging at Panel Level

H. Stahr
Groupmanager Technology
AT&S, R&D, Leoben, Austria

Abstract
Embedding is without any doubt the key driver for advanced packaging. This has been shown over the last years. Miniaturization is the general unbroken trend in electronics and it looks for a big variety of technical solutions coming from the different main streams of packaging. A new hype was pushed up when TSMC showed their new fan out package solution for the A10 processor in Apple's iPhone 7. The whole supply chain has reacted by developing materials, equipment and methodologies to support fan-out packaging to catch a piece of this attractive cake.
In this field of expectation Fraunhofer IZM has built a consortium for panel level packaging with a focus on panel level molding. This consortium in the meantime has 16 members which are material suppliers, process and machine suppliers, PCB and substrate makers and a big silicon house. In this presentation the latest developments of this consortium and further interesting project results from IZM will be reported.
Power application is another field for embedding technologies starting with DC-DC low power converters years ago in AT&S. New concepts with low thermal resistance and low inductance are developed and the industrialization was started. These concepts have been developed in the frame of the Catrene project EmPower which ended this year. The performance of these concepts and power applications will be shown in this presentation furthermore there is a view on the market potential for embedded power application.

Authors :
Andreas Ostmann , IZM
Hannes Stahr , AT&S

Biografie
Hannes Stahr
• He studied electronics and telecommunication engineering at the University in Graz and received his diploma in 1988
• He works as a group manager technology in the R&D of AT&S and was deeply involved in the most recent developments for HDI PCB
• Since 1997 his focus area is component embedding in PCB staring with printed passive components
• In 2008 he guided the FP7 project Hermes to success which resulted in the industrialization of the chip embedding technology und later to the foundation of the business unit Advanced Packaging in AT&S
• The Catrene project EmPower was started in 2013 focusing on the development of embedded power modules and power packages using new embedding and power module concepts. He is the consortium leader of EmPower and will report in his speech about the progress.
• He is author and co-author in 21 filed patent families for PCB and advanced packaging

How technology development will shape the power electronics market in the next 5 years

M. Rosina
Senior Analyst, Energy Conversion and Emerging Materials
Yole Développement, Power Electronics and Compound Semiconductors, Villeurbanne (Lyon), France

Abstract
The power electronics represents a healthy market driven mainly by the CO2 emission reduction targets. In 2016, the power device market was worth $16B and it will grow steadily for the next five years.
Within this presentation, Yole Développement will highlight the latest material and technology trends and the impact they will have on the power electronics supply chain.
The needs for lower CO2 emissions have led power electronic industry to develop more efficient and smaller solutions. Increased power density results in strong technology challenges calling for innovations on different levels: semiconductor material, packaging materials, device design… Several new power device designs have emerged in the last years, principally driven by the severely challenging requirements for high power density and integration from the electric and hybrid electric vehicles (EV/HEV). The high manufacturing volumes observed in automotive industry help and accelerate the implementation of these new technologies.
All these technology trends are creating opportunities for some material suppliers, but at the same time, they are threatening some of today's businesses for power electronics. In recent years, we have seen consolidation among power semiconductor market leaders with several acquisitions, such as Infineon buying International Rectifier and ON Semiconductor buying Fairchild. These moves were intended to strengthen positions in the overall power semiconductor business. Nevertheless, in coming years the market leaders will face strong competition from Tier-1 automotive manufacturers and new entrants from China. Outsourced Semiconductor Assembly and Test companies (OSATs) could also propose services to provide advanced packaging technologies to power device manufacturers. This will define a new business model that diverges from the traditional power device supplier business.

Biografie
Dr. Milan Rosina is a Senior Analyst for Energy Conversion and Emerging Materials at Yole Développement. Dr. Rosina has more than 15 years of scientific and industrial experience with prominent research institutions, an equipment maker, and a utility company. His expertise includes new equipment and process development, due diligence, technology, and market surveys in in the fields of power electronics, renewable energies, energy storage, batteries, and innovative materials and devices.

Trends in Passives for Power Electronics

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Abstract
The capability of a power electronic system is strongly influenced by its passive components. In this regard, the passives should offer a maximum level of operating temperature, switching frequency, electrical field and current, and robustness. This calls for new materials and technologies, innovative product designs, and an increased level of component integration. Passive components that fulfill these requirements enable new possibilities for power electronic systems and are therefore called ‘More-than-Moore Passives’.
In this presentation we review the specific requirements on passive components used for power electronics. We outline some of the current physical and practical limitations of passives, and present some examples how these constraints can be overcome. Emphasis is placed on new materials for improving the high temperature and high frequency characteristics of capacitors and inductors. Also some examples of system integration of passives are given.

Biografie
Dr. Georg Kuegerl earned his PhD in Physics at the Graz University of Technology (TU Graz) in Graz, Austria. In 1992 he joined Siemens Components, which in the meantime is a part of TDK Corporation. He is now the Chief Technology Officer of TDK's Piezo and Protection Devices Business Group, and is also Head of the TDK European R&D Center.

Investing to Boost Power Electronics From Materials to Systems - Opportunities and Challenges

A.Z. Zhou
Managing Partner
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Abstract
Over the last 30 years, the semiconductor industry has been driven by rapid growing in demand for CPUs and Memories by personal computers and communications products at a speed and cost predicted by the Moore's law. As Moore’s law approaching its limit, more attention and resources are devoted in developing new devices and new materials including compound semiconductors such as GaN and SiC. These third generation WBG semiconductor materials are ideal for power electronics.

As the world’s first Billion dollar fund dedicated to invest in compound semiconductors and build-up the eco-system globally. We have explored investment opportunities and challenges in many companies from start-ups to conglomerates around the world. These companies are developing new power semiconductor materials and devices, advanced power switching techniques, power control and monitoring technologies, power conversion&storage innovations, and adaptive power optimization algorithms, variable motor drives, green technologies for power generation, conversion and distribution, new internet and “sharing economy” business model in power, smart connected grid,etc. Of course, solution size, efficiency, and cost are well-established metrics for power technology advances and trends for these metrics are discussed.

In summary, this talk examines the state of compound semiconductor power technology from an investor perspectives, including materials, devices, and systems; and share our vision for how the world of power electronics may evolve over the coming years and where we are investing to build up and accelerate the adoption and mass manufacturing of new materials, devices, and technologies in power electronics for applications in consumer electronics and mobile devices today as well as Electric Vehicles in the near future.

Biografie
Alan Zhen Zhou is the Managing Partner at An Xin Capital focusing on compound semiconductor ecosystem investments from material, equipment, process, device, to systems. Dr.Zhou has over twenty years of semiconductor experiences where he held both technical and management executive positions at IBM, AT&T, Lucent, Agere Systems and Qualcomm. He also founded and co-founded several companies, including CSMC (IPO in Hongkong), MEMSIC (IPO in NASDAQ), Top Global (acquired), Belleds and Bellnet Technologies.

As vice president at Qualcomm, Alan was responsible for all Qualcomm chipset business and design wins in China where he managed Sales, Operations, Customer Services and Field

Applications Engineering functions. His team delivered >$3B revenue and >150M units of smart phone chipsets per year to over 50 major OEMs. While working for Lucent and AT&T, he established the first communications IC design center and launched the first GSM handset reference design to a dozen leading communications and consumer electronics companies in China. He also built the first submicron IC foundry in China (now China Resources) with technologies transferred from AT&T Bell Labs.

Dr.Zhou received both of his MS and Ph.D. degrees in Electrical Engineering and Computer Science from MIT with his BS degree in EE from NYU-Poly.