Advanced Packaging Conference

Welcome Remarks

L. Altimime
President
SEMI Europe, Berlin, Germany

Abstract
Coming Soon

Biography
Laith Altimime, as President of SEMI Europe, leads SEMI's activities in Europe and the Middle East and Africa (EMEA). Altimime has P&L responsibility as well as ownership of all Europe region programs and events, including SEMICON Europa. He is responsible for establishing industry standards, advocacy, community development, expositions, and programs. He provides support and services to SEMI members worldwide that have supply chain interests in Europe. He manages and nurtures relationships with SEMI members in the region and globally as well as with local associations and constituents in industry, government, and academia. Altimime has more than 30 years of international experience in the semiconductor industry. Prior to joining SEMI in 2015, He held senior leadership positions at NEC, KLA-Tencor, Infineon, Qimonda and imec. Altimime holds an MSc from Heriot-Watt University, Scotland.

References

Elevating Power Efficiencies Through Advanced Packaging Innovation

M. Gerber
Senior Director, Engineering, Marketing & Technical Promotion
ASE, Texas, United States of America

Abstract
Coming Soon

Biography
Mark is Senior Director Engineering, Marketing & Technical Promotion at ASE, and provides technical support for customer activities focused around Flip Chip, Interconnect, and SiP Packaging Technologies, within 5G, AI, Mobile, Automotive and IoT.
With over 25 years of semiconductor packaging experience, Mark previously worked at Texas Instruments, Motorola SPS, and Dallas Semiconductor in various areas of manufacturing, assembly and testing of electronics components and systems, with an emphasis on new product introductions (NPIs) and the development of new technologies and processes. Mark holds a Bachelor's degree in Mechanical Engineering from Texas A&M University, has written 25+ papers and holds over 32 semiconductor packaging patents.

References

Deep Pitch Scaling of Wafer-to-Wafer and Die-to-Wafer Cu/SiCN Hybrid Bonding

A. Jourdain
R&D Manager
Imec, Pathfinding Integration, Leuven, Belgium

Abstract
Hybrid bonding is recognized as the key technology for advanced heterogeneous wafer-level system integration. This is enabled through aggressive pad size and 3D interconnect pitch scaling, resulting in minimal electrical die-to-die interconnect delay. In this presentation we will discuss the properties of SiCN dielectrics as material of choice for hybrid bonding, as well as the process requirements for the mixed Cu/SiCN surface finish of wafers. The physical mechanisms of hybrid bonding will be discussed. The various improvements in wafer processing and wafer alignment and bonding will be discussed, resulting in high yield hybrid bonding down to 400nm interconnect pitch. When applying this hybrid bonding technology to die-to-wafer, additional challenges need to be addressed. Particularly challenging is maintaining the quality and cleanliness of the Cu/SiCN surface through die thinning, singulation and individual die pick & place operations. We discuss a process flow to enable the mitigation of these challenges, demonstrating 2 µm pitch die-to-wafer hybrid bonding.

Biography
Anne Jourdain received her PhD degree in Physics from University Joseph Fourier of Grenoble, France, in 1998. In 1999, she joined IMEC (Interuniversity Microelectronics Center) in Leuven, Belgium, to work on wafer-level-packaging solutions for RF-MEMS applications. In 2007, she joined the 3D Integration Research Program of IMEC to work on various wafer-to-wafer bonding and wafer thinning technologies. In 2019, she became responsible for the Backside Power Delivery Network integration activities within the program before taking the lead of the 3D Heterogeneous Integration team in 2022, looking at collective die-to-wafer and direct hybrid bonding technologies for 3D stacking applications. She is currently leading the Heterogeneous Integration and Packaging Development Group.

References

Meeting the Demands of Future Computing with Chiplets and Advanced Packaging

J. Sexton
IBM Fellow, Future Computing Systems
IBM, IBM Research Europe, Dublin, Dublin, Ireland

Abstract
The era of generative AI fundamentally fundamentally has changed how computing is designed and deployed. It is clear that future computing will be characterized by an unprecedented increase in compute, memory, and bandwidth requirements of all workloads. Chiplet architectures and advanced packaging offer an exciting path to meeting these demands through much more tightly integrated compute and memory units, enabling higher compute densities and bandwidths with lower latency and power. Heterogeneous integration coupled with open interface standards can also enable targeted architectures to accelerate specific use cases through co-packaging of diverse chiplets from different sources. We will discuss the challenges that are arising for future computing and the opportunity that is provided by chiplet based design to address those challenges.

Biography
Dr. James Sexton is an IBM Fellow, Future Computing Systems, at IBM Research Europe. Dr. Sexton received his Ph.D. in Theoretical Physics from Columbia University, NY. His areas of interest lie in Advanced Computing, Computational Science, Applied Mathematics and Analytics. Prior to joining IBM, Dr. Sexton held appointments as Lecturer then Professor at Trinity College Dublin, as postdoctoral fellow at IBM T. J. Watson Research Center, at the Institute for Advanced Study at Princeton and at Fermi National Accelerator Laboratory.

References

Advanced Electrolytes Meeting Future Requirements in Microbump Technology

J. Stubbe
Global Application Manager
MKS Instruments / Atotech, Semiconductor,
Berlin, Germany

Abstract
In this study, we investigate the challenges and advancements associated with meeting emerging bump requirements in advanced packaging technologies through optimized Electrochemical Deposition (ECD) plating processes. Tracing the historical evolution from Flip Chip to 3-D stacking, the industry's demand for smaller bump sizes and pitches is emphasized. We address the complexities of ECD Cu, Ni(-alloy), and Tin(-alloy) processes, focusing on microbump development and evaluating NiFe alloy as a superior diffusion barrier. The study concludes by highlighting empirical results, offering experimental solutions for miniaturization challenges in advanced packaging, with a particular focus on the promising performance of NiFe as a barrier material.

Biography
Jessica Stubbe studied chemistry in Berlin, where she earned her PhD in coordination chemistry with a focus on electrochemistry. Her career began at Atotech as a scientist in the semiconductor department. Through hard work and dedication, she advanced to lead the electrochemical deposition team in the semiconductor division, overseeing application processes and ensuring optimal performance in their projects.

References

Challenges of new chiplet integration – how organic interposers challenge BEOL equipment

E. Brandl
Business Development Manager
EVG, St. Florian am Inn, Austria

Abstract
The innovations of chiplet integrations took interesting turns in the last few years as this platform promises high performance application system at low-cost and faster-to market solution in comparison to SoC integration. Several approaches for the modular chiplet implementation have been introduced, where performance requirements, cost considerations and scalability need differ. Although the chiplet integration on Si interposers is a very important technology, a trend towards the utilization of organic materials, for example in high density build up organic substrates can be observed.
As in all advanced packaging technologies, form factor is crucial. Temporary bonding offers support for organic interposers during thinning to reduce the formfactor in z-direction and allow for better heat management as these organic interposers have limited heat dissipation capability.
Already established chiplet packaging technologies like chip-first or RDL first FoWLP are still facing the manufacturing challenge of high warped wafers originating in the CTE difference of chiplets and mold. This challenge is also valid for high density build up organic substrates and needs to be addressed. There are two major approaches for handling high warpage wafers. Either the wafers are forced flat, which works with thinner, flexible organic wafers or the equipment must comply with the wafer warpage. The later approach is used with thick and stiff wafers and is linked to a higher process complexity.
We will show the manufacturing considerations of each warpage handling approach with their advantages and challenges in respect to the temporary bonding, debonding and further downstream processes with process and equipment compatibility.
In this presentation, we will also give a short overview on the different chiplet integration platforms with their advantages and challenges. In more detail the integration of organic materials as in RDL/ organic interposers will be shown and the equipment challenges, especially wafer warpage in temporary bonding and debonding equipment and possible solutions will be introduced.

Biography
Elisabeth Brandl is business development manager at EV Group for temporary bonding and metrology. She holds a Master degree (DI) in technical physics from the Johannes Kepler University Linz specialized on nanoscience and - technology.
Since 10 years she works at EVG and was, amongst other topics responsible for the UV laser debonding launch. She published several articles and papers in the field of temporary bonding and metrology.

References

Power and Thermal Management in Advanced Chiplet-Based Packaging

Y. Kweon
Sr Director of Chiplets FCBGA Development
Amkor Technology Inc, Chiplets FCBGA BU,
Tempe, United States of America

Abstract
Chiplet-based packaging has several benefits, such as yield enhancement through logic die partitioning, system form factor reduction, and on-time to market through heterogeneous integration. However, chiplet-based packaging requires an optimized interconnection among semiconductor device dies for high bandwidth, low latency, and low power in the small form factor as advanced chiplet-based packaging. Thus, there are several challenges, such as PDN (Power Distribution Network) optimization, TDP (Thermal Dissipation Path) creation, and thermal stress minimization in the complexed chiplet-based heterogeneous integration. To solve these challenges, it needs to consider power delivery optimization while managing thermal dissipation.
Amkor can support an efficient thermal dissipated chiplet-based packaging solution to succeed customers business. As known, semiconductor IC (Intergrated Circuits) power densities are still increasing yearly; moving to high performance colling systems, such as boiling liquid carries away heat generated by computer servers. Based on this kind of advanced cooling method at Data Center, packaging thermal resistance portion of Θ_{JA} is increased. Thus, it is important to make a better thermal performed FCBGA packages with TIM (Thermal Interfacial Materials) of Data Center application, and advanced chiplet-based packaging requires higher thermal dissipation performance continuously. For example, polymer TIMs have a limit to perform a low Θ_{JC} on the thermal dissipation requirement because of a higher interfacial thermal resistance as TIM I. Therefore, advanced chiplet-based heterogeneous integrated FCBGA with Indium alloy TIM is one of solution because there are many positive customers experimental data. This means that Indium alloy TIM as TIM I could provide 2x longer semiconductor device lifetime relatively. In addition, a molded FCBGA can support to create a new thermal dissipation path and to reduce semiconductor device ILD (Interlayer Dielectric) thermal stress for advanced 2.5D and 3D chiplet-based heterogeneous integrated packages.

Biography
Mr. YoungDo Kweon is currently working for Amkor Technology HQ in USA as R&D program manager. He has been working in development of several packages and assembly new platforms since 1988. Recently, he is focusing on higher thermal dissipation solutions of advanced chiplet-based heterogeneous integrated FCBGA packaging.
Mr. Kweon received BS degree in Metallurgical Engineering from Hanyang University in 1987, MS in Semiconductor Engineering from Samsung Semiconductor Technology Institute in 1995, and MS with CALCE Electronics Package Research Center in Mechanical Engineering from University of Maryland at College Park in 1998. He has held several patents and published papers.

References

Challenges in Advanced Packaging for High Performance Computing

C. Yang
Corporate Fellow
STATS ChipPAC, Technology Office, Singapore, Singapore

Abstract
With ever growing demands of AI and cloud applications, advanced packaging especially 2.5D/3D with chiplet integration, becomes a major technology path to meet the increasing demands of computing power. Power delivery and thermal management are two crucial roadblocks in various scenarios, e.g. when large size xPU power can reach thousand watts, liquid cooling and high efficiency power modules at both board and package level become prerequisites for the system to work properly. Package and silicon power delivery solutions, e.g. silicon capacitors (including DTC, MIM etc.), integrated VR etc. add process complexities and cost but are necessary to make the advanced node IC work properly. Further integration in both board and package level can been foreseen, e.g. 48V package integrated VR to meet future demands. On the other side, the thermal management (basically all power delivered to computing ICs will be dissipated as heat) becomes very challenging, advanced package and system level cooling methods are needed. Thermal interface material is a major concern at many cases where advanced TIM becomes a very hot topics in the industry. Heat induced reliability (silicon, package) is also a critical job for the packaging industry. Key trends observed and a few cases will be discussed.

Biography
Dr. Yang is currently corporate fellow for JCET STATS ChipPAC. He has more than 20 years'experience in electronics system and IC packaging development. At present he is leading corporate technology office at JCET STATS ChipPAC. Before joining JCET, he was at Flex on SiP products and technology development in IoT, automotive, medical, and industrial applications, covering design, manufacturing, and testing areas. He has worked at Intel on memory packaging design and technology development for 13 years. Dr. Yang hold a Ph.D. degree from National University of Singapore, EMBA from Washington University in St. Louis, and Master and Bachelor from Shanghai Jiaotong University.

References

Half-bridge GaN by Fan-out Panel Level Packaging

Q. Tang
Vice General Manager
Guangdong Fenghua Semiconductor Technology Co., Ltd., Guanghzou, China, People's Republic of

Abstract
Gallium nitride (GaN) power devices have been widely used in the fields of fast charging with their high voltage and high frequency performance. However, high-power industrial applications such as motor control and inverters have still not been developed. Fan-out panel level packaging (FOPLP) is an attractive packaging technology which brings many benefits, such as low inductance, thin package height, and ease for multi-die integration. In order to give full play to the advantages of GaN power devices and expand the application of GaN in other aspects, it is important to improve the power density, reduce the parasitic inductance, and reliability of the packages.
In this paper, Silicon (Si) chips and GaN field-effect transistors (FETs) were integrated into a quad flat no lead (QFN) package. The GaN FETs and Si chips were interconnected through re-distribution layer (RDL) Cu plating process and formed a half-bridge GaN module. Chip positioning, RDL layout and warpage behavior were optimized by package stress simulation. Thermal performance of different designs was studied by finite element analysis (FEA) tools. One watt heat dissipation was applied on the GaN chip to simulate package heat performance, and balancing of the heat dissipation was optimized by RDL design. In addition, thermal stress was optimized as well based on the Von Mises stress analysis on bumping area. Warpage and package stress on chips were minimized by tuning the package structure. A suitable Cu thickness was identified with consideration of current carrying capability and heat dissipation. The reliability performances including temperature cycling and high temperature accelerated test (HAST), were evaluated based on Joint Electron Device Engineering Council (JEDEC) requirements.
By overcoming the technical challenges faced during the GaN FOPLP process, we successfully fabricated a small GaN half-bridge package with dimensions of 6mm×7mm×0.45 mm. By using only three layers of Cu RDL, the required electrical performance of the device was achieved, and the package warpage (46 micrometers) was controlled to minimize the mechanical stress. 30% of printed circuit board (PCB) area reduction was achieved by compared to the discrete package circuit layout.

Biography
Qingyuan Tang earned his Ph.D. from City University of Hong Kong, P.R. China, in 2011 in Electronic Engineering. After graduated, he worked in Sierra Wireless, Nexperia, and Facebook before for different technical positions. He is now working as a Leader in Guangdong Fenghua Semiconductor Technology Co., Ltd. for R&D management.

References

AI-Driven 3D X-Ray Inspection: A Game-Changer for Advanced Semiconductor Packages

I. Drolz
Vice President Marketing & Product Strategy
Comet, Hamburg, Germany

Abstract
Coming Soon

Biography
Isabella Drolz serves as the Vice President of Marketing & Product Strategy at Comet AG's X-ray Systems Division. The division develops advanced X-ray/CT systems and AI software solutions under its brands Comet Yxlon and Dragonfly. Comet Yxlon provides X-ray and CT inspection solutions from lab to fab environments, while Dragonfly offers AI-powered software that enables scientists, researchers, and industrial customers to perform complex image analyses and extract actionable insights in a repeatable, reliable, and cost-efficient manner, driving product yield.

In her role, Isabella oversees Market and Product Management, Global Application & Training Centers, Marketing, and the Academia Program. She holds a degree in industrial engineering, a Bachelor of Science in International Business Administration, and an MBA from Southern Nazarene University in Oklahoma City, USA. With a strong background in mechanical and plant engineering, Isabella has held several management roles focused on market-driven product and business development.

References

Importance of High-Performance Integrated Metrology for D2W and W2W Hybrid Bonding Applications

T. Schmidt
Product Manager Bonder
SUSS MicroTec Solutions GmbH, Business Unit
Bonder, Sternenfels, Germany

Abstract

Integrated high-performance metrology for overlay has become a key requirement for state-of-the-art hybrid bonding applications not only as a potential quality gate for incoming substrates, but in particular to monitor bonding performance in general.

Powered by the need of more and more memory and computing capabilities, hybrid bonding is gradually adopted to produce the required chips for HPC application. This advanced packaging technology relies on dielectric fusion bonding of two wafers or dies together at room temperature, electrical interconnection of the Cu pads is formed subsequently at the post-bond anneal in a separate oven. Surface quality, cleanliness and Cu-recess control are key process parameters to ensure high yield and cost-effective integration of this assembly technology. The different bonding strategies, from W2W towards known good dies selected and transferred directly to the target wafer (sequential D2W) or via a temporary substrate (collective D2W) are illustrated in the following figure below.

In this article, we want to shift the focus towards the requirements for integrated metrology solutions and discuss the benefits and results obtained by in-line measurement to enable both, high bonding performance and process control.

We present the W2W overlay concept based on our dual side pneumatic deflection and bond wave propagation concept. This technology features, together with a 20mK temperature control enables for scaling correction and offer a <50nm post bond accuracy (@3sigma) with a max vector not larger than 80nm. In order to ensure and monitor the bonding performance, a powerful and reliable metrology solution is required. The integration of the ISO3-based SET NEO HB flip-chip bonder into a SUSS production cluster even places additional requirements on the metrology platform for void free sequential D2W placement. Integrated metrology can easily feedback both wafer-to-wafer and die-to-wafer alignment offsets if sufficiently fast and accurate. In case of D2W direct glass carrier pick-up capability allows to handle and realize void free stacking of <50um thin dies assisted by up to 3kgF bond force to mitigate the die-warpage. Furthermore, by combining D2W with W2W bonding, thin dies placed on glass carrier with LR/TBM can be collectively transferred in one single step to the target wafer. Here D2CW overlay error can then be improved by prior overlay mapping and derived global offsets.

Biography

Thomas Schmidt is Product Manager in the Bonder Division of SUSS MicroTec iSolutions GmbH n Sternenfels. After his graduation in Microsystems Technology at the University of applied sciences in Kaiserslautern he has held various positions in MEMS/semiconductor processing and has also lectured on advanced lithography as well as on MEMS and advanced CMOS fabrication.
Since December 2017 Thomas Schmidt is a member of the Bonder Division of SUSS MicroTec (product line "Permanent Wafer Bonding“) with a strong focus on automated cluster platforms for MEMS/packaging applications and hybrid bonding for advanced packaging.

References

Sinter Print Surface Condition Measurement for Power Electronics

A. Lindloff
Senior Process Specialist Pre-Sales
Koh Young Europe GmbH, Alzenau, Germany

Abstract
Within the semiconductor packaging landscape, printing remains the preferred material transfer method due to its historical reliability and cost-effectiveness spanning millennia. In electronic industries, stencil printing is particularly favored for its prolonged usability of metal sheets in mass-production settings. The quality of stencil printing is intricately linked to various critical factors affecting material transfer efficiency, a pivotal consideration as print quality serves as the linchpin for subsequent processes. Rigorous control of print quality is instrumental in minimizing costs and defects.

The standard for monitoring and controlling material transfer efficiency in automotive electronic production is 3D phase-shifting shadow Moiré metrology. Leveraging a comprehensive 3D reconstruction of the measurement object and its surroundings, this methodology allows for an exhaustive analysis of the surface condition of a sinter pad. Precise measurement and analysis of critical factors, including peaks, holes, height, and chip placement area slope, become possible. Given the sinter material's limitations, holes act as thermal isolators, creating operational hotspots, and peaks pose a risk for stress-induced cracks. Consequently, controlling surface conditions is imperative for mitigating premature failures.

Effectively controlling surface conditions requires specialized algorithms. In the stencil print process, where edges of sintering paste pads may deviate from specifications, the analysis area is strategically confined to the chip placement region. High repeatability and accuracy in measuring peaks and holes within this area enable the generation of data that can be employed for direct response to the print process or for process modeling. This includes the analysis of critical hole and peak sizes to preempt premature failures.

Keywords: sintering, printing, 3D measurement, phase-shifting shadow Moiré

Biography
Axel Lindloff studied general electrical engineering at the Bielefeld University of Applied Sciences and has been active in the SMT world since 1999. He initially gained 3 years of experience in sales of stencils and consumables before moving to the application department of a well-known printing machine manufacturer in 2003. Here, he worked until 2012 with the optimization of existing processes, audits and the development of new printing applications. Since September 2012, Mr. Lindloff has been working for Koh Young Europe GmbH as an application engineer. Here, he mainly deals with questions relating to solder paste printing and process optimization with the 3D data obtained.

References

Pioneering Precision: AI Enhancements in Packaging Visual Inspection

B. Van Poucke
VP Market Strategy and Development
Robovision, Gent, Belgium

Abstract
In the context of back-end packaging and test lines, the semiconductor industry is witnessing a paradigm shift towards Industry 4.0 principles. This represents a significant opportunity for Integrated Device Manufacturers (IDMs) and Outsourced Assembly and Test (OSAT) entities to enhance throughput, minimise capital expenditures, and gain a firmer grip on cost efficiency.
Chiplets and heterogeneous integration solutions are characterised by the use of new materials, more complex process steps, and a high level of customization. This results in a growing defect complexity and the need for very efficient and high performance quality control.
Traditional approaches often lead to significant time expenditure on recipe creation, as the number of products, customised processes, process steps, and inspection machines increases. Even the most advanced recipes struggle to classify all defects with great accuracy.
In this paper, we chart a path to lights out operation in the era of advanced packaging. We first introduce a new approach using deep learning vision AI for defect inspection and then present a path to large scale operation by means of tangible strategies and solutions for the main operational challenges.
The approach can be best described as a “Subject Matter Expert first” workflow providing minimum description and knowledge loss in the creation of vision AI models which helps achieve human-like performance. Combined with a set of easy to use governance flows for label purity, data set purity and model performance monitoring this approach also guarantees optimal model performance at initial model creation and during model operation.
Instantiating this approach in a systemic way requires a platform approach governing the full model life cycle management with self-service data consumption for SME’s and data scientists. A single platform, providing flexibility in early process research and stability in High Volume Manufacturing.
The approach shows an 48% increase in FTE productivity for critical competences like data scientists, process owners and computer scientists and as such tackles the critical competence challenges of the semiconductor industry. The SME-first approach both creates trust with SME’s to start using vision AI, while it enables them to fully drive model outcomes. Last but not least it offers an agile model development capable of driving continuous model improvements and handling the large product mix in an efficient way.

Biography
Bart Van Poucke is leading the semiconductor market strategy and devlopment at Robovision, a platform provider for developing scalable vision AI solutions to power intelligent machines. He started his semiconductor carreer at imec in Belgium in various roles from research engineer towards business devlopment roles.

References

Innovative Approaches to Improve Reliability in Microelectronics - The ECSEL JU project iRel40

K. Pressel
Assembly and Packaging
Infineon Technologies AG, Regensburg, Germany

Abstract
Coming Soon

Biography
Dr. Klaus Pressel studied Physics at the University of Würzburg and with a scholarship of the German DAAD at S.U.N.Y. Albany (New York, U.S.A.). Klaus received his PhD in Physics from the University of Stuttgart for research on point defects in III/V semiconductors. He then joined IHP Frankfurt (Oder), where he focused on Si CMOS and SiGe design and technology. In 2001 Klaus joined Infineon Technologies at Regensburg, where he is focusing on innovations in assembly and packaging technology. His special interests are System-in-Package solutions, high frequency applications, chip-package-board/system co-design, as well as understanding reliability and quality. Klaus has been project leader of many European funded projects, e.g. the recent ECSEL JU iRel40 project. Klaus is representing Infineon in various international technical committees, e.g. SEMI Advanced Packaging Conference, ESTC, the Eureka XECS program, IEEE Heterogeneous Integration Roadmap. Klaus is author/co-author of more than 200 publications in semiconductor physics and technology, circuit design, assembly and interconnect technology and owns/co-owns more than 20 patents.

References

Quantum Failure Analysis for the Semiconductor Industry

M. Garsi
Head of Hardware
QuantumDiamonds GmbH, Munich, Germany

Abstract
Advanced packaging solutions such as 2.5/3D integration and chiplets, are becoming essential. However, they complicate access and introduce new failure modes including verticals. Similar problems arise with modern trends such as the move to backside power delivery or new materials for high power devices. Diamond-based quantum sensing can image currents from multiple layers non-destructively via their magnetic field. The technique is capable of detecting defects in hidden layers and infere three-dimensional current density distributions. In addition, high sensitivity is achieved at DC currents as well as higher frequency bands up to several GHz. In this talk, we will present the capabilities of the innovative technique with examples from multiple industries including advanced packages.

Biography
Dr. Fleming Bruckmaier has seven years of working experience in quantum technologies, including a PhD from the Technical University of Munich. He worked on cutting-edge diamond-based technologies targeted at the semiconductor and bio-tech markets resulting in several publications in prestigious journals such as Science Advances or Nature Communications.
Since 2022 he is CTO at the Munich-based quantum sensing company QuantumDiamonds, which develops magnetic field microscopes, used in semiconductor electrical failure analysis.

References

Driving Sustainability in Semiconductor Packaging

P. Farbos de Luzan
Head of Sustainability, Electronics
Henkel, Sustainability, Singapore, Singapore

Abstract
Henkel Adhesive Technologies aims to be the leader in sustainable adhesive solutions for the electronics industry, fostering climate action, circularity, and safety worldwide.

Within our wirebond and advanced packaging solutions portfolio, we innovate to reduce greenhouse gas emissions through sustainable use of raw materials and enhanced adhesive efficiency.

Moreover, we prioritize responsible chemistry, avoiding or replacing harmful substances to ensure a toxic-free product portfolio that benefits both people and the planet.

At the keynote, Pierre Farbos de Luzan, Head of Sustainability at Henkel Electronics, will discuss Henkel's ongoing efforts, solutions, and challenges in promoting sustainability in semiconductor packaging.

Biography
Pierre is the Head of Sustainability for global Electronics business at Henkel, leading the development and implementation of sustainability strategies with the aim to deliver innovative and sustainable solutions for climate action, circularity and safety.

Prior to that, he was driving the development of sustainability services for Accenture across APAC, Middle-East and Latin America regions, delivering complex and high-value projects for international clients across strategy, sustainability, supply chain and operations.

Pierre holds a bachelor degree from HEC Montreal (Canada) and master degree from ESSEC Business School (France).

References

Competitive and Sustainable Advanced Packaging (CSAP) - a new approach to FO-PLP

M. L. Farrugia
General Manager
Chip Integration Technology Center (CITC),
Nijmegen, Netherlands

Abstract

Fan-out wafer level packaging (FO-WLP) is a well-established technology, enabling high-resolution redistribution layers and complex electrical routing. An emerging variation, fan-out panel level packaging (FO-PLP), offers further advantages in processing area and cost. Scaling FO-PLP to larger areas reduces production costs per product, making it appealing for diverse applications. However, FO-WLP and FO-PLP face challenges in discrete power devices. Power devices, like silicon and silicon carbide diodes and MOSFETs, rely on vertical geometries, necessitating high-performance vertical interconnects through the molding compound (TMV). While fan-out technologies show promise—lower RdsON, improved thermal dissipation, and compatibility with thinner dies—commercial adoption lags due to higher package costs.
We present CSAP technology: Competitive and Sustainable Advanced Packaging . This technology merges advanced packaging processes with printed electronics. CSAP replaces conventional compression molding with laser-drilled vias by a cost-effective, fully additive printing processes. In our proof-of-concept work, we create packages for silicon MOSFET dies and initial electrical results demonstrate the viability of this innovative approach. In particular, the clip and vertical contacts are realized by printing the vias and the seed layer. An electroplating process is used to grow a thicker layer of Cu to ensure good electrical and thermal conductivity. The seed layer is printed into the desired shape and added only at the locations where metallization is required, thereby reducing the material use in the fabrication process.
By quantifying the package costs using a model, we demonstrate that CSAP significantly reduces packaging costs compared to traditional Fan-Out Panel Level Packaging (FO-PLP), making it an attractive technology option for devices that require feature size larger than 60 um.

Biography

Mark Luke is a Canadian born Maltese, now living in the Netherlands for the last 16 years. He graduated in Mechanical Engineering from the University of Malta and joined the semiconductor industry right after. He Started as a process engineer in STM’s Malta assembly plant and later joined STM’s Package Development center in Grenoble, France. In 2007 Mark Luke joined NXP in Nijmegen working on various breakthrough innovation projects and was very active in the transition from gold wire to copper wire. Currently he is the General manager of CITC.

References

Advanced Materials with Tailored Thermal Properties for Advanced Packaging Application

M. Vozarova
Material and 3D Printing Researcher
RHP-Technology GmbH, Advanced Materials,
Seibersdorf, Austria

Abstract

E. Neubauer[1], Z.Kovacova[1], Lea Babejova[1], Maria Vozarova[1], Carmen Vladu[1], M.Kitzmantel[1], D.Dewire[2], J.Vriens[2]

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Lightweight dissipative materials with tailored Coefficient of Thermal Expansion (CTE) is a focal point in materials used in electronic packaging applications. This research aims on materials possessing not only high thermal conductivity, but also allowing to provide significant CTE reduction to conventional Aluminum, Copper and Silver alloys widely employed in electronics. A second material category comprises aluminum alloys reinforced with carbon fibers or with Silicium Carbide (Al-SiC). Especially the fiber reinforced composites allow to tailor the anisotropy of thermal properties. New concepts for the manufacturing have been applied, including methods such as direct hot pressing which allows a precise control of the SiC or Carbon fiber content and facilitates the production of large plates with uniform microstructure up to 400 mm in diameter. This approach allows minimizing energy consumption, while ensuring customizable properties and enhanced thermal and mechanical performance tailored for specific applications. Thermophysical analysis have been carried out showing the positive impact of the inserts on the reduction of the coefficient of thermal expansion as well as the improvement of the thermal diffusivity/conductivity value. Examples of different shapes and heat sink components, which were realized, will be presented.

Biography
Coming Soon

References