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## EU DIGITAL FUTURE FORUM

C. Frieling
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**Biography**
Christopher Frieling is Director for Advocacy and Public Policy at the SEMI Europe Brussels Office. Christopher has a background in EU affairs, innovation, and tech policy. Prior to SEMI he worked at the Brussels office of Fraunhofer in several roles including most recently as Senior Advisor. Christopher holds an MSc in Economics of Science and Innovation and a Bachelor of Business Administration

## HiCONNECTS – An Introduction by NXP

A. Sanfilippo
Senior Manager Public Funding
NXP Semiconductors Germany GmbH, München, Germany

**Abstract**
The challenges and major HiCONNECTS objectives are to transform the centralized cloud platform to decentralized platforms which include edge cloud computing in a sustainable, energy-efficient way. This will

bring cloud services including Artificial Intelligence (AI) closer to the IOT end-users, which enables them to really use the COT and IOT efficiently.
The technologies underpinning this revolutionary step include the development of high-performance computing, storage infrastructure, network interfaces and connecting media, and the analysis of IOT sensors and big data in real-time. This major step forward will enable, for example, the mobile clients (during the 5G deployment phase and 6G exploration) to move among different places with minimum cost, short response time and with stable connection between cloud nodes and mobile devices.
The main underlying technology to be developed by the HiCONNECTS consortium, comprising large industrial players, universities and RTO's, and many SMEs, can be summarized under the title: 'heterogenous integration' (HI) which is needed to meet the computing power, bandwidth, latency and sensing requirements for the next generation cloud and edge computing and applications. The HI revolution brings the electronic components and systems (ECS) into a new domain, which combines traditional silicon wafers integrated circuit (IC), InP based high speed electronics , and Si and InP photonics devices and interconnect.
The HiCONNECTS ambition is to demonstrate, through HI development, a leap in computing and networking reliability and performances across the full vertical and horizontal ECS value chain (i.e. essential capabilities and key applications) in a sustainable way. In addition, HiCONNECTS will focus on the development of next generation design, algorithms, equipment (HW/SW), systems and Systems of Systems (SOS).

**Biography**
Dr. Andrea Sanfilippo is currently working as Senior Manager – Public Funding at NXP Semiconductors, Munich (Germany). Previously, he worked for many years as technology planning and cooperation manager and head of the cooperation dept. for the German speaking area at Huawei Technologies in Munich (Germany) and as innovation manager in the R&D incentives domain at Deloitte and PNO, in Milan (Italy). Andrea also obtained a PhD in Physics at the Fritz Haber Inst. of the Max-Planck Society in Berlin (Germany).

**HiCONNECTS - Photonics Heterogeneous Integration Pilot Line**

D. Velenis
R&D Manager 3D and Silicon Photonics Devices and Components group
imec, 3DSIP, Leuven, Belgium

**Abstract**
Enabling bandwidth scaling of optical interconnects while reducing the energy per transmitted bit, requires the heterogeneous integration of different devices and components in a photonics transceiver system. Challenges related to the integration compatibility of new materials, accurate component assembly, and heat dissipation while maintaining a high-yield process are addressed with the development of a photonics pilot line within the HICONNECTS consortium. The primary activities of the pilot line focusing on co-packaged optics, efficient integration of light sources, and heterogeneous integration of non-silicon components are discussed in this presentation.

**Biography**
Dimitrios Velenis is the leader of the 3D and silicon photonics device and components group at imec. He has been with imec for more than 15 years, with expertise on the benchmarking of advanced integration flows for 3D and Silicon Photonics interconnects. He has obtained M.Sc. and Ph.D. degrees from the University of Rochester. Previously, Dimitrios worked as Assistant Professor at the ECE Department at Illinois Institute of Technology, and as a Research Associate at the University of Rochester. He is author and coauthor of more than 70 papers in journals and conference proceedings.

**3D-RDL & TPV-based Advanced Wafer-Level Packaging Pilot Line for RF applications**

A. Ghannam
Founder & CEO
3DiS Technologies, Labège, France

**Abstract**

In recent decades, the increasing focus in modern communication systems has been on highly integrated and high-performance RF modules based on silicon technologies, where multiple RF channels are frequently consolidated within a single Front-end system, amplifying its complexity and size;

As Moore's law benefits approach their boundaries, enhancements in system performance increasingly depend on the backend of production, particularly the packaging process. thus, researchers are actively pursuing solutions through the integration of multiple RF front-end devices into compact modules using 3D packaging technology.

3DiS will present pilot line 3 under HiCONNECTS project, which is built upon innovative manufacturing and metrology processes to provide 3D mmWave Advanced Wafer-Leve-Packaging solution. The novel packaging process will multi-layer use 3D-RDL and Thru-Package-Vias to enable such complex integration with very low RF losses.

**Biography**

Ayad Ghannam received PhD degree in Microwave, Electromagnetism and Optoelectronic from University of Toulouse III, France, in 2010.
During PhD, he worked as a research engineer at Freescale Semiconductors, France branch, and LAAS-CNRS where he designed high-Q power inductors and developed an Above-IC process for their integration. After graduation, he continued working in LAAS-CNRS as a research engineer where he developed an innovative 3D interconnect technology. He is author of several scientific papers and patents in the field of RF integrated passives and wafer-level packaging. He founded 3DiS Technologies in 2014, a spinoff that offers innovating packaging and 3D system integration solutions based on a novel 3D RDL technology.

**HiCONNECTS - Enhanced Chip manufacturing developments**

D. Pagano
Project Manager
STMicroelectronics, APFEM Catania Wafer Fab
Operations, Catania, Italy

**Abstract**
The challenges and major HiCONNECTS objectives are to transform the centralized cloud platform to decentralized platforms which include edge cloud computing in a sustainable, energy-efficient way. This will bring cloud services including Artificial Intelligence (AI) closer to the IOT end-users, which enables them to really use the COT and IOT efficiently.
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**Biography**
Daniele Pagano is Funding Project Manager at STMicroelectronics s.r.l.
He has covered various positions and responsibility in Catania Wafer Fab Operations (Litography, Dry Etching, APC & SPC, Epitaxy, Quality & Process Control), past experiences in collaborative projects like IMPROVE (2012), INTEGRATE (2015), MADEin4 (2022), SATURN (2023) and nowadays HiCONNECTS

and IPCEI. He is author and co-author of several publications on journals and international conferences.

Dr. Giuseppe Fazio, graduated in physics at University of Milano. He has significant experience in industrial electronic devices and since 2000 he works in Semiconductor industries.
In semiconductor field Giuseppe has significant experiences in advanced process and equipment control. He was APC/AEC group leader in STMicroelectronics, and holding the same position in Numonyx and in Micron from 2009 to 2013.
From 2016 to 2022 as Industrial Engineering project manager, in this position in charge of development and deployment Central Functions IE methodology and systems.
Today in Front End Manufacturing as project manager he coordinates programs aimed at maintaining and improving the performance of production equipment.
Past experiences in collaborative project, he is author and co-author of several publications and some patents.

**Digital Twin Software for Finite Element Analysis.**

R. Tomar
Managing Director
DigitalTwin Technology GmbH, Cologne, Germany

**Abstract**
Finite Element Analysis (FEA) has long been a pivotal tool in engineering and design, enabling the simulation of complex physical systems. However, as industries evolve towards greater complexity and integration, there is an increasing need for advanced software solutions that can enhance the capabilities of FEA. This presentation introduces the concept of Digital Twin Software for Finite Element Analysis (DT-FEA), a transformative approach that harnesses the power of digital twins to elevate the accuracy, efficiency, and comprehensiveness of FEA simulations.

DT-FEA bridges the gap between physical and digital realms by creating a virtual replica of a physical system. This digital twin faithfully captures not only the geometry but also the material properties, boundary conditions, and dynamic behavior of the real-world counterpart. It leverages real-time data integration, AI-driven analytics, and multidisciplinary modeling to continuously update and refine the digital twin's representation, ensuring its fidelity to the evolving physical system.

**Key advantages of DT-FEA include:**
1. Real-time Monitoring and Predictive Analysis: DT-FEA allows engineers and analysts to monitor the performance of physical systems in real time. By continuously comparing the digital twin's behavior to the actual system, deviations and anomalies can be detected early, facilitating predictive maintenance and reducing downtime.

2. Multidisciplinary Integration: DT-FEA enables the integration of multiple simulation domains, such as structural, thermal, fluid, and electromagnetic analysis, within a single platform. This holistic approach provides a comprehensive view of system behavior and interactions.

3. Optimization and Design Exploration: With DT-FEA, designers can explore a vast design space efficiently. Parametric studies and optimization algorithms can be applied to the digital twin, accelerating the development of innovative and efficient solutions.

4. Collaborative Decision-Making: DT-FEA supports collaborative decision-making by providing a common platform for engineers, designers, and stakeholders to interact with and analyze the digital twin. This fosters cross-functional collaboration and informed decision-making.

5. Reduced Cost and Risk: By enabling a deeper understanding of system behavior and performance, DT-FEA reduces the need for costly physical prototypes and mitigates the risk of unexpected failures or performance issues in real-world applications.

**Biography**
*Rahul Tomar* is a distinguished mechanical, civil, and software engineer with over 23 years of extensive experience in the field of engineering and technology. He is most notably recognized as the Co-Founder of *DigitalTwin Technology GmbH*, a groundbreaking company at the forefront of the digital twin revolution in the

engineering and construction sectors.

Rahul's profound understanding of mechanical and civil engineering principles, coupled with his expertise in software development, has played a pivotal role in the success of DigitalTwin Technology GmbH. He has spearheaded the development of innovative software solutions that bridge the gap between the physical and digital worlds, revolutionizing how engineers and designers approach their work.

Through his leadership, DigitalTwin Technology GmbH has enabled organizations across the globe to harness the power of digital twins for real-time monitoring, predictive analysis, and collaborative decision-making. These advancements have not only improved efficiency in engineering and construction projects but have also significantly reduced costs and risks associated with complex ventures.

Rahul Tomar's relentless pursuit of excellence and his unwavering dedication to pushing the boundaries of technology have left an indelible mark on the engineering and software development industries. His vision for the future of digital twin technology continues to drive innovation and transformation, making him a respected figure in the global engineering community.

**The Pack4EU Project - Booster Electronics Packaging, Assembly and Test in Europe**

S. Kroehnert
Senior Manager, Pack4EU-Project
SEMI Europe, Dresden, Germany

**Abstract**
No digitalization without chips, and no chips without package. Pandemic, trade wars, geopolitical crises , supply chain interruptions ... the last view years made visible and perceptible like never before the strong dependencies Europe has in the Semiconductor business on other regions of this world and the fragileness of the Semiconductor supply chain. That's also affecting the - in Europe because of decades of outsourcing strategies anyway very weak - Electronics Packaging, Assembly and Test manufacturing, as an increasingly important part of the Semiconductor value chain. Moore's Law slowing down and higher integration levels for better system performance are achieved by More-than-Moore solutions, System-in-Package and Heterogeneous Integration solutions e.g. for the Packaging of Chiplets. Packaging is becoming a product differentiator, and the increasing complexity moves collaborative Chip-Package-Board-System co-design in the focus of IDMs and OEMs. Through the European Chips Act, the European Union aims to reach its target to double its current global market share to 20% in 2030. But what's about Electronics Packaging, Assembly and Test? Its manufacturing share in Europe is at the moment only 3%. Will the majority of wafers and chips still be shipped to Asia for Packaging, Assembly and Test in 2030 too? The Horizon-Chips-JU-CSA "Pack4EU" project, started in July 2023, is analysing the European OFFER and DEMAND sides for Electronics Packaging, the member states activities and regional focus areas, and the skill and education needs. The project is identifying the gaps and working on policy recommendations for three pillars of the European Chips Act with focus on Electronics Packaging. On top, a "Pan-European Network for Advanced Packaging made in Europe" will be established. This presentation will give an overview of the project and the current work status.

**Biography**
Steffen Kröhnert is Senior Manager, Pack4EU-Project, at SEMI Europe GmbH in Berlin, Germany, since October 2023, and President & Founder of ESPAT-Consulting in Dresden, Germany, since July 2019. He is providing a wide range of consulting services around Semiconductor Packaging, Assembly, and Test, mainly for customers in Europe. Until June 2019, he worked for more than 20 years in different R&D, engineering, and management positions at large IDMs and OSATs in Germany and Portugal, namely Siemens Semiconductors, Infineon Technologies, Qimonda, NANIUM, and Amkor Technology, where he most recently served as Senior Director Technology Development. Since 2016 Steffen has chaired or co-chaired the European SEMI-integrated Packaging, Assembly, and Test - Technology Community (ESiPAT-TC). Steffen has authored or co-authored 23 patent filings and many technical papers in the field of Packaging Technology. He also co-edited two textbooks about "Embedded and Fan-Out Wafer and Panel Level Packaging Technologies”. He is an active member of several technical and conference committees of IEEE EPS - where is was elected to the Board of Governors (2021-2023) for Region 8 (EMEA), IMAPS, SEMI - where he is chairing the Advanced Packaging Conference (APC) committee for more than 10 years, and

SMTA. Steffen holds an M.Sc. in Electrical Engineering and Microsystems Technologies from the Technical University of Chemnitz, Germany.