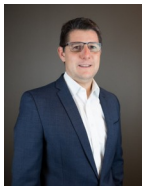
Materials Innovations

Topic Coming Soon



M. Jörger
Head of Business Line Power Electronic Materials
Heraeus Electronics, Head of Business Line Power Electronic Materials, Hanau, Germany

Abstract
Coming Soon

Biography
Michael Jörger has 20 years experience in managing product development and launching of innovative materials for electronics and renewable energies with a focus of Power Modules and Semiconductor Packaging materials.
Michael holds a Ph.D in Material Science from ETH Zurich, Switzerland, and a diploma in chemistry from the University of Karlsruhe in Germany.
Currently he is leading the Business Line Power Electronic Materials at Heraeus Electronics.

Designing Atomic Level Process Chemistries. The Role of Atomistic Simulation in Developing Sustainable Deposition and Etch Processes.

M. Nolan
Head of Group Materials Modelling for Devices
Tyndall National Institute, Cork, Ireland

Abstract
In modern semiconductor device fabrication, the dimensions involved means that Atomic Level Processing, exemplified by Atomic Layer Deposition (ALD), is widely used for film deposition. Further scaling and use of complex three-dimensional structures means that Thermal Atomic Layer Etch (tALE) will start to take centre stage in etching. The key chemistry takes place at surfaces which drives the self-limiting characteristics and other advantages of these atomic level processing approaches.
However, there is a side to device processing that needs to be addressed and this is the heavy environmental impact and non-sustainable nature of current atomic level processing chemistries. Specific examples include: up to 99% of precursors introduced into the processing tool are simply wasted, the high process temperatures, the complex synthesis of precursors (which can add to their high cost), using fluorinated and other environmentally unfriendly chemicals, the large number of sequential deposition & etch cycles which remove material that is wasted and the potentially large number of laboratory experiments (many of which fail) that are needed to develop a new process chemistry. I will present how first principles atomistic simulations based on Density Functional Theory can be used to predict the chemistry of atomic level deposition and etch processes and how these simulations can help with enhancing the sustainability of semiconductor devices processing, setting the industry on the path to truly green and sustainable manufacturing processes. The first topic is the simulation of plasma enhanced deposition (PE-ALD) of metals, using the example of cobalt for next generation interconnects. Our simulations show the first example of an atomistic level study of the full PE-ALD cycle for Co metal. We showed that the process requires use of ammonia or mixed H2/N2 plasma, eliminating the requirement to explore different plasmas to see what works. Calculated energy barriers for key steps give guidance regarding the temperatures required for the process, eliminating the need to explore the role of temperature through multiple time and resource consuming experiments. Finally, we also show how substrate pre-treatment can reduce nucleation delay and therefore deposit the target film more rapidly.
Our second example is MLD of hybrid materials, using alucone and titanicone as the prototypical examples. Using aliphatic ethylene glycol and glycerol results in less-than-ideal growth per cycle (they lie flat) and poor ambient stability. Therefore, we developed functionalized benzene rings as rigid alternatives and show that the molecules remain upright, which provides high GPC and stability. Subsequent work on titanicones with both DFT and experiment, using these aromatic precursors, confirms the enhanced stability of MLD films using aromatic molecule, which also show high growth rates.
My presentation therefore demonstrates how first principles simulations are a vital part of developing greener and more sustainable atomic level processing chemistries for semiconductor device processing. Finding efficient processes through simulations can increase the usage and efficiency of film processing. Other examples where simulations can and will play a role include developing non-halogenated ALE chemistries, better design of reactors to maximise precursor use, better precursor design with higher atom economy and finding alternatives to unsustainable synthesis chemistries.

Biography
Dr. Michael Nolan is the Head of Group - Materials Modelling for Devices at Tyndall National Insitute, UCC, Ireland. Tyndall is Ireland's leading ICT and DeppTech research institute with close on 600 staff and students and is world leading in ICT, communications, photonics, device processing and materials. Dr. Nolan is also interim Cheif Scientist, Chairperson of the Science Council of the Irish Centre for High End Computing and Associate Editor of the Diamond Open Access Beilstein Journal of Nanotechnology. He is a Funded

Investigator on the Science Foundation Ireland Research Centres Insight, AMBER and VistaMilk. Currently Dr. Nolan leads a team of 4 PhD students and 7 postdocs in the first principles simulation of new atomic level processing chemistries, which is carried out together with leading groups in Europe, including M. Knez, A. Devi, C. Detavernier and M. Karppinen and beyond, e.g. S. George. This encompasses atomic layer deposition, atomic layer etch and hybrid molecule layer deposition.

He received his PhD in Microelectronic Engineering in 2004 from University College Cork and was a postdoc with Prof. G. Watson (Chemistry, Trinity CD 2003-05) and Dr. S. Elliott (Tyndall Institute 2005-09) and has been a tenured researcher since 2009, having been promoted to Principal Scientist in 2015 and Head of Group in 2022. Dr. Nolan has graduates 7 PhDs and supervised 7 postdocs. He has published extensively on modelling of surfaces and surface chemistry for energy, semidonductor device and medical device applications.

An important aspect of the group's work is interaction with industry, either through direct funding or leveraged co-funding. Work with industry includes LAM Research (Enterprise Ireland Innovation Partnership, co-I), Stryker (Enterprise Ireland Innovation Partnership, lead-I), Intel, Applied Materials and Logitech, with other contracts subject to commercial sensitivity. Dr. Nolan has a licence agreement with UMICORE and two patents.

Epitaxial Growth of SiGe/Si Multi-Layers for Advanced Logic Devices

R. Khazaka
Principal Technologist and Epitaxy Program Manager
ASM, Leuven, Belgium

Abstract
In this talk, we will review the requirements and challenges of SiGe/Si multi-layers epitaxy for advanced technology nodes, namely complementary FET (CFET). CFET concept relies on stacking top and bottom devices vertically. To enable such integration, the epi stack should be thicker and different compared to gate-all-around architecture. Thus, requiring two different Ge contents in the stack to create etch contrast. In general, high Ge content SiGe layers show relaxation signs earlier than low Ge content SiGe layers, due to the increased lattice mismatch with Si substrate. Therefore, the high Ge content combined with several SiGe/Si layers would make it prone to relaxation and misfit dislocation (MD) appears on the surface. These defects would be detrimental for device performance and needs to be eliminated. Firstly, the characterization techniques suitable to detect such defects would be discussed. Moreover, optimized process conditions to enable fully-strained MD-free wafers will be presented highlighting the feasibility of the stack on industry relevant specs. Finally, transmission electron microscopy images will be shown depicting the sharp interface transition and smooth top surface morphology.

Biography
Dr. Rami Khazaka is Principal Technologist leading the Research and Development (R&D) epitaxy team at ASM Belgium. Dr. Khazaka joined ASM in 2018 as Senior Process Engineer to develop Group IV epitaxy processes. Before joining ASM, he was a postdoctoral researcher at CEA-LETI where he developed material for both CMOS and optoelectronic applications. Dr. Khazaka has more than 15 filed US patents and co-authored more than 30 papers in peer-reviewed journals. He holds a Master degree in renewable energies science and technology from Ecole Polytechnique, Paris, France and Ph.D. in Electronics from the François Rabelais University, Tours, France.

Carbon Nanotube Membranes for EUV Photolithography– a Versatile Material Platform

E. Salmi
Carbon Nanotechnology Engineer
Canatu, Core Engineering, Vantaa, Finland

Abstract
The next generation of high-NA extreme ultraviolet (EUV) photolithography introduces increasingly higher power levels and faster reticle accelerations, enabling the next step in scanner efficiency. This results in higher heat load and mechanical stress on the EUV pellicles. Here we demonstrate carbon nanotube (CNT) pellicles manufactured directly from a floating catalyst chemical vapor deposition (FC-CVD) reactor, using a dry deposition method. This facile direct method yields highly uniform carbon nanotube networks of high strength and purity, enabling exceedingly thin CNT pellicles with high transparency at EUV wavelengths. Control over the FC-CVD synthesis allows tailoring of the carbon nanotube diameter and wall count (SWCNT or FWCNT), as well as control over the CNT network morphology such as the density, bundle size, and orientation of CNTs. The combination of this direct synthesis method with the exceptional mechanical and thermal properties of CNTs provides a versatile membrane platform, which can be further modified with post process steps such as purification to remove metal impurities. To enable conformal and thin coatings on CNTs, wet or dry functionalization steps are demonstrated to match the surface chemistry of CNTs to the specific deposition chemistry used in atomic layer (ALD), chemical vapor (CVD), or physical vapor (PVD) deposition processes. Thicker and denser CNT membranes with appropriate coatings are also suitable for other roles, such as filtering debris from an EUV source, blocking DUV photons and electrons, and providing a gas seal for differential pressure.

Biography
Emma Salmi is a senior nanomaterials engineer at Canatu. She has been spearheading the development of free-standing carbon nanotube membranes with primary focus on the FCCVD synthesis and early processing steps for optimum pellicle manufacturing for two years. Her background encompasses nanotechnology, thin film deposition systems and carbon nanomaterials with 15 years of industrial and academic experience. She has 37 peer-reviewed publications, conference papers and patents.

2D Materials for Future Microelectronic Devices

L. Le Van-Jodin
Project leader
CEA/Leti, DCOS, Grenoble, France

Abstract
Due to their exceptional properties, 2D materials (2DM) are intensively studied for a large spectrum of applications as FET for more Moore developments, sensors, NEMS, optoelectronic or photonic but also more recently for quantum technology. Unlike silicon, 2DM do not suffer from the short channel effect and then could be ultimate material for nanosheet FET. Exceptional performances can be obtained at device level. However, the upscaling required further developments.
In this talk, an overview of the challenges to go from the lab device to the large scale manufacturing. 2DM cannot be industrially processed exactly as silicon and some adaptations have to be found to be able to process them in silicon fab. Indeed, the self-passivated nature of 2D materials required developments to preserve their properties and avoid any damage during the steps like deposition onto 2DM, etching or cleaning. Specific processes are developed allowing an atomic precision. Another key point is the transfer of 2D material from growth substrate to final substrate. Large scale growth made recent progress and processes for good quality of 2D material up to 300 mm wafers already exist. However, the growth temperature is often higher than 700°C, 2DM cannot be deposited during the device manufacturing then have to be transferred by wafer bonding technology. Nanoscale characterization is also a key factor to prepare the large scale integration. Eventually, characteristics of promising devices will be shown as example of 2D material capability for the future of microelectronics.

Biography
Lucie Le Van-Jodin, Ph.D. is a project manager and a team leader for 2D material transfer at CEA-Leti. Lucie started her scientific carrier studying thermoelectricity during her Ph.D research. She started to work at CEA in 2003 on carbon nanotubes for chemtronics, developing growth and characterization of this material. She spent more than 10 years in the CEA's microbatteries Lab. There, she studied the relationship between the structural and electrical properties of the inorganic electrolyte. In 2018, she joined the film transfer Lab (LIFT). She is working on transfer of various materials as silicon, III-V, piezoelectric, wide gap materials… mainly by SmartCut™ technology. Recently, she focused her works on 2D material transfer for microelectronics applications.