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Topic Coming Soon

J. Behnke
INFICON, Cologne, Germany

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Abstract
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Biography
Mr. Behnke has over 35 years of semiconductor industry experience including: logic and memory manufacturing, technology/product development and fab operational excellence. As the GM of Final Phase Systems an INFICON Product Line, John leads a team that develop and deploy SMART software solutions that enable fabs to improve their manufacturing efficiency. FPS's suite of software solutions are built upon a common Datawarehouse which enables advanced Fab Scheduling and optimized WIP movement as well as other related capabilities. He is also a Co-Chair of the Semi North America Smart Manufacturing Special Interest Group.

Prior to FPS John served as the CEO and President of Novati Technologies, the SVP and GM of the Semiconductor Group of Intermolecular, the CVP for Front End Manufacturing, Process R&D and Technology Transfers at Spansion and the Director of AMD's Fab 25's Engineering and Operations groups where he was a founding member of AMD's Automated Precision Manufacturing (APM) initiative which led the Semiconductor industry's development and use of APC and other advanced factory systems. He also led the successful conversion of Fab 25 from Logic to Flash memory which was enabled through the virtual automation of the fab.

Mr. Behnke earned a B.S. degree in Mechanical Engineering with an Industrial Engineering Minor from

Marquette University. Mr. Behnke holds five U.S. patents.

Squeezing More Wafers out of a Fab: Can this be Done without Driving Cycle Times Through the Roof?

P. Lendermann
D-SIMLAB Technologies, Singapore, Singapore

Abstract
Despite the current dip in global IC demand in some areas, industry leaders are optimistic about mid- and long-term growth prospects in semiconductor manufacturing which is also illustrated by the large number of new wafer fabrication facilities that are already under construction or being planned across the globe.
In this setting, optimisation of factory capacity – with the objective to squeeze even more wafers out of existing fabs – will continue to be a critical challenge. To achieve this, powerful techniques to determine fab load mixes that are able to maximise wafers out – or better revenue, or even much better margin – with existing capacity are essential. At the same time, because of the complex operating curve of a wafer fab it is important to precent cycle times from going through the roof to make sure that delivery performance to customers does not suffer. In an environment with fast-changing customer demand and product mixes, as well as frequent commissioning of new equipment this is not an easy task at all.
How such load mix optimisation can be achieved through a combination of static and dynamic (simulation-enabled) capacity models and powerful yet intelligent optimisation techniques will be showcased in this presentation. Enhancement of the wafer out potential by a double-digit percentage without exceeding operationally feasible equipment utilisation limits and without compromising cycle time has been demonstrated with multiple semiconductor manufacturing companies.

Biography
Peter Lendermann is a Co-Founder and the Chief Business Development Officer of D-SIMLAB Technologies, a Singapore-headquartered company providing simulation-based decision support solutions to Semiconductor Manufacturing companies. Prior to this he worked at the Singapore Institute of Manufacturing Technology where he led related R&D activities until spinning them off into D-SIMLAB. Peter has been engaged in the field of production logistics, supply chain management and related decision support technologies and solutions since the early 1990's. He holds a PhD in Physics from Humboldt University in Berlin (Germany) and an MBA in International Economics and Management from SDA Bocconi in Milan (Italy).