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Sustainability Driven Innovation: transistor scaling and defectivity targets for sustainable manufacturing

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Abstract
A key requirement for sustainable innovation is achieving the highest number of good known die (KGD) per wafer. Historically, this has been achieved in parallel with the introduction of larger wafers (greater area), minimizing die size with transistor two-dimensional (2-D) scaling, and improving die quality with defect reduction and yield enhancement efforts.
As wafer size has reached a plateau at 300mm - transistor scaling has transitioned from 2-D to 3-D technologies. 3-D scaling, supported by disruptive technologies such as FinFet, Nanosheet, and Forksheet, will reach an end by 2030. The ultimate frontier of transistor scaling relies now on the complementary FET (CFET) approach, which will unlock the Z-dimension scaling.

Z-dimension scaling will face significant challenges to achieve both high yield and reduce the ecological footprint of the manufacturing process and supply chain. To achieve the targets, sophisticated techniques for early defect detection, quantification, and removal will need to adopt.
Reaching carbon neutrality is a collective effort, and the operational perspective, including new materials introduction, fab management, and manufacturing equipment design - including the whole supply chain – is an important part of the equation.
In this presentation, we explore the scaling roadmap for logic devices, requirements for layer-based tolerable defects with growing device complexity and show examples of technology solutions to achieve high yield with a lower ecological footprint reduction.

Biography
Dr. Yasutoshi Okuno received a Ph.D. degree in engineering from Osaka University, Osaka, Japan, in 1993. He is currently serving as Vice President & Corporate Officer of the technology strategy at SCREEN Semiconductor Solutions Co., Ltd. since 2021 and has been responsible for the technology strategy since 2010. Before that, he managed a module process team for advanced CMOS pathfinding at TSMC for 9 years. His carrier in the field started at R&D Group, Texas Instruments, Inc., Tsukuba, Japan, and moved to Memory R&D Group, Kilby Center, Texas Instruments, Inc. as a FEOL Process Engineer. In late 1998, he is with the ULSI Process Development Group, Panasonic Corporation, where he led the FEOL module integration for the advanced CMOS process.

Exotic applications of nanosecond laser annealing

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Abstract
The need for lower and lower thermal budget in microelectronics has driven annealing technologies from furnaces to millisecond processes. The era of nanosecond laser annealing (NLA) is coming. On one hand, such technique enables treatments at very high temperatures in the melt and sub-melt regimes, with unprecedented cooling rates, that give access to very high active dopant concentrations. One the other hand, thanks to its short pulse duration, NLA also enables surface heating with an excellent in-depth selectivity, which is particularly suited for various 3D architectures. In this presentation, several More-than-Moore applications of NLA currently developed at CEA-LETI will be shared. The use of NLA will be illustrated for 3D sequential integration, for ferroelectric memories integrated in the BEOL and for exotic applications leveraging superconducting silicon.

Biography
Dr. Sébastien Kerdilès received a Ph.D. degree in materials science from the University of Caen, France, in 2000. Then, he worked for 2 years for a start-up in the Paris area. From 2002 to 2013, he worked for SOITEC as a research staff member first, then as a technology development manager, and finally as an SOI designer. During this period, he contributed to the industrialization of 200 & 300mm SOI substrates manufacturing, including RF-SOI and Fully depleted SOI. In 2013, he joined CEA-LETI, where he is in charge of thermal treatments. His research interests include the investigation of pulsed laser annealing for various applications such as 3D integration, memories, and MEMS. He authored or co-authored more than 50 journal articles and conference papers and holds over 20 patents.