

# SEMICON® EUROPA

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## Materials Innovation

### Current trends in digital chemistry to drive semiconductor innovation



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#### Abstract

The semiconductor industry is of course the enabler of digitization, but some commentators have pointed out the irony that it lags behind other industries in its own adoption of digital practices of "Industry 4.0". Looking in particular at R&D, the cost of achieving each successive technology node continues to climb steeply. With the 5 nm node estimated to cost a company \$0.5bn in R&D, immense savings could be made through increased digitization of R&D activities. Such changes will be natural for today's workforce of digital natives, who access data on the cloud, share information in social networks and dial in to meetings online regardless of geography.

Another aspect of the digital revolution is the transformative effect of easy access to vast computing power, and here too the semiconductor industry can benefit from its own technology. In the ideal situation, hypotheses will be tested first in simulation, as this should be both cheaper and more systematic than lab-based experiments. Looking at materials and process R&D, we discuss whether simulation software has achieved the accuracy, ease-of-use and robustness to allow this. We also focus on how to bridge gaps in expertise. Finally, we consider examples of machine learning in materials R&D and how improvements in data curation are needed right across the R&D landscape.

#### Biography

Co-author Dr Mathew D. Halls is Senior Vice President, Materials Science, Schrödinger.

Presenting author Dr Simon Elliott is Director of atomic level process simulation at scientific software company Schrödinger, where he develops and applies techniques based on quantum mechanics and/or machine learning to the surface chemistry of deposition and etch. Prior to this, he studied chemistry at Trinity College Dublin and Karlsruhe Institute of Technology, and until 2018 led research on modelling atomic layer deposition at Ireland's Tyndall National Institute. He was co-chair of the 16th International Conference on Atomic Layer Deposition and chair of the 175-member European network on the same topic. He can sometimes be found introducing theatre improvisation games to scientists as a route to better communication skills.

## EUV Lithography patterning: status and challenges towards High NA



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### Abstract

Nowadays, the device scaling driven by the Moore's law is continuing by the deployment of the 0.33NA extreme ultraviolet lithography (EUVL) in high volume manufacturing for single print and multi-patterning schemes further driven by the need to improve cycle time and cost. To further simplify and improve EUV patterning reducing cost and enable 2nm technology and below, high NA EUV lithography is under development and in 2023 imec and ASML will open a high NA EUV Lab, where the first high 0.55NA scanner will be installed.

At the same time, as the nanoscale is pushed further down, the stochastic nature of the patterning process becomes one of the major patterning roadblocks. To enable the high NA technology new knobs and faster learning cycles on patterning process development are needed to improve the process window and minimize the stochastic patterning defectivity issues. Lithography solutions can't afford alone the stochastic challenges; thus, the etching and thin film processes become essential to holistically offer, together with the lithographic process, novel clean patterning solutions. This presentation will show the latest development on EUV patterning materials and their challenges and provide an insight status of overcoming these obstacles towards high NA.

### Biography

Danilo De Simone holds a MS degree in chemistry from the university of Palermo (Italy) and has 22 years of experience in semiconductor R&D field. He led the development of lithographic materials for 90nm and 65nm NOR Flash devices for STMicroelectronics (STM) in Italy and covered the role of assignee at STM Alliance in France and STM in Singapore. In 2008, he joined Numonyx to lead the R&D development for lithographic materials and first 32nm double patterning for PCM devices. In 2011, he moved to Micron Technology to introduce 45nm phase-change-memory devices in HVM, and to develop patterning solutions for novel devices. In 2013, he joined the international nanoelectronics research center imec leading the research on patterning materials for EUV lithography. He is editorial board member of the Journal of Micro/Nanopatterning, Materials, and Metrology (JM3), member of SPIE committee for the Patterning Materials and Processes program and member of the International Advisory Board of the Photopolymer Science and Technology Conference (ICPST).

## Nanoscale metals are comprised of grain boundaries that are significantly different from those found in bulk materials



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### Abstract

Metals are the simplest of solids and copper is probably the best known and most studied of all. The properties of copper metal of macroscopic dimension are well understood. However, the same cannot be said when copper is reduced to nanoscale dimensions. Like most metals, copper is a granular solid comprised of grains with boundaries between them. Here in this talk we focus on what we have learned about nanoscale copper by using scanning tunneling microscopy and molecular static simulations. In particular we visualize for the first time the 3D structure of grain boundaries (GBs) that emerge at the surface of nearly coplanar copper nanocrystalline (111) films. Remarkably, we find that GBs at surfaces are different from those in the bulk. We show that GBs in metals actually prefer to lie along close packed planes which in turn necessitates the tilting and restructuring of the boundary as it approaches the (111) surface. The restructuring depth can be a few to several tens of nanometers. This behavior is due to a previously unrecognized phenomenon that involves the rotation of the dislocation lines that comprise the GB, which minimize the energy and has significant implications for materials properties [1, 2]. Since transport in copper occurs predominantly along close packed planes these restructure boundaries, which also lie along close packed planes, are expected to have unusual scattering properties. Whether fully relaxed restructured boundaries are possible under device fabrication conditions remains to be established.

### References:

- [1] Xiaopu Zhang, Jian Han, Adrian P. Sutton, David J. Srolovitz, John J. Boland. *Science* 357, 397-400 (2017)
- [2] Xiaopu Zhang, Hailong Wang, Moneesch Upmanyu, John J. Boland (under review)

### Biography

**Prof John Boland** received a BSc degree in chemistry from University College Dublin and a PhD in chemical physics from the California Institute of Technology, where he was an IBM graduate fellow and recipient of the Newby-McKoy graduate research award. From 1984 to 1994 Prof Boland was a member of the research staff at the IBM T.J. Watson Research Center (New York). In 1994 he joined the chemistry faculty at the University of North Carolina at Chapel Hill where he was appointed the J.J. Hermans Chair Professor of Chemistry and Applied and Materials Science. In 2002 Prof Boland moved to the School of Chemistry at Trinity College Dublin as a Science Foundation Ireland Principal Investigator and Professor of Chemistry. In June 2005 he was appointed Director of the Centre for Research on Adaptive Nanostructures and Nanodevices (CRANN) until July 2013. He also served as TCD Vice President and Dean of Research (2015-2017).

Prof. Boland became an elected Fellow of Trinity College Dublin in 2008, a fellow of the American Vacuum Society (AVS) in 2009 and a fellow of the American Association for the Advancement of Science (AAAS) in 2010. He was the 2011 laureate of the ACSIN prize for nanoscience. He is the recipient of an Outstanding Researcher Awards from IBM (1992) and Intel (2017). He is the recipient of a prestigious European Research Council Advanced Grant. Prof. Boland's research interests are focussed on the novel properties of nanoscale materials and their potential in device and sensor applications.

## **How Did and Will Atomic Scale Processing Change the Logic and Memory Industries**

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### **Abstract**

Coming soon

### **Biography**

Coming soon