Future of Computing

Opening Remarks by Session Chair

T. Signamarcheix
Vice President, Strategic Development,
CEA-Leti, Grenoble, France

Abstract
Not Applicable

Biography
Thomas Signamarcheix joined CEA-Leti in 2008, and in 2011, he was named manager of a research laboratory on substrates engineering. From 2015 to 2019, he was in charge of business development management for Leti's Silicon Component Division and Architecture and Embedded Software Division. As Key Account Manager of several strategic collaborations, he also directly managed a wide range of activities (semiconductor, alternative energy, sensor, radio-frequency, etc.) promoting innovation at both hardware and architecture levels.
He has been vice president of CEA-Leti's strategic development since 2020, managing Leti's strategic program (Quantum Electronic, Artificial Intelligence, wearable healthcare devices and mixed reality) and strategic partnerships. He has a PhD in the physics of semiconductor devices from Grenoble Institute of Technology (INPG), and he has contributed to nearly 10 patents and co-authored more than 50 scientific publications.

Com-Putare: Together We Think

M. Peeters
VP R&D Connectivity
imec, Leuven, Belgium

Abstract
Digitization is upon us. And while it feels we have been taking about smart devices forever, it is only in the past years that we have gone from devices that we just call smart to devices that actually need to be smart. And with it, these have gone from simple sensors that measure scalar point values to lidars that map out the world around us. All of this data only has value when consumed, processed and used to close some loop. Here is the crux of our sustainability issue: how do we manage this balance between sending data and processing data, what are the technologies that will enable a sustainable future of computing.

Biography
“If you can't explain it simply, you don't understand it well enough.” (attributed to Einstein, Feynman, and others) → This is the key element in success to every endeavour in research and development. Be it the technical or the business aspects. It drives the three skills I constantly aim to improve: understanding, communicating, and the focus to think and reduce things to their core.

Today, I am VP of R&D for Connectivity at imec. We build the enabling platforms for the next generation of communication systems, from the materials, devices, circuits, signal processing all the way up to the orchestration engines. My previous experience as CTO for both the Wireline and Wireless business lines at (what is now) Nokia was built on the culture, enthusiasm, and love for technology and science that I got from my time at Bell Labs—and the principles of Free Inquiry bestowed on me by my Alma Mater, the Vrije Universiteit Brussel (VUB).

During my research career starting with a Ph.D. in Applied Physics and Photonics from the VUB, I have authored more than 100 peer-reviewed publications, many white papers and hold patents in the access and photonics domains. An electrotechnical engineer by training, I am a senior member of IEEE and a Fellow of the VUB.

Outside of work, my quest to discover the recipe for a perfect lasagna is balanced by bouts of long-distance running to offset the inherent caloric intake.

Will More-than-Moore Technologies with 3D Integration meet the Challenges of Edge AI Devices ?

S. Joly
Parnerships Manager 3D integration and packaging
CEA-Leti, Grenoble, France

Abstract
In the world of high performance computing, over a decade the performances of the computing has constantly increase beyond the almost automatic but slowing down improvement in processor performance with Moore's Law. Big players have moved to new architectures such as chiplets only possible thanks to the integration of More-than-Moore technologies. 2.5D and 3D integration, memory cubes, accelerators and heterogeneous architectures are key elements of the success towards performance and energy efficiency. This transition has shown clear benefits and sustainability for HPC market. The question is still open for Edge AI components where real time, ultra-low power, large amount of data, low cost are the main drivers: how can 3D integration play a role for these embedded processors? CEA-Leti has been involved for more than two decades in 3D integration with industrial partners. This presentation will discuss about:

- What are the main drivers for computing in edge devices ?
- What could be the architectures' new paradigm ?
- How 3D integration will be an enabler, and how CEA-Leti's roadmap supports this promising technology

Biography
Sylvie Joly is currently working as 3D integration and packaging Partnerships Manager at CEA-LETI. Sylvie received M.Sc. in Microelectronics from ISEP "Institut Supérieur d'Electronique de Paris" in 1989. She completed her education with a Master in Marketing and Innovation at the Grenoble Ecole de Management (GEM) in 2001. Prior to this position, she worked for more than 8 years as display business developer at CEA-LETI. In 2004 as Sr. Marketing Engineer in the CEA's Technology Transfer Department, she built a strong experience in setting up and managing technical marketing surveys. Before joining CEA, she spent 10 years in the industry as an R&D engineer, and 8 years as Sales engineer in several companies including Hewlett Packard and Ericsson.

A Materials to Systems Understanding of a BEOL Embedded Analog NVM Memory Technology for Edge Compute Applications

M. Chudzi
VP of Technology for IMS
Applied Materials, Dresden, Germany

Abstract
Coming Soon

Biography
Dr. Chudzik is VP of Technology for IMS at Applied Materials focusing on device and module engineering solutions in the specialty and packaging segments.
He has a PH.D in Electrical engineering from Northwestern University.
Mike has been at Applied Materials for 8 years and prior to that he worked at IBM for 14 years in various roles in DRAM and CMOS process integration and management.

MicroLED Advance Bonding Method to enable AR Metaverse

R. Yan
Business Unit Director
GLOBALFOUNDRIES, Dresden, Germany

Abstract
Mark Zuckerberg and companies seem to think that smart glasses will one day replace smartphones. They're not alone, and it will probably happen at some point in the not-too-distant future. But for such a product to exist, we still face plenty of challenges both in hardware and software, especially in the microdisplay that is required for smart glasses.
MicroLED is one of the best microdisplay solutions for smart glasses. The key challenges are how to integrate LED arrays from a small epi wafer to a full-size CMOS backplane wafer in a way that is cost-effective. A crude method is coring: the larger CMOS wafer is cored to the size of the epi wafer and the two are bonded with wafer-to-wafer (W2W) bonding tools. This is suitable for R&D and low volume production, but there is too much wasted CMOS wafer to be valid for mass production. Another method is Direct Die-to-Wafer (D2W) Integration: the pixelated frontplane epi wafer is diced and the resulting dies are then bonded to corresponding locations on the backplane wafer. While this reduces the amount wasted, bonding accuracy becomes more challenging, and throughput is potentially slower.
GF believes that innovative D2W integration is a good way to increase throughput. In this method, epi dies are first transferred to blank wafer of the same size as the backplane wafer. Standard W2W bonding is then used to finish the integration of frontplane and backplane.
In this paper, we will present GlobalFoundries® (GF®) advanced D2W bonding solution to resolve the microLED manufacturing challenges.

Biography
Ruby is a Business Line director in AIM Strategic Business Unit. She is responsible for HMI (Human-Machine-Interface) product line in wearable, AR/VR, smart home and machine vision applications.