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Advanced Packaging Conference

Building Europe's Digital Future - A Pan European Investment



F. Scheper

Corporate Vice President in the Sales and Marketing Group General Manager and President EMEA

Intel Corporation, Oisterwijk, The Netherlands



Abstract

Building Europe's Digital Future - A Pan European Investment

Biography

Frans Scheper is Corporate Vice President in the Sales and Marketing Group General Manager and President, for Europe, Middle East and Africa (EMEA) for Intel Corporation.

Frans is responsible for Intel's overall business in EMEA which includes driving revenue growth, engaging with the local ecosystem to create new opportunities, and strengthening Intel's existing regional customer and partner relationships.

As President, Frans oversees Intel's recently announced plans for the "once-in-a-generation" investment in Europe as part of its IDM 2.0 strategy, with research, design, leading-edge semiconductor manufacturing and industry partnerships that will help build Europe's digital future.

Frans recently joined Intel (2022) from ams OSRAM, where he was Chairman and Executive Vice President of Opto Semiconductors. He brings extensive European and international market experience, having also held executive board positions at WeEn Semiconductors, NXP Semiconductors and the CEO position at Nexperia.

Based in the Netherlands, Frans holds a bachelor's degree in business and commerce from HES Den Haag, and an MBA from the International Institute for Management Development (IMD).

Semiconductors for Software Defined Vehicles



L. Beer
VP Product Management ASIC's & SOC's
Robert Bosch GmbH, Automotive Electronics,
Reutlingen, Germany

Abstract

The importance of SW in Automotive is constantly increasing and currently we are reaching a point where its justified to talk about software defined vehicles.

In his talk, Leopold will elaborate why semiconductors became a special focus topic for automotive OEM's and what this means for the traditional automotive semiconductor and system suppliers. At this stage of evolution, traditional, hierarchical supply chains restructure into to supply networks - opening up opportunities for new players.

Based on technology requirements, Leopold will show how this new structures could look like and which are the new Key Succes Factors for the involved players.

Leopold will use real life examples to explain the way Bosch Automotive Electronics addresses this topic.

Biography

Mr. Leopold Beer

VP Product Management ASIC's and SOC's within the Bosch Automotive Electronics Division.

Leopold Beer graduated the University of Stuttgart with a diploma in Physics. He specialized in semiconductor physics.

Leopold started his career as engineer in the DRAM plant of Siemens Semiconductors (Today Infineon Technologies) in Regensburg and since then held various functions in the automotive and semiconductor industry.

Leopold joined Bosch Sensortec in 2006 as Director of Sales and was later on promoted to Head of Global Marketing and Product Management. From 2013 to 2018 Leopold held the position of Regional President for Asia Pacific and was based in Shanghai/China. Since August 2018, Leopold oversees the ASIC & SOC product portfolio of Bosch Automotive Electronics.

Amkor Activities in Portugal and Overall Trends in Europe



J. Silva
Vice President of Operations & R&D
Amkor Technology Europe Portugal (ATEP),
Mindelo, Portugal



Abstract

Coming soon

Biography

José joined Amkor in July 2017 as part of the Nanium acquisition and is currently Vice President of Operations & R&D at ATEP. He started his career in the semiconductor industry at Siemens and later held management positions as Quality Director and Operations Director at Infineon, Qimonda and Nanium. José holds a degree in Electrical Engineering from Universidade do Porto and an MBA from Porto Business School.

Opening Remarks



R. Rettenmeier
Senior Product Marketing Manager
Evatec AG, BU Advanced Packaging, Truebbach,
Switzerland



Abstract

not applicable

Biography

Roland Rettenmeier qualified as a Mechanical Engineer in 1997 and completed his MBA studies at Vienna and Danube Universities in Austria in 2005. Roland extended his education through many further formal international courses and programs since that time (e.g. Six Sigma Program with AT&S and Nokia; Innovation Technology Leader at Stanford University).

Roland has worked in the field of Electronics and Semiconductor manufacturing since 2001, managing multiple international projects. After joining Evatec in 2016 as Senior Product Marketing Manager (PMM) within the Business Unit for Advanced Packaging, he focused on business development for Panel Level Packaging where Evatec has now become the recognised market leader for thin film technology solutions. Since 2020 he has also supported development of Evatec's wafer level packaging solutions business.

In addition to his market and customer responsibilities, Roland represents Evatec in the Panel Level Packaging consortium of Fraunhofer IZM Berlin, in the Packaging Research Center at Georgia Tech, USA and in the Panel Level Packaging Consortium at the NCAP in Wuxi, China.

Complete LVS verification methodology and process for complex System-In-Package assemblies



R. Theveniau
CAD Support Senior Staff Engineer
ST Microelectronics, Crolles, France



Abstract

Systems in Package (SiP) have been around for some years and were typically the integration of multiple bare unpackaged chips along with discrete devices interconnected with just a few signals. However, as silicon scaling (aka Moore's Law) slows and silicon densities reach their physical limits, there is growing shift to disaggregation of once monolithic functions into smaller, node optimized high yield chiplets, heterogeneously integrated on a high-performance substrate as an advanced System-In-Package (SiP), or module. These designs utilize multiple high performance and high bandwidth interfaces between the chiplets enabling higher densities, greater device functionality, and improved overall silicon yield. All the devices used in a SiP are often designed concurrently, by different teams, in different time zones. Thus, the risk to make mistakes in data exchange is very high. To mitigate this risk a comprehensive system description along with a controlled data exchange flow is key. Furthermore, although each device is tested independently, there is a need for a formal signoff check or verification that covers the whole system.

In STMicroelectronics we have developed an automated layout versus schematic (LVS) methodology that electrically verifies the module and system-level designs logical connectivity. Using a combined 3D assembly level DRC/LVS methodology our divisions can prevent System in Package failures due to swapped balls, shorted power nets or any uncontrolled change in the design layouts.

This paper will describe the essential steps and process of a fully integrated workflow that can verify and validate a complete multi-chiplet SiP design assembly using an LVS approach including the technologies used to enable such a solution.

Biography

After 5 years spent in Cadence UK and 5 years in Texas Instruments France, Raphael Theveniau joined STMicroelectronics in 2009 as System in Package expert. He is now part of Technology R&D group in ST, in Digital Design Flows and Methodology team. He has more than 20 years of experience in Digital Design, covering most aspects of place and route and signoff flows and package design. His role as SiP expert consists in developing, promoting and supporting flows through ST kits for internal divisions as well as external customers. Now his role is more focused on Die-Package Co-design flows, and more specifically System in Package LVS.

Ultra-fine pitch Die bonding approaches with Cu interconnects for high-performance 3D IC packages



A. Roshanghias
staff scientist
Silicon Austria Labs GmbH, Villach, Austria



Abstract

Cu to Cu direct bonding is currently the most attractive approach for 3D integration due to its compatibility with the wafer back-end-of-the-line (BEOL) fabrication process. Direct or hybrid Cu bonding is an established wafer-to-wafer (w2w) bonding process at foundries. However, considering the increasing demand for heterogeneous chip stacking and high production yield with known good die (KGD), chip-to-chip (C2C), and chip-to-wafer (C2W) Cu bonding processes still encounter technological challenges. In this study, we will explore different die-level bonding strategies for both protruded and recessed Cu interconnects. Here, Cu bumps with a diameter of 4 μm , and a pitch size of 18 μm surrounded by SiO₂ layer were fabricated with different topographies (dishing heights) and were bonded at the different bonding temperatures. The results of the electrical examinations, bonding strength, texture, and interface analysis will be further discussed here.

Biography

Dr. Ali Roshanghias is currently a staff scientist in the department of heterogeneous integration technologies at Silicon Austria Labs (SAL). He received his Ph.D. in materials science and technology from Sharif University of Technology (Iran) in 2012. He pursued his career as a post-doc researcher at Nagaoka University of Technology (Japan) and Vienna University (Austria) in the fields of electronic materials and advanced microelectronics packaging. In 2015 he joined Silicon Austria Labs (formerly known as CTR Carinthian Tech Research AG) as a senior scientist and project manager. His research interests include heterogeneous integration technologies, hybrid electronics, and 3D integration.

Optimization of the Cu Microstructure to Improve Cu-to-Cu Direct Bonding for 3D Integration

R. Schmidt
R&D Manager Semiconductor
Atotech, Berlin, Germany



Abstract

Advanced packaging solutions and heterogeneous integration are key technologies to enable devices with improved operating characteristics, including higher performance, increasing power efficiency, and decreasing form factor. Packages with high I/O densities are required to efficiently combine, e.g., processing and memory units but impose restrictions to the pitch of the interconnects. Conventional technologies, including wire bonds and flip chip bonds are limited to larger pitches and, therefore, not suitable to meet the requirements of upcoming packaging technologies with respect to I/O densities. Direct copper-to-copper interconnects are supposed to allow such small pitches of 10 μm or even below. However, formation of such bonds usually requires high temperatures and pressures. Temperature-sensitive devices like DRAM components restrict the maximum temperature that can be applied to the package. Thus, copper material is required, which allows bond formation at relatively low temperatures. In this context, hybrid bonding processes were discussed that involve initial bond formation via the usually oxide-based dielectric at room temperature followed by copper-to-copper bonding at elevated temperatures. The copper material is usually prepared by electrolytic deposition and the properties of the respective deposits may be modified by properly designed organic additives as well as process parameters. Strong bond formation of the copper should be obtained upon grain growth over the interface of the two deposits, which are brought into contact during the bonding step. In order to facilitate such growth at relatively low temperatures, suitable microstructures need to be prepared. Ideally, morphologies should be chosen in a way that they can be maintained throughout all process steps after the electrolytic deposition but, at the same time, allow grain growth over the interface during copper-to-copper bonding. Various strategies to enable improved seamless grain growth and maintain suitable microstructures throughout the preceding process steps will be compared in terms of the resulting copper microstructures after bonding. In this context, different electrolytic copper deposition processes, the resulting morphologies, as well as their respective advantages and challenges with regards to copper-to-copper bond formation will be discussed.

Biography

Experience with process development for semiconductor applications since 2016

Author of numerous scientific publications and patents in the area of metallization for semiconductor applications.

Lecturer at the Humboldt University of Berlin since 2013

Experience with metallization processes for electronics industry for > 10 years

Predictive Maintenance Scheduling for Assembly Manufacturing



C. Bode
Technical Product Manager
INFICON, Intelligent Manufacturing Systems,
Austin, United States of America



Abstract

The semiconductor industry and its struggles with supply chain issues have made the global news almost daily. Tactical options to address issues with existing manufacturing assets include getting more capacity out of existing fabs and/or enabling fabs run a broader mix of technologies and products for a longer period. Factory automation capabilities are certainly a necessary solution to facilitating such improvements, whether in terms of maximizing tool availability or manufacturing productivity. Assembly facilities are beginning to adopt such solution in volume from their front-end manufacturing counterparts to good effect. Smart Manufacturing solution integration is increasingly demonstrating the capability to move beyond point solution development in back-end facilities to deliver differentiating capabilities in manufacturing efficiency and productivity. This talk will discuss examples of harmonizing deployed solutions to facilitate predictive maintenance scheduling through the integration of tool control and factory scheduling.

INFICON has deployed Smart Manufacturing capabilities to a customer Assembly site that demonstrates the end-to-end solution and business process integration of a predictive maintenance capability. FabGuard® Fault Detection and Classification (FDC) is deployed on a Disco grinder tool to monitor a number of tool parameters for general tool control capability, but also monitors the blade thickness over time to predict when a blade replacement will be needed. Such information is shared with the factory Digital Twin to support overall factory modeling and prediction capability. Factory Scheduler, in addition to performing the nominal responsibility of scheduling material to be run on each of the tools, can consume the FDC data and maintenance prediction to schedule an optimal time to perform the tool maintenance given operator and tool availability. The shared decision support with the integrated solution makes it so that the parts and assignment of duties can be done ahead of time, minimizing tool downtime and maximizing maintenance efficiency. The presentation will discuss the deployment and impact of these solutions as deployed in our customer facility.

Biography

Christopher Bode, PhD is a recognized process control and factory automation solution developer within the semiconductor industry. He has over 25 years experience with APC technology development and implementation, as well a general factory systems development and integration across solution domains, with prior stints at AMD and GLOBALFOUNDRIES. He currently is a Technical Product Manager with INFICON in their Intelligent Manufacturing System organization, with responsibilities across their FabGuard (TM) and FPS product lines.

Ultra low-temperature silver sintering materials for substrate-based power applications

R.-X. Dong
Project Leader
Niching Industrial Corp., R&D Division, Hsinchu,
Taiwan



Abstract

The demand of high powder semi-conductor devices is increasing continuously. Especially for wide band gap (WBG) semiconductors, the die-attach (DA) materials need to be bonded at a lower temperature, $\leq 200^{\circ}\text{C}$ ideally, and operated at a high temperature ($\sim 300^{\circ}\text{C}$). Low-temperature sintering silver provides excellent properties to meet the requirement of DA materials on WBG applications. The common sintering temperature of commercial products is $> 200^{\circ}\text{C}$. High sintering temperature generates a higher level of thermal stress in the DA materials, which would cause negative effects for larger dies, including void generation, delamination, crack, metallization peeling, and so on. Lower sintering temperature could reduce thermal stress during packaging processes. In addition to 200°C sintering Ag paste (DN-1206Q), we have developed DA Ag paste with 175°C sintering temperature (DN-1301A) for the requirement of low stress. This article is investigating the effect of sintering temperature on the performance and properties of DA materials.

The storage modulus of 175°C (DN-1301A) and 200°C (DN-1206Q) sintering Ag paste are 14 and 18 GPa respectively. This is more than 20% reduction which could be a great help in terms of thermal stress. As for die shear strength (DSS), DN-1301A showed comparable results while curing at 175°C comparing with DN-1206Q curing at 200°C . Thermal conductivity (TC) of both 175°C and 200°C sintering Ag paste is more than 120 W/mk. In summary, lower sintering temperature can reduce the thermal stress of DA materials which is a positive contribution to the resistance of temperature variations. The performance of DN-1301A curing at 175°C is similar to 200°C sintering Ag paste (DN-1206Q). Based on this study, it is very promising that a lower sintering temperature at 175°C for silver sintering paste can deliver similar performance as curing at 200°C . This could be a breakthrough for those requiring lower curing temperature such as laminate substrate-based packages.

Biography

2006-2010 Ph.D, Institute of Polymer Science and Engineering, National Taiwan University.
2014-2016 Researcher, Industrial Technology Research Institute
2016-2019 R&D Manager, New Micropore, Inc.
2019-Now R&D Project Leader, Niching Industrial Co.

3M Insulative Thermal Bonding Film (ITBF) for Power Module Packaging



W. Grommes
European Application Development
3M, Neuss, Germany



Abstract

Abstract:

The traditional substrate used in power modules is ceramic based, and typically called a Direct Bonded Copper (DBC) substrate. Comparing to DBC, the newly emerging Insulated Metal Substrate (IMS) shows benefits in smaller and thinner design with higher power density, better warpage control in packaging processes, and potential overall cost reduction, while offering comparable heat dissipation. The key insulation material in IMS is the organic composite thermally conductive sheet bonding to both copper foil and baseplate. The current challenges for this insulation material is how to improve its thermal conductivity, insulation properties, processability and long term reliability.

In this presentation, we introduce a new 3M solution for Insulative Thermal Bonding Film (ITBF) for IMS substrate in power module packaging. Based on 3M thermal management material technologies for filler, polymer and processes, we have developed a thermal bonding film with thermal conductivity up to 12 W/mK, and with superior insulation breakdown voltage >6.5 KV at thicknesses of 120 and 150 μm . Material aging and shelf life studies have been conducted. 3M ITBF film showed stable performance in 3000-hour aging tests at 150°C, showing 3M ITBF advantages in product handling and reliability. IMS substrates have been fabricated with 3M ITBF film and have demonstrated good copper bonding and lamination processability. Both thermal resistance and dielectric insulation have been measured based on industry standard methods, demonstrating that 3M ITBF film can enable high performance IMS. Based on the fabricated IMS substrate, a materials model was established. Simulations of heat dissipation and stress management demonstrated that 3M ITBF can significantly reduce insulator stress and slightly improve chip solder stress. Furthermore, the development of 3M ITBF roadmap is discussed.

Walther Grommes, Patricia Tien, Monroe Wang, Davie Wang, Koji Ito, Evelyn Liao, Marc Dunham, Benson Chen, Wei Zou

Biography

Walther Grommes has many years of experience in the semiconductor industries as a manufacturing & process development engineer.

Bachelor Professional of Chemical Production and Management, 1996, IHK Munich.

Since 2007 at 3M in the Electronics Markets Solutions Division, responsible as European Application Development Specialist

for various semiconductor applications on adhesive & tape solutions, wafer support system for thin wafer solutions, cleaning & coating solutions.

Semiconductor Packaging Materials Enabling Advanced Flip-Chip and Heterogeneous Integration



R. Trichur
Global Head of Semiconductor Packaging
Henkel Corporation, Irvine, United States of
America



Abstract

In recent years, semiconductor chip package architectures have become more complex to deliver various applications' power, performance, size, and cost requirements. Chipsets used in consumer electronics devices such as mobile phones and handheld electronics predominantly require miniaturization, high functionality, low cost, and low power. Therefore, the packages specified for this market segment may include package-on-package (PoP) formats to save space or wafer-level packages (WLP) to deliver lower cost and, in many cases, higher functionality. In comparison, processors used in high-performance computing (HPC) and artificial intelligence (AI) applications place a premium on performance while balancing cost, power, and footprint. Because of these factors, packaging architects have developed several custom package formats like chiplets, large-die flip-chip, and multi-chip packages in 3D and 2.5D, among others. Both end markets require unique innovations in semiconductor packaging materials to enable efficient package production and in-application performance. While package designs have come a long way, challenges to meeting new, demanding requirements persist. Advanced packaging material solutions are central to addressing these issues.

Liquid compression molding materials are predominantly used in fan-out or chip-on-wafer packaging for wafer-level encapsulation processes. As the interconnect density or stacking height increases, fine-filler, low-warpage materials are necessary to deliver the package's reliability and the wafer's processability. In AI and HPC applications, the package body size increases with subsequent generations. These large body packages are susceptible to thermal stresses resulting in warpage and reliability concerns. Component level adhesives like lid and stiffener attach materials must be able to manage/prevent warpage while maintaining good adhesion and reliability performance. Lastly, underfills also play a crucial role in packaging logic and memory devices. Pre-applied and post-applied underfill in liquid and film formats are needed to address challenges in flow time, interconnect density, voiding, crack formation, and various other issues. This Keynote will present the latest innovations in encapsulation materials used for fan-out wafer-level molding processes, alongside developments in advanced liquid underfills and lid/stiffener attach materials.

Biography

Coming soon

GlobalFoundries 22FDX® Auto grade 1 Chip Package Interaction Reliability Assessment



S. Capecchi
MTS Reliability
GlobalFoundries, Quality and Reliability, Dresden,
Germany



Abstract

Semiconductor devices are becoming every year more pervasive in the automotive industry. Moreover, the growth of the Electrical Vehicle (EV) market in addition to new features such as Advanced Driver Assistance Systems (ADAS), Lidar and auto connectivity is accelerating this trend. The value of the market for automotive semiconductor applications is set to grow from about \$35B in 2020 to about \$80B in 2026 (~15% CAGR) and it is expected to reach about \$300B by 2035*. Therefore, this tremendous growth has generated an increased interest for semiconductor IDMs and foundries to enter or strengthen their presence in the automotive supply chain.

In this work we present a chip package interaction (CPI) Automotive Grade1 reliability assessment performed onto a GlobalFoundries 22FDX® technology test vehicle. The presentation will focus mainly on the temperature humidity bias life test (THB), which is one of the AEC-Q100 requirements. The aim of the CPI assessment is to prove that the GlobalFoundries 22FDX® back-end of line metallization (BEoL) the passivation and the Far BEoL interconnects are robust enough in an Auto G1 standard package and can withstand the AEC-Q100 grade 1 reliability environmental stresses.

For this purpose, a test vehicle has been designed and fabricated by GlobalFoundries Fab1 including the Cu pillar interconnects. The subsequent packaging has been carried out by an external Auto G1 qualified OSAT using their Auto G1 HVM bill of material (BOM) and assembly process. The environmental stresses and electrical readout have been carried out in GlobalFoundries Fab1.

The test vehicle is a 22FDX® 8x8 mm² silicon die assembled in a 14x14 mm² Flip Chip Chip Scale Package (FCCSP) with an Embedded Trace Substrate (ETS) coreless substrate. This test vehicle contains various kinds of CPI sensors distributed in sensitive die locations.

Compared to the component level reliability stress, which is also carried out as part of the CPI assessment, the THB assessment requires a dedicated board level stress and a dedicated test infrastructure. The THB adapter card assembly process, the electrical test pre and post stress and the THB reliability environmental stress have been set up and carried in GlobalFoundries Fab1.

The focus of this presentation is on the technical challenges, such as the CPI structure design, the THB board and adapter card design, the electrical readout, and the adapter card assembly.

*Source: Yole Développement

Biography

I am currently a member of the quality and reliability group in GlobalFoundries Fab1 in Dresden, Germany. The main focus of my activity is Chip Package Interaction (CPI) reliability. I have previously worked in process engineering in Globalfoundries, ST-Microelectronics and in Intel.

I hold a Master's Degree in Physics

Reliability characterization of silver sintering for die attach applications



E. Smits
Program Manager
CITC, Nijmegen, The Netherlands



Abstract

With advances in miniaturization of electronic components, there is a trend towards ever increasing power density in semiconductor devices. In part, Wide-Band Gap (WBG) materials such gallium nitride (GaN) and silicon carbide (SiC) have enabled more efficient devices but also allowed for much higher operating temperatures. Consequently power dissipation and mechanical stresses in electronic packages have increased dramatically. From environmental perspectives, there is a strong drive to phase out lead-based solder.

Discrete components are commonly assembled in packages based copper lead frames. The key challenge for such packages are the mismatches in coefficient of thermal expansion (CTE) between Cu lead frame and WBG power dies. During operation, the packages repeatedly undergo temperature swings, causing repeated thermomechanical stresses and fatigue. When not mitigated, these stresses lead to premature failure of the electronic components.

Silver Sinter pastes (pressure based and pressureless) are a promising replacement of lead rich solder combining superior thermal and electrical performances. It is the scope of major research activity but a reliable solution for attaching WBG semiconductors to copper bases while retaining superior thermal and electrical performances has proven to be challenging. Unlocking the full potential of WBG semiconductor power electronics will hinge on solving these technological challenges at the package level.

In this presentation, the author presents an overview of *CITC* research activities on advanced packaging with a focus on packaging for power electronics and silver sintering solutions. An overview of the current state of silver sinter materials is provided. The performance and limitations of the materials are addressed. Beyond materials, methods used to investigate the performances and degradation will be covered as well as the thermomechanical simulations for predicting package reliability.

Biography

Edsger Smits received his Ph.D. with honors from the University of Groningen in the field of organic electronics. In 2009, he joined TNO/Holst Centre focusing oxide based thin film transistors for displays, flexible and stretchable sensors and electronics for bio-medical applications. In 2021 he become responsible for the "Power Packaging " at CITC. Topics of interests include mini and micro led, laser transfer, flexible and stretchable electronics and power packaging.

HFBP as a New and Better Approach to DFN



M. Azzopardi
Business Development Engineering
JCET, Dresden, Germany



Abstract

Coming Soon

Biography

Mark Azzopardi has been building semiconductor packaging experience for just over 20 years, after getting his Engineering degree in Mechanical engineering from the University of Malta in 2002. He started his career as a process engineer and moved to R&D for SiP and MEMS packaging. Mark then joined Statchippac, now JCET, in 2011 as technical program manager and moved to Business Development supporting the European local sales team early 2022.

Innovative Sensor Packaging in Europe



B. Knott
Head of the Infineon Technologies Backend
Innovation Group
Infineon, Dresden, Germany



Abstract

The presentation will include topics like: eWLB radar (fan-out WLP at Infineon Regensburg); Pressure sensors e.g. for automotive; Magnetic sensors and Gas sensors.

Biography

Bernhard Knott is the Head of the Infineon Technologies Backend Innovation group. He is responsible for new Package Concepts, Prototyping, new Materials, Simulation and Virtual Prototyping. Until 2016 he was leading the Package Development for Sensors and Waferlevel Package Development in Regensburg, Germany. Prior joining the Backend Organization, he held several Management Position in Frontend Technology dealing with BiCMOS Technologies, Sensors and Innovation projects. After receiving his Diploma in Physics from the University of Regensburg, he started his career in Semiconductor Industry in 1997 in developing an embedded NVM Technology. Bernhard holds several patents and patent applications in the area of FE Technology, Sensors and Packaging.

Impulse Printing™: Enabling 3D Printed Interconnects for Volume Production



R. Hendriks
Program Lead
Holst Centre / TNO, Eindhoven, The Netherlands

Abstract

Impulse Printing™ is a brand new technology developed by Holst Centre that will bring unique 3D interconnect solutions to the back-end semiconductor and display market. High resolution structures can be printed over steps, gaps, and even wrapped around substrates at incredible speeds. For example, wrap-around printing of electrodes to create a back-to-front interconnect for μ LED displays, or printing directly on silicon dies as an alternative to wire bonding. Off the shelf materials such solder paste, conductive adhesive, silver micron flake ink, copper nanoparticle ink and dielectric ink have already been printed successfully, showing compatibility with a wide range of viscosities and particles sizes. The unique capability of printing almost any materials onto any type of topology makes Impulse Printing™ suitable for quick adoption into existing production lines.

Biography

Program Lead experienced in developing novel printing technologies in the field of hybrid printed electronics. Responsible for defining the overall strategy and leading the execution of innovative technologies, including ultra-high resolution printing, laser-assisted transfer, 3D printed electronics and photonic soldering. Driven by innovation and determined to take concepts to full industrial implementation. Over 10 years of experience working in research and start-up environment across the U.S. and Europe.

The challenges in testing small and highly integrated devices in a massive parallel test system

M. Wagner
Engineering Manager - Interface Solutions Group
Cohu, Interface Solutions Group, Kolbermoor,
Germany



Abstract

The triumph of electronic components started in the 1950s with the introduction of semiconductor transistors. Since this time the content of electronics has risen significantly. Innovations in the semiconductor industry are supporting the megatrends like mobility car electrification including ADAS-systems, sensors, connectivity, and advanced security.

This trend drives demand for enhanced packaging concepts like system-in-package (SiP), SoC and heterogeneous integration, as well as optimized existing and new materials that support package miniaturization including pad size reduction, smaller pad to pad distance and thermal performance.

Time to market and cost are the main challenges for new electronic technologies that will be deployed in mass production.

This Presentation describes the development of a contactor for singulated, small WLCSP devices in massive parallelism test, supporting more than 200 contact sites. It considers different aspects which address the challenges of reliable and cost-efficient device testing. The active retracting technology in the contactor increases the reliability of processing the devices after test as well as supporting force-controlled device handling and methods of accurately aligning contactor probes to fine-pitch device pads or balls. It further addresses the cost-effectiveness by supporting highly parallel testing and performance monitoring over the entire lifetime to optimize maintenance intervals by an integrated track and trace feature

The presentation will also review the thermal aspects of testing devices in a high parallelism environment.

This approach requires close cooperation with the Handler supplier in order to optimize the overall performance of the entire system

Biography

Markus Wagner is Engineering Manager of the Interface Solutions Group at Cohu and is based out of Kolbermoor, Germany. Markus graduated from the University of Rosenheim with a Diploma in Mechanical Engineering. He has been in the semiconductor final test environment more than 20 years with Cohu, a provider of semiconductor equipment and services for the back-end semiconductor manufacturing. Markus has held a number of management positions in engineering and product marketing and holds several patents for innovative contacting solutions. Over the years he has gained experience in integrating contactors solutions into MEMS and final test systems.