Advanced Packaging Conference

Semiconductors for Software Defined Vehicles

L. Beer
VP Product Management ASIC's & SOC's
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Abstract
The importance of SW in Automotive is constantly increasing and currently we are reaching a point where its justified to talk about software defined vehicles.
In his talk, Leopold will elaborate why semiconductors became a special focus topic for automotive OEM's and what this means for the traditional automotive semiconductor and system suppliers. At this stage of evolution, traditional, hirarchical supply chains restructure into to supply networks - opening up opportunities for new players.
Based on technology requirements, Leopold will show how this new structures could look like and which are the new Key Succes Factors for the involved players.
Leopold will use real life examples to explain the way Bosch Automotive Electronics addresses this topic.

Biography
Mr. Leopold Beer
VP Product Management ASIC’s and SOC’s within the Bosch Automotive Electronics Division.

Leopold Beer graduated the University of Stuttgart with a diploma in Physics. He specialized in semiconductor physics.
Leopold started his career as engineer in the DRAM plant of Siemens Semiconductors (Today Infineon Technologies) in Regensburg and since then held various functions in the automotive and semiconductor industry.

Leopold joined Bosch Sensortec in 2006 as Director of Sales and was later on promoted to Head of Global Marketing and Product Management. From 2013 to 2018 Leopold held the position of Regional President for Asia Pacific and was based in Shanghai/China. Since August 2018, Leopold oversees the ASIC & SOC product portfolio of Bosch Automotive Electronics.

Complete LVS verification methodology and process for complex System-In-Package assemblies

R. Theveniau
CAD Support Senior Staff Engineer
ST Microelectronics, Crolles, France

Abstract
Systems in Package (SiP) have been around for some years and were typically the integration of multiple bare unpackaged chips along with discrete devices interconnected with just a few signals. However, as silicon scaling (aka Moore's Law) slows and silicon densities reach their physical limits, there is growing shift to disaggregation of once monolithic functions into smaller, node optimized high yield chiplets, heterogeneously integrated on a high-performance substrate as an advanced System-In-Package (SiP), or module. These designs utilize multiple high performance and high bandwidth interfaces between the chiplets enabling higher densities, greater device functionality, and improved overall silicon yield. All the devices used in a SiP are often designed concurrently, by different teams, in different time zones. Thus, the risk to make mistakes in data exchange is very high. To mitigate this risk a comprehensive system description along with a controlled data exchange flow is key. Furthermore, although each device is tested independently, there is a need for a formal signoff check or verification that covers the whole system.
In STMicroelectronics we have developed an automated layout versus schematic (LVS) methodology that electrically verifies the module and system-level designs logical connectivity. Using a combined 3D assembly level DRC/LVS methodology our divisions can prevent System in Package failures due to swapped balls, shorted power nets or any uncontrolled change in the design layouts.
This paper will describe the essential steps and process of a fully integrated workflow that can verify and validate a complete multi-chiplet SiP design assembly using an LVS approach including the technologies used to enable such a solution.

Biography
After 5 years spent in Cadence UK and 5 years in Texas Instruments France, Raphael Theveniau joined STMicroelectronics in 2009 as System in Package expert. He is now part of Technology R&D group in ST, in Digital Design Flows and Methodology team. He has more than 20 years of experience in Digital Design, covering most aspects of place and route and signoff flows and package design. His role as SiP expert consists in developing, promoting and supporting flows through ST kits for internal divisions as as well as external customers. Now his role is more focused on Die-Package Co-design flows, and more specifically System in Package LVS.

Ultra-fine pitch Die bonding approaches with Cu interconnects for high-performance 3D IC packages

A. Roshanghias
staff scientist
Silicon Austria Labs GmbH, Villach, Austria

Abstract
Cu to Cu direct bonding is currently the most attractive approach for 3D integration due to its compatibility with the wafer back-end-of-the-line (BEOL) fabrication process. Direct or hybrid Cu bonding is an established wafer-to-wafer (w2w) bonding process at foundries. However, considering the increasing demand for heterogeneous chip stacking and high production yield with known good die (KGD), chip-to-chip (C2C), and chip-to wafer (C2W) Cu bonding processes still encounter technological challenges. In this study, we will explore different die-level bonding strategies for both protruded and recessed Cu interconnects. Here, Cu bumps with a diameter of 4 µm, and a pitch size of 18 µm surrounded by SiO2 layer were fabricated with different topographies (dishing heights) and were bonded at the different bonding temperatures. The results of the electrical examinations, bonding strength, texture, and interface analysis will be further discussed here.

Biography
Dr. Ali Roshanghias is currently a staff scientist in the department of heterogeneous integration technologies at Silicon Austria Labs (SAL). He received his Ph.D. in materials science and technology from Sharif University of Technology (Iran) in 2012. He pursued his career as a post-doc researcher at Nagaoka University of Technology (Japan) and Vienna University (Austria) in the fields of electronic materials and advanced microelectronics packaging. In 2015 he joined Silicon Austria Labs (formerly known as CTR Carinthian Tech Research AG) as a senior scientist and project manager. His research interests include heterogeneous integration technologies, hybrid electronics, and 3D integration.

Optimization of the Cu Microstructure to Improve Cu-to-Cu Direct Bonding for 3D Integration

R. Schmidt
R&D Manager Semiconductor
Atotech, Berlin, Germany

Abstract
Advanced packaging solutions and heterogeneous integration are key technologies to enable devices with improved operating characteristics, including higher performance, increasing power efficiency, and decreasing form factor. Packages with high I/O densities are required to efficiently combine, e.g., processing and memory units but impose restrictions to the pitch of the interconnects. Conventional technologies, including wire bonds and flip chip bonds are limited to larger pitches and, therefore, not suitable to meet the requirements of upcoming packaging technologies with respect to I/O densities. Direct copper-to-copper interconnects are supposed to allow such small pitches of 10 µm or even below. However, formation of such bonds usually requires high temperatures and pressures. Temperature-sensitive devices like DRAM components restrict the maximum temperature that can be applied to the package. Thus, copper material is required, which allows bond formation at relatively low temperatures. In this context, hybrid bonding processes were discussed that involve initial bond formation via the usually oxide-based dielectric at room temperature followed by copper-to-copper bonding at elevated temperatures. The copper material is usually prepared by electrolytic deposition and the properties of the respective deposits may be modified by properly designed organic additives as well as process parameters. Strong bond formation of the copper should be obtained upon grain growth over the interface of the two deposits, which are brought into contact during the bonding step. In order to facilitate such growth at relatively low temperatures, suitable microstructures need to be prepared. Ideally, morphologies should be chosen in a way that they can be maintained throughout all process steps after the electrolytic deposition but, at the same time, allow grain growth over the interface during copper-to-copper bonding. Various strategies to enable improved seamless grain growth and maintain suitable microstructures throughout the preceding process steps will be compared in terms of the resulting copper microstructures after bonding. In this context, different electrolytic copper deposition processes, the resulting morphologies, as well as their respective advantages and challenges with regards to copper-to-copper bond formation will be discussed.

Biography
Experience with process development for semiconductor applications since 2016
Author of numerous scientific publications and patents in the area of metallization for semiconductor applications.
Lecturer at the Humboldt University of Berlin since 2013
Experience with metallization processes for electronics industry for > 10 years

Semiconductor Packaging Materials Enabling Advanced Flip-Chip and Heterogeneous Integration

R. Trichur
Global Head of Semiconductor Packaging
Henkel Corporation, Irvine, United States of America

Abstract
In recent years, semiconductor chip package architectures have become more complex to deliver various applications' power, performance, size, and cost requirements. Chipsets used in consumer electronics devices such as mobile phones and handheld electronics predominantly require miniaturization, high functionality, low cost, and low power. Therefore, the packages specified for this market segment may include package-on-package (PoP) formats to save space or wafer-level packages (WLP) to deliver lower cost and, in many cases, higher functionality. In comparison, processors used in high-performance computing (HPC) and artificial intelligence (AI) applications place a premium on performance while balancing cost, power, and footprint. Because of these factors, packaging architects have developed several custom package formats like chiplets, large-die flip-chip, and multi-chip packages in 3D and 2.5D, among others. Both end markets require unique innovations in semiconductor packaging materials to enable efficient package production and in-application performance. While package designs have come a long way, challenges to meeting new, demanding requirements persist. Advanced packaging material solutions are central to addressing these issues.
Liquid compression molding materials are predominantly used in fan-out or chip-on-wafer packaging for wafer-level encapsulation processes. As the interconnect density or stacking height increases, fine-filler, low-warpage materials are necessary to deliver the package's reliability and the wafer's processability. In AI and HPC applications, the package body size increases with subsequent generations. These large body packages are susceptible to thermal stresses resulting in warpage and reliability concerns. Component level adhesives like lid and stiffener attach materials must be able to manage/prevent warpage while maintaining good adhesion and reliability performance. Lastly, underfills also play a crucial role in packaging logic and memory devices. Pre-applied and post-applied underfill in liquid and film formats are needed to address challenges in flow time, interconnect density, voiding, crack formation, and various other issues. This Keynote will present the latest innovations in encapsulation materials used for fan-out wafer-level molding processes, alongside developments in advanced liquid underfills and lid/stiffener attach materials.

Biography
Coming soon

GlobalFoundries 22FDX® Auto grade 1 Chip Package Interaction Reliability Assessment

S. Capecchi
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GlobalFoundries, Quality and Reliability, Dresden, Germany

Abstract

Semiconductor devices are becoming every year more pervasive in the automotive industry. Moreover, the growth of the Electrical Vehicle (EV) market in addition to new features such as Advanced Driver Assistance Systems (ADAS), Lidar and auto connectivity is accelerating this trend. The value of the market for automotive semiconductors applications is set to grow from about $35B in 2020 to about $80B in 2026 (~15% CAGR) and it is expected to reach about $300B by 2035*. Therefore, this tremendous growth has generated an increased interest for semiconductors IDMs and foundries to enter or strengthen their presence in the automotive supply chain.

In this work we present a chip package interaction (CPI) Automotive Grade1 reliability assessment performed onto to a GlobalFoundries 22FDX® technology test vehicle. The presentation will focus mainly on the temperature humidity bias life test (THB), which is one of the AEC-Q100 requirements. The aim of the CPI assessment is to prove that the GlobalFoundries 22FDX® back-end of line metallization (BEoL) the passivation and the Far BEoL interconnects are robust enough in an Auto G1 standard package and can withstand the AEC-Q100 grade 1 reliability environmental stresses.

For this purpose, a test vehicle has been designed and fabricated by GlobalFoundries Fab1 including the Cu pillar interconnects. The subsequent packaging has been carried out by an external Auto G1 qualified OSAT using their Auto G1 HVM bill of material (BOM) and assembly process. The environmental stresses and electrical readout have been carried out in GlobalFoundries Fab1.

The test vehicle is a 22FDX® 8x8 mm^2 silicon die assembled in a 14x14 mm^2 Flip Chip Chip Scale Package (FCCSP) with an Embedded Trace Substrate (ETS) coreless substrate. This test vehicle contains various kinds of CPI sensors distributed in sensitive die locations.

Compared to the component level reliability stress, which is also carried out as part of the CPI assessment, the THB assessment requires a dedicated board level stress and a dedicated test infrastructure. The THB adapter card assembly process, the electrical test pre and post stress and the THB reliability environmental stress have been set up and carried in GlobalFoundries Fab1.

The focus of this presentation is on the technical challenges, such as the CPI structure design, the THB board and adapter card design, the electrical readout, and the adapter card assembly.

*Source: Yole Développement

Biography

I am currently a member of the quality and reliability group in GlobalFoundries Fab1 in Dresden, Germany. The main focus of my activity is Chip Package Interaction (CPI) reliability. I have previously worked in process engineering in Globalfoundries, ST-Microelectronics and in Intel.

I hold a Master's Degree in Physics

Reliability characterization of silver sintering for die attach applications

E. Smits
Program Manager
CITC, Nijmegen, The Netherlands

Abstract
With advances in miniaturization of electronic components, there is a trend towards ever increasing power density in semiconductor devices. In part, Wide-Band Gap (WBG) materials such gallium nitride (GaN) and silicon carbide (SiC) have enabled more efficient devices but also allowed for much higher operating temperatures. Consequently power dissipation and mechanical stresses in electronic packages have increased dramatically. From environmental perspectives, there is a strong drive to phase out lead-based solder.
Discrete components are commonly assembled in packages based copper lead frames. The key challenge for such packages are the mismatches in coefficient of thermal expansion (CTE) between Cu lead frame and WBG power dies. During operation, the packages repeatedly undergo temperature swings, causing repeated thermomechanical stresses and fatigue. When not mitigated, these stresses lead to premature failure of the electronic components.
Silver Sinter pastes (pressure based and pressureless) are a promising replacement of lead rich solder combining superior thermal and electrical performances. It is the scope of major research activity but a reliable solution for attaching WBG semiconductors to copper bases while retaining superior thermal and electrical performances has proven to be challenging. Unlocking the full potential of WBG semiconductor power electronics will hinge on solving these technological challenges at the package level.
In this presentation, the author presents an overview of *CITC* research activities on advanced packaging with a focus on packaging for power electronics and silver sintering solutions. An overview of the current state of silver sinter materials is provided. The performance and limitations of the materials are addressed. Beyond materials, methods used to investigate the performances and degradation will be covered as well as the thermomechanical simulations for predicting package reliability.

Biography
Edsger Smits received his Ph.D. with honors from the University of Groningen in the field of organic electronics. In 2009, he joined TNO/Holst Centre focusing oxide based thin film transistors for displays, flexible and stretchable sensors and electronics for bio-medical applications. In 2021 he become responsible for the “Power Packaging “ at CITC. Topics of interests include mini and micro led, laser transfer, flexible and stretchable electronics and power packaging.

Impulse Printing™: Enabling 3D Printed Interconnects for Volume Production

R. Hendriks
Program Lead
Holst Centre / TNO, Eindhoven, The Netherlands

Abstract
Impulse Printing™ is a brand new technology developed by Holst Centre that will bring unique 3D interconnect solutions to the back-end semiconductor and display market. High resolution structures can be printed over steps, gaps, and even wrapped around substrates at incredible speeds. For example, wrap-around printing of electrodes to create a back-to-front interconnect for µLED displays, or printing directly on silicon dies as an alternative to wire bonding. Off the shelf materials such solder paste, conductive adhesive, silver micron flake ink, copper nanoparticle ink and dielectric ink have already been printed successfully, showing compatibility with a wide range of viscosities and particles sizes. The unique capability of printing almost any materials onto any type of topology makes Impulse Printing™ suitable for quick adoption into existing production lines.

Biography
Program Lead experienced in developing novel printing technologies in the field of hybrid printed electronics. Responsible for defining the overall strategy and leading the execution of innovative technologies, including ultra-high resolution printing, laser-assisted transfer, 3D printed electronics and photonic soldering. Driven by innovation and determined to take concepts to full industrial implementation. Over 10 years of experience working in research and start-up environment across the U.S. and Europe.

The challenges in testing small and highly integrated devices in a massive parallel test system

M. Wagner
Engineering Manager - Interface Solutiosn Group
COHU, Interface Solutuions Group, Kolbermoor, Germany

Abstract
The triumph of electronic components started in the 1950s with the introduction of semiconductor transistors. Since this time the content of electronics has risen significantly. Innovations in the semiconductor industry are supporting the megatrends like mobility car electrification including ADAS-systems, sensors, connectivity, and advanced security.

This trend drives demand for enhanced packaging concepts like system-in-package (SiP), SoC and heterogeneous integration, as well as optimized existing and new materials that support package miniaturization including pad size reduction, smaller pad to pad distance and thermal performance.

Time to market and cost are the main challenges for new electronic technologies that will be deployed in mass production.

This Presentation describes the development of a contactor for singulated, small WLCSP devices in massive parallelism test, supporting more than 200 contact sites. It considers different aspects which address the challenges of reliable and cost-efficient device testing. The active retracting technology in the contactor increases the reliability of processing the devices after test as well as supporting force-controlled device handling and methods of accurately aligning contactor probes to fine-pitch device pads or balls. It further addresses the cost-effectiveness by supporting highly parallel testing and performance monitoring over the entire lifetime to optimize maintenance intervals.by an integrated track and trace feature

The presentation will also review the thermal aspects of testing devices in a high parallelism environment.

This approach requires close cooperation with the Handler supplier in order to optimize the overall performance of the entire system

Biography
Markus Wagner is Engineering Manager of the Interface Solutions Group at Cohu and is based out of Kolbermoor, Germany. Markus graduated from the University of Rosenheim with a Diploma in Mechanical Engineering. He has been in the semiconductor final test environment more than 20 years with Cohu, a provider of semiconductor equipment and services for the back-end semiconductor manufacturing. Markus has held a number of management positions in engineering and product marketing and holds several patents for innovative contacting solutions. Over the years he has gained experience in integrating contactors solutions into MEMS and final test systems.