Semiconductor Packaging Materials Enabling Advanced Flip-Chip and Heterogeneous Integration

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Abstract
In recent years, semiconductor chip package architectures have become more complex to deliver various applications' power, performance, size, and cost requirements. Chipsets used in consumer electronics devices such as mobile phones and handheld electronics predominantly require miniaturization, high functionality, low cost, and low power. Therefore, the packages specified for this market segment may include package-on-package (PoP) formats to save space or wafer-level packages (WLP) to deliver lower cost and, in many cases, higher functionality. In comparison, processors used in high-performance computing (HPC) and artificial intelligence (AI) applications place a premium on performance while balancing cost, power, and footprint. Because of these factors, packaging architects have developed several custom package formats like chiplets, large-die flip-chip, and multi-chip packages in 3D and 2.5D, among others. Both end markets require unique innovations in semiconductor packaging materials to enable efficient package production and in-application performance. While package designs have come a long way, challenges to meeting new, demanding requirements persist. Advanced packaging material solutions are central to addressing these issues.
Liquid compression molding materials are predominantly used in fan-out or chip-on-wafer packaging for wafer-level encapsulation processes. As the interconnect density or stacking height increases, fine-filler, low-warpage materials are necessary to deliver the package's reliability and the wafer's processability. In AI and HPC applications, the package body size increases with subsequent generations. These large body packages are susceptible to thermal stresses resulting in warpage and reliability concerns. Component level adhesives like lid and stiffener attach materials must be able to manage/prevent warpage while maintaining good adhesion and reliability performance. Lastly, underfills also play a crucial role in packaging logic and memory devices. Pre-applied and post-applied underfill in liquid and film formats are needed to address challenges in flow time, interconnect density, voiding, crack formation, and various other issues. This Keynote will present the latest innovations in encapsulation materials used for fan-out wafer-level molding processes, alongside developments in advanced liquid underfills and lid/stiffener attach materials.

Biography

Coming soon

GlobalFoundries 22FDX® Auto grade 1 Chip Package Interaction Reliability Assessment

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Abstract

Semiconductor devices are becoming every year more pervasive in the automotive industry. Moreover, the growth of the Electrical Vehicle (EV) market in addition to new features such as Advanced Driver Assistance Systems (ADAS), Lidar and auto connectivity is accelerating this trend. The value of the market for automotive semiconductors applications is set to grow from about $35B in 2020 to about $80B in 2026 (~15% CAGR) and it is expected to reach about $300B by 2035*. Therefore, this tremendous growth has generated an increased interest for semiconductors IDMs and foundries to enter or strengthen their presence in the automotive supply chain.

In this work we present a chip package interaction (CPI) Automotive Grade1 reliability assessment performed onto to a GlobalFoundries 22FDX® technology test vehicle. The presentation will focus mainly on the temperature humidity bias life test (THB), which is one of the AEC-Q100 requirements. The aim of the CPI assessment is to prove that the GlobalFoundries 22FDX® back-end of line metallization (BEoL) the passivation and the Far BEoL interconnects are robust enough in an Auto G1 standard package and can withstand the AEC-Q100 grade 1 reliability environmental stresses.

For this purpose, a test vehicle has been designed and fabricated by GlobalFoundries Fab1 including the Cu pillar interconnects. The subsequent packaging has been carried out by an external Auto G1 qualified OSAT using their Auto G1 HVM bill of material (BOM) and assembly process. The environmental stresses and electrical readout have been carried out in GlobalFoundries Fab1.

The test vehicle is a 22FDX® 8x8 mm^2 silicon die assembled in a 14x14 mm^2 Flip Chip Chip Scale Package (FCCSP) with an Embedded Trace Substrate (ETS) coreless substrate. This test vehicle contains various kinds of CPI sensors distributed in sensitive die locations.

Compared to the component level reliability stress, which is also carried out as part of the CPI assessment, the THB assessment requires a dedicated board level stress and a dedicated test infrastructure. The THB adapter card assembly process, the electrical test pre and post stress and the THB reliability environmental stress have been set up and carried in GlobalFoundries Fab1.

The focus of this presentation is on the technical challenges, such as the CPI structure design, the THB board and adapter card design, the electrical readout, and the adapter card assembly.

*Source: Yole Développement

Biography

I am currently a member of the quality and reliability group in GlobalFoundries Fab1 in Dresden, Germany. The main focus of my activity is Chip Package Interaction (CPI) reliability. I have previously worked in process engineering in Globalfoundries, ST-Microelectronics and in Intel.

I hold a Master's Degree in Physics

Reliability characterization of silver sintering for die attach applications

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Abstract
With advances in miniaturization of electronic components, there is a trend towards ever increasing power density in semiconductor devices. In part, Wide-Band Gap (WBG) materials such gallium nitride (GaN) and silicon carbide (SiC) have enabled more efficient devices but also allowed for much higher operating temperatures. Consequently power dissipation and mechanical stresses in electronic packages have increased dramatically. From environmental perspectives, there is a strong drive to phase out lead-based solder.
Discrete components are commonly assembled in packages based copper lead frames. The key challenge for such packages are the mismatches in coefficient of thermal expansion (CTE) between Cu lead frame and WBG power dies. During operation, the packages repeatedly undergo temperature swings, causing repeated thermomechanical stresses and fatigue. When not mitigated, these stresses lead to premature failure of the electronic components.
Silver Sinter pastes (pressure based and pressureless) are a promising replacement of lead rich solder combining superior thermal and electrical performances. It is the scope of major research activity but a reliable solution for attaching WBG semiconductors to copper bases while retaining superior thermal and electrical performances has proven to be challenging. Unlocking the full potential of WBG semiconductor power electronics will hinge on solving these technological challenges at the package level.
In this presentation, the author presents an overview of *CITC* research activities on advanced packaging with a focus on packaging for power electronics and silver sintering solutions. An overview of the current state of silver sinter materials is provided. The performance and limitations of the materials are addressed. Beyond materials, methods used to investigate the performances and degradation will be covered as well as the thermomechanical simulations for predicting package reliability.

Biography
Edsger Smits received his Ph.D. with honors from the University of Groningen in the field of organic electronics. In 2009, he joined TNO/Holst Centre focusing oxide based thin film transistors for displays, flexible and stretchable sensors and electronics for bio-medical applications. In 2021 he become responsible for the “Power Packaging “ at CITC. Topics of interests include mini and micro led, laser transfer, flexible and stretchable electronics and power packaging.

Impulse Printing™: Enabling 3D Printed Interconnects for Volume Production

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Abstract
Impulse Printing™ is a brand new technology developed by Holst Centre that will bring unique 3D interconnect solutions to the back-end semiconductor and display market. High resolution structures can be printed over steps, gaps, and even wrapped around substrates at incredible speeds. For example, wrap-around printing of electrodes to create a back-to-front interconnect for µLED displays, or printing directly on silicon dies as an alternative to wire bonding. Off the shelf materials such solder paste, conductive adhesive, silver micron flake ink, copper nanoparticle ink and dielectric ink have already been printed successfully, showing compatibility with a wide range of viscosities and particles sizes. The unique capability of printing almost any materials onto any type of topology makes Impulse Printing™ suitable for quick adoption into existing production lines.

Biography
Program Lead experienced in developing novel printing technologies in the field of hybrid printed electronics. Responsible for defining the overall strategy and leading the execution of innovative technologies, including ultra-high resolution printing, laser-assisted transfer, 3D printed electronics and photonic soldering. Driven by innovation and determined to take concepts to full industrial implementation. Over 10 years of experience working in research and start-up environment across the U.S. and Europe.

The challenges in testing small and highly integrated devices in a massive parallel test system

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Abstract
The triumph of electronic components started in the 1950s with the introduction of semiconductor transistors. Since this time the content of electronics has risen significantly. Innovations in the semiconductor industry are supporting the megatrends like mobility car electrification including ADAS-systems, sensors, connectivity, and advanced security.

This trend drives demand for enhanced packaging concepts like system-in-package (SiP), SoC and heterogeneous integration, as well as optimized existing and new materials that support package miniaturization including pad size reduction, smaller pad to pad distance and thermal performance.

Time to market and cost are the main challenges for new electronic technologies that will be deployed in mass production.

This Presentation describes the development of a contactor for singulated, small WLCSP devices in massive parallelism test, supporting more than 200 contact sites. It considers different aspects which address the challenges of reliable and cost-efficient device testing. The active retracting technology in the contactor increases the reliability of processing the devices after test as well as supporting force-controlled device handling and methods of accurately aligning contactor probes to fine-pitch device pads or balls. It further addresses the cost-effectiveness by supporting highly parallel testing and performance monitoring over the entire lifetime to optimize maintenance intervals.by an integrated track and trace feature

The presentation will also review the thermal aspects of testing devices in a high parallelism environment.

This approach requires close cooperation with the Handler supplier in order to optimize the overall performance of the entire system

Biography
Markus Wagner is Engineering Manager of the Interface Solutions Group at Cohu and is based out of Kolbermoor, Germany. Markus graduated from the University of Rosenheim with a Diploma in Mechanical Engineering. He has been in the semiconductor final test environment more than 20 years with Cohu, a provider of semiconductor equipment and services for the back-end semiconductor manufacturing. Markus has held a number of management positions in engineering and product marketing and holds several patents for innovative contacting solutions. Over the years he has gained experience in integrating contactors solutions into MEMS and final test systems.