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Power Electronics

Advanced silicon devices - Applications and Trends

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Abstract
Switch mode power supplies for eg telecom and server applications show a continuous increase of efficiency over the last decade. Reviewing major conferences such as APEC or calls for funding creates the impression that progress in power electronics can only be brought by wide band-gap devices such as SiC- or GaN based power switches. This presentation will hence highlight how silicon based power devices are responding to these requirements. Choosing the right topology and control method helps to overcome material limitations. Typically these solutions require more complex control but offer the benefit of well-established technologies. Furthermore future generations will continue to push the boundaries of today devices to even better performance.

The presentation will take an unbiased view on silicon based power devices versus their wide band-gap fellows both from a device as well as application perspective.

Biografie
Dr. Gerald Deboy received the M.S. and Ph.D. degree from the Technical University Munich in 1991 and 1996 respectively. He joined Siemens Corporate Research and Development in 1992 and the Semiconductor Division of Siemens in 1995, which became Infineon Technologies later on, contributing mainly to optical investigation methods for ICs and power devices during this period. His research interests were later focused on the development of new device concepts for power electronics, especially the revolutionary COOLMOS(TM) technology. From 2004 onward he was heading the Technical marketing department for power semiconductors and ICs within the Infineon Technologies Austria AG. Since 2009 he is leading a business development group specializing in new fields for power electronics. He is a Sr. member of IEEE and has served as a member of the Technical Committee for Power Devices and Integrated Circuits within the Electron Device Society. He has authored and coauthored more than 70 papers in national and international journals including contributions to three student text books. He holds more than 60 granted international patents and has more applications pending.

The Influence of Repetitive UIS on Electrical Properties of Advanced Automotive Power Transistors

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Abstract
MOSFETs in automotive systems can be subjected to events of unclamped inductive switching (UIS) over the lifetime of their application [1-2]. UIS occurs when the MOSFET is connected to some kind of inductance (a lumped element or parasitic), and there is a rapid change in current [3-4]. When a power MOSFET is used in circuit application an unclamped inductive load or parasitic elements present an extremely stressful switching condition for the power MOSFET since all energy stored in the inductor during the on state is dumped directly into the device during its turn off, causing the impact ionization within which avalanche conduction is enabled. Repetitive avalanching to which device is subjected for several millions of pulses generates high concentrations of electron–hole pairs that become hot carriers (HC) and can be injected into the gate dielectric [5-6] . Main effects of hot carrier injection (HCI) are change of threshold voltage V_{TH}, drain-source leakage current I_{Dleak}, breakdown voltage V_{BR} and ON-resistance R_{ON}. These changes during the lifetime operation of the device pose considerably risks against the requirement of a long-term reliability of automotive power MOSFETs [7]. Three different types of automotive grade MOSFETS were used for investigations: vertical DMOS rated to 24 V and two Trench MOS transistors rated to 24 V and 90V. Degradation of capacitances C_{DG} and C_{in} was observed in all three types of structures. However degradation (shift) of *I-V* curves was observed only in Trench MOS devices. From analysis it is clear that DMOS transistors are less vulnerable to HCI in case of repetitive avalanching then Trench MOS devices and that breakdown voltage in modern high voltage Trench MOS devices is more affected by repetitive avalanching than in standard low voltage TrenchMOS devices. Dramatic decrease of breakdown voltage for 90V rated transistor from V_{BR} = 118V to V_{BR} = 98 V and increase of on-resistance for 200% was observed after 10^8 stress pulses.

Biografie
Dr. Juraj Marek, received his MSc. and PhD degrees in Electronics, both from Slovak University of Technology in Bratislava (STUBA), Slovakia, in 2007, and 2011, respectively. Since 2006 he is employed as a researcher at Institute of Electronics and Photonics. His main areas of expertise are oriented mainly to Si and GaN based semiconductor power devices characterization, TCAD modeling
and simulation, and analysis of energetic capability - UIS test. The results of his scientific work were published in 11 current content journals, several papers in peer reviewed journals and many international conference proceedings.

Innovative plating system for an embedded packaging concept of power modules.

M. Hörburger
Product Manager Semiconductor Advanced Packaging
Atotech Deutschland GmbH, Semiconductor Advanced Packaging, Berlin, Germany

Abstract
The current paper will explore some of the challenges of the growing power electronics market and how to overcome them with a novel approach to embedding packaging, using an innovative electroplating tool. Embedding technology refers to the integration of components (IGBTs, MOSFETs and dies) into PCB to build up a compact and dense package. Therefore the new plating system enables simultaneous double side Cu plating for improved efficiency and cost effective manufacturing, both of which are necessary to address the future requirements for power device manufacturing.

This work is part of Catrene's EMPower project that houses leading automotive suppliers (Continental, ST Microelectronics), PCB manufacturer (AT&S), technical universities, and Atotech as equipment and process supplier for semiconductor advanced packaging technologies.
The targets of the EMPower project are to lower costs and enable higher reliability and smaller form-factor, which are expected to have a potential impact of up to 10% on automobile manufacturing by 2035.

The paper presents the results of double sided Cu plating in terms of warpage, stress, uniformity and process time that have been successfully fulfilled, according to the specification of the EMPower project.

Biografie
Markus Hörburger
(Dipl. chem. oec.)

Product Management Advanced Semiconductor Packaging
2,5 years at Atotech Deutschland GmbH

Educational Background:
- University of Ulm
- Diploma in Business and Chemistry

Professional Background:
- Merck Millipore: Product Management – Strategic Process Development
- BASF SE: Strategic Business Development - Open Innovation
- Atotech Deutschland GmbH : Product Management Semiconductor Advanced Packaging - Processes and chemistry solutions for wafer level packaging technologies used for Power Chips, MEMS, Memory, Logic and others.

Comparison of electrothermal constraints on semiconductor power modules in photovoltaic DC/AC inverters

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Abstract
The semiconductor power modules using Silicon carbide SiC are used more often regarding their high switching speed, and in the case of a photovoltaic system, this will mean a more compact system and a cheaper one. The DC/AC inverter is the first component to fail, and only few studies exist on the reliability of this inverter, especially for the one using MOSFETs SiC power modules.
The junction temperature of the transistors and its variations with time accelerate the ageing of these modules.
This paper presents a comparative study between Si IGBTs, Si IGBTs with an anti-parallel SiC Schottky diode (hybrid IGBTs) and SiC MOSFETs with respect to the variations of the junction temperature of the semiconductor, in the case of a photovoltaic DC/AC inverter, and using a suitable heat sinker for each power module.
The estimation of these variations were done using the current measurements data issued from multiple photovoltaic power stations during several years.
Those measurements are used as an input for power losses estimation model coded with Matlab, then the resulting power losses are used to estimate the corresponding junction temperature using another Matlab model serving to estimate this temperature.
Rainflow counting algorithm and other methods are used to compare the variations of the junction temperature in the 3 cases, and to estimate the lifetime of these 3 power modules.
Results showed that the electrothermal coupling of the on-state resistor RdsON in the case of the MOSFET SiC has a positive effect on its lifetime in some conditions, and the same effect has the use of the anti-parallel Schottky diode in the case of the hybrid IGBT module.

Biografie
Biography:
Mouhannad Gabriel Dbeiss born in Tripoli Lebanon in 11/04/1991.
• 2009-2014: Graduated as an Electrical and Electronical Engineer (Industrial Informatics and Control) from The Lebanese University-Faculty of Engineering I, Tripoli Lebanon.
• 2013-2014: Research Masters in Reliability-Identification-Diagnostics (TSMI-FID) from Lebanese University, Tripoli Lebanon.
• 2014: Internship on Renewable Energy (Wind Turbine Generators) in UTC-Compiegne France.
• 2014-2015: Applications Engineer at National Instruments (NI), Middle East Branch, Beirut Lebanon.
• 2015-Present: PhD student at CEA-INES (French Alternative Energies and Atomic Energy Commission – National Institution of Solar Energy) and “Université Grenoble Alpes-INP-G2ELab”, working on Health Monitoring of Photovoltaic Inverters using SiC MOSFETs, Grenoble France.
• 2015-Present: Assistant Professor at “IUT- Université Grenoble Alpes” and “Polytechnique-Université Grenoble Alpes”, Grenoble, France.

1200 V double trench SiC MOSFETs technology and device reliability results

F. Filsecker
Application Engineer
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Abstract
The double trench MOSFET technology, featured in the new 3rd generation SiC MOSFETs from ROHM has already been introduced in previous conferences. A review of this structure and its main advantages compared to the traditional planar MOSFET structure will be outlined, including static and dynamic characteristics of both device types. It features a lower on-state resistance RDSon (from 8.5 mΩcm2 to 4.1 mΩcm^2 for 1200V devices) and lower turn-on losses (about 45% less).

The core of the presentation will be centered in reliability and robustness test results of this new device. For a discrete device operating at temperatures up to 175°C this comprises:

-Lifetime estimations in blocking state and of gate oxide

-Gate-Source threshold voltage shift (High temperature gate bias test for positive and negative VGS values)

-Body-diode reliability (DC and pulse test)

-High-humidity, high-temperature reverse bias test

-Avalanche ruggedness and typical breakdown voltage

-Short circuit withstand time

The results indicate that the 3rd gen. MOSFETs achieve a better performance than the previous one without compromising device reliability. However, due to the reduction of the on-state resistance RDSon, the short circuit saturation current is larger than in the previous generation. This leads to a reduced short circuit withstand time (5 ms), roughly 50% of the one achieved before.

Biografie
Felipe Filsecker was born in Viña del Mar, Chile. He received the Electrical Engineering degree from the Pontificia Universidad Católica de Valparaíso, Chile, in 2009. After this he worked in the Chair of Power Electronics of the Technische Universität Dresden, Germany, where he specialized in the area of characterization and application of high power semiconductor devices. Currently he is working as an application engineer at ROHM Semiconductor.

Silicon carbide 1200V and 650V Schottky rectifies with ruggedness and reliability comparable to silicon power products

A. Konstantinov
Design Engineer
Fairchild Semiconductor, Kista, Sweden

Abstract
Concerns for reliability are one of major roadblocks for widespread adoption of SiC high voltage power devices. In the talk we will present the new SiC Schottky-barrier diode (SBD) technology recently developed at Fairchild Semiconductor in order to meet or exceed the standards for reliability and ruggedness applied to high voltage silicon devices.

Inherent issues of SiC SBDs with reverse leakage and avalanche and surge-current ruggedness are overcome with optimized Junction-Blocked Schottky (JBS) rectifier design with improved Schottky-metal shielding. This not only suppresses high-temperature reverse currents but also improves SBD avalanche ruggedness. Very high mean specific avalanche energies have been achieved, 20 W/cm^2 for 650V rectifiers and 12 W/cm^2 for 1200V. No pronounced parameter drift upon repetitive avalanche or surge-current test occurs until the destructive energy is reached. Fairchild SiC SBDs are 100% avalanche-tested.

Some makes of SiC power devices are currently limiting the field lifetime of PV modules to 3 to 4 years because of anode corrosion. Excessive temperature-humidity-bias tests were performed with Fairchild SBDs and the corrosion acceleration factors due to temperature, humidity and bias were established. The new SBD technology was also compared to existing products. With the acceleration factors established we can expect the 1200V SBD anode corrosion time in PV modules be increased by a factor of 100.

The approach of Fairchild to manufacturing strategy is to entirely bypass 4” production. Production was started at a high-volume 6” silicon fab. Dedicated SiC-specific tools included a high temperature implanter and an implant anneal tool, while other tools are shared with silicon manufacturing. The combination of much larger size of 6” wafers with cost sharing between silicon and SiC manufacture has an important contribution to improved cost structure of SiC power devices at Fairchild.

Biografie
Andrei Konstantinov received the MS degree in electrical engineering from Department of Optoelectronics, St. Petersburg Electrotechnical University, St. Petersburg, Russia, in 1979, and the PhD degree in semiconductor physics from the Ioffe Institute, Russian Academy of Sciences, St. Petersburg, in 1984. Dr. Konstantinov was active in multiple semiconductor startups including AMDS/Intrinsic Semiconductor, Genesic and Transic AB. His research interests include silicon carbide device phenomena and device process technologies.

UV Laser thermal annealing: the enabling technology for vertical devices and 3D monolithic integration for power electronics, MEMS and alternative substrates.

F. Mazzamuto
Process Manager
SCREEN, LASSE, Gennevilliers, France

Abstract
In semiconductor, the age of 3D is expanding in all market segments. In power electronics, vertical devices have always exploited the 3rd dimension and most recently non-volatile memories migrated from planar to 3D-NAND in HVM. The same transition is proceeding in MEMS and advanced logic devices with the possibility of forming monolithic stacks at each level of logic and/or sensors.
One common bottleneck in this transition has been the temperature limitation in the manufacturing process of the top layer. For standard annealing techniques, this temperature is uniform inside the wafer and has a similar limitation (typically on the order of 500°C or less) to the ones in BEOL. SCREEN is providing a unique solution which is able to treat the top layer selectively and independently from the buried stack. Using UV laser annealing technology we are able to bypass all temperature limitations achieving a surface temperature at, or in excess of, the melting point of the silicon on the top layer but minimizing the annealing effect in buried layers and substrate.
In power electronics the efficacy of the approach has been demonstrated over a significant period of time for Si based devices, and now has extended to emerging SiC-based devices. Possible value has been shown for memory. In MEMS, the top sensitive layer can be formed without temperature limitation on top of buried CMOS technology. Finally, the surface localized annealing enables electronics on alternative substrates such as low-cost, flexible, organic plastic materials, often having poor robustness to high temperature.

Biografie
Electronic engineer and specialized in nanotechnology, Fulvio Mazzamuto started his career as researcher at Paris University XI. In 2008, fascinated by the interactions of multiple physics he started modeling and engineering the interactions between electrons, phonons and photons in emerging materials and devices. Starting his Ph.D. during the boom of two-dimensional materials, he applied his multi-physics experience to explore thermal and electrical transport in graphene nanoribbon, up to design the first graphene-based thermoelectric generator.

Obtained his Ph.D in 2011 in Paris University XI, he join EXCICO, company specialized in laser annealing system for semiconductor manufacturing process. He has been working two years as field application manager, for the adoption and the integration of laser anneal in manufacturing process of Si-based power device, backside CMOS illuminated sensor and MEMS.

In 2014 he started developing new processes solutions around laser annealing technology to open new market opportunities for LASSE, (former EXCICO), new subsidiary of SCREEN semiconductor group. Today he is deeply involved in power electronics for laser annealing integration in next generation devices, including Si-based, but especially the emerging SiC and GaN-based devices.

Fast high yield dicing of 4 and 6 inch SiC-wafer

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Market Development Manager
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Abstract
The paper will present details on current evaluation results for TLS-Dicing™ for SiC wafers. After development of the basic principle [Lewke, et al., 2014] and the demonstration of high separation quality [Dohnke, et al., 2015] current work is focused on yield improvement. First we investigated the influence of structures inside dicing street on the TLS process. These results we applied to thin 100 mm SiC wafers and observed very high geometrical yield of 96%. Finally we also tested comparable 150 mm wafer. Additional bending strength evaluations of the diced chips are currently in progress and results will be presented during the presentation.
TLS-Dicing™ is a kerf free laser based separation technology. A controlled crack is guided through brittle material like SiC or Silicon using thermally induced mechanical stress. Resulting separation quality of backside metallization layers and chip's side wall is very high. For higher separation straightness an additional shallow continuous surface scribe was used. In order to improve yield the influence of metal structures inside the dicing street to the scribe process was investigated. Therefore two different laser wave lengths were tested. Besides the influence of metal structures on the scribe process minimization of particles and heat affected zones in combination with high straightness of the TLS separation was in focus of this evaluation. A stable parameter field with constant energy input per unit length could be described as base for optimal cleaving results.
After a short overview on the basic principles and the technology, the presentation will focus on results of the laser scribe investigations, the current application results for SiC-dicing and achieved performance indicator values like yield, throughput and chip quality. Observed potential risks of yield loss will be discussed and transferred in design rules and best practice based dicing rules.

Biografie
Dr. Hans-Ulrich Zuehlke works as Marked Development Manager Semiconductor at 3D-Micromac AG. He joint 3D-Micromac in January 2014. After studying scientific instrument engineering he received his PhD in the field of computer architectures.
Since twenty years H.-U. Zühlke is active in the field of laser processing tools, last ten years with a focus on laser processes for the semiconductor and PV industry.

Si, SiC or GaN: technology and cost comparison

E. Barbarini
Senior Cost Engineer
System Plus Consulting, Nantes, France

Abstract
The presentation proposes an overview of the latest innovations in power devices showing the differences of Si, SiC and GaN transistors from the technical and economical point of view.

The objective of the presentation is to define which are the cost drivers of the new technologies in power devices, understand the reason of the success of the different technologies for different application and estimate a cost evolution.
Different devices have been opened and analyzed to understand the different technology innovations and a breakdown cost analysis of the manufacturing process has been developed.
The presentation includes deep technical analysis of technology supported by optical and SEM pictures. The cost analysis are the results of description of production process and software calculation of all the parameters which have an impact on final manufacturing cost.

Silicon transistors are well established devices which will still have a future: in the latest years the improvement of manufacturing process and decreased production cost will drive toward a standardization and popularization of these devices.
Starting from 2010 new products are entering the market to compete with silicon: SiC MOSFETs and GaN on Si HEMT are one of them.
SiC is a good candidate for high power devices of 1200V and more while GaN on Si HEMT offers new capabilities, such as the possibility to work at higher frequencies.
But from the cost point of view it is still not appealing on the market. A single SiC component could reach a price almost 5 times higher than a standard Silicon transistor and on GaN devices the presence of a GaN epitaxial structure can double the final wafer manufacturing steps cost.
To conclude GaN and SiC are the good candidates to enter the respective power devices sector but at the same time their cost will be the factor which will define their effective application.

Biografie
After a bachelor’s degree in Electronic Engineer from Politecnico di Torino, Elena obtained a master's degree in Nanotechnologies for the ICT from Politecnico di Torino, EPF Lausanne and INP Grenoble. Subsequently she got a PhD in Electronic Devices in collaboration with Vishay Semiconductors.
After some years in Italy, where she had different significant experience in research and manufacturing of electronics components, she moves to France.
Elena is actually Senior Cost Engineer at System Plus Consulting where she in charge of the Power Electronics division.

200-mm G-FET™ GaN-On-Silicon power switch enabling new generation of power converter applications

F. Letertre
COO & Co founder
Exagan, Grenoble, France

Abstract
GaN-on-Silicon power devices are recognized as a key technology to sustain future power converter systems roadmaps in the field of IT electronics, renewable solar and emission free automotive applications. Exagan is implementing proprietary G-Stack™ 200-mm's GaN-on-Silicon and G-FET™ technologies into high volume production to enable higher integration and improved efficiency. The advantage of its unique expertise in GaN-on-silicon material fabrication while leveraging on its attractive fab-lite business model, allows Exagan to provide GaN-on-Silicon power switches solutions to meet future market performance, reliability and cost targets. This paper will present the latest developments achieved and potential products to be released.

Biografie
Fabrice Letertre received engineering degree from INPG-ENSPG with specialization in semiconductor materials, technology and devices, Grenoble, France in 1995. He joined CEA-LETI in 1995 in the Silicon-On-Insulator (SOI) material department and Soitec in 1998 where he held various R&D management and project leader positions. From 2009 to 2003, he was responsible, as Soitec group VP R&D, of managing Soitec's strategic projects portfolio including GaN, III-V and advanced SOI activities. In 2014, he co-founded Exagan with the aim to develop a leading European source of GaN power switches based on Exagan proprietary 200 mm GaN-on-Silicon technology, for power conversion applications. He holds more than 60 patents and has co-authored more than 40 technical papers.

GaN-Si MOCVD advancements from Single Wafer Reactor technology for improved power device performance

R. Morgan
Product Lead
Veeco, Marketing, Somerset, United States

Abstract
Continued growth in mid and high voltage applications in consumer power supplies, alternative energy and data centers are requiring improved power efficiency, operating frequencies and system size reductions. GaN devices are being introduced in market at a higher pace, that deliver on these parameters over traditional Si devices. In order to produce these devices in volume at yield, reliability and cost targets, GaN-Si MOCVD is required for the next generation. The MOCVD process now has to deliver superior film quality with a tight run to run control, low defectivity and high uptime. In response to these high volume production requirements, Veeco has developed the next generation MOCVD system based on single wafer architecture that has demonstrated industry leading performance at multiple customers. In this talk we will discuss the latest results as relevant to high volume production requirements.

Biografie
Ray Morgan is a Lead Product Marketer in the MOCVD business unit at Veeco Instruments, focused in the GaN on Si power segments. With more than 13 years of industry experience at ON Semiconductor, Texas Instruments and NXP, he has held marketing, product and engineering positions. Ray earned his bachelors of science in electrical engineering from Arizona State University with a focus on semiconductors and an Executive MBA from Thunderbird School of Global Management. He can be contacted at rmorgan@veeco.com.

600V MISHEMT recessed gate technology at CEA, LETI

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reserchear
CEA, LETI, DCOS /SCPE, Grenoble, France

Abstract
Wide bandgap materials have demonstrated a great potential in high-power electronics due to their high device breakdown voltage and high current density, which are two key parameters industrial motors and electrical vehicles. Recent improvements in the growth of wide bandgap semiconductor materials provide the opportunity now to design and fabricate transistors that demonstrate performance in terms of low on-resistance and capability to work at high temperature.
We have implemented a 600V enhancement mode AlGaN/GaN high mobility transistor with a fully CMOS compatible technology using a silicon substrate.
To guarantee the safety of systems in off-mode a U shape recessed gate was employed to cut the 2DEG. The GaN-based recessed MIS-gate structure in conjunction with a P doped GaN layer located under the gate allows to achieve positive threshold voltage. The low on-state resistance is maintained by the 2-D electron gas remaining in the channel (and low access resistances) except for the recessed MIS-gate region. The desired device breakdown voltage was achieved with the addition of several gate, source and drain field plates.
This 600V transistor exhibits a threshold voltage close to 1V and specific resistance lower than 6 mohm.cm².
The main advantage of wide band gap devices is that they can be operated at temperatures above 150°C. If we consider that interest of wide band gap devices like GaN/Si HEMT is the low Ron resistance, they should be the best candidates for power applications.
We used room-temperature 2DEG density ns to extract the electron mobility. The reduction in µch with decreasing value of ns was usually explained by polar-optical-phonon scattering, ionized impurities and trapped charges in or close to the 2DEG. We have measured the electrical characteristics of Leti's Hemt in temperature up to 175°C. In addition to static measurements, we will present and discuss dynamic Ron behavior of this device in temperature.

Biografie
Rene ESCOFFIER, engineer of research entered the CEA-LETI in 2010 in the wide bandgap component technology laboratory. He worked in the modelling of components from 1992 till 1998 then joined the Motorola Company until 2004 to design structures for the safety of integrated circuits. He specialized himself for the Freescale company (2004-2010), in the design and the test of power components from the chip to its integration into module. He is now a project leader of power module optimizations in terms of cost and electric efficiency and their use in battery-driven vehicles.

Packaging Technologies for Power Microtransformer Devices

D. Dinulovic
Senior Project Manager
Würth Elektronik eiSos GmbH & Co. KG, R & D,
Garching, Germany

Abstract
Recent developments in power electronics are driven by two major trends: increasing power density and higher level of integration (eg. power system in package).

As a consequence the requirements on power magnetic components (transformers, inductors) are tremendously changing. Device size, profile height and inductance value has to be reduced while switching frequency increases.
This requires not only the further development of magnetic materials but also new packaging concepts for passive components to shrink devices size and profile height, reduce parasitics and enable the integration into power system in package solutions.

New developments in the field of passive power devices are focused on miniaturization and on integration. Power inductors and transformers should provide smaller inductance and smaller size. Decreasing of the inductance value causes the decreasing of the device size and profile height.
Thin-film technology shows good potential to fulfill all of these requirements on power devices. New kinds of micro power devices are aired in many research works developed and tested at high switching frequencies, but the development of adequate packaging technology for micro magnetic devices is still open issue.
In our work we will show the implementation of two packaging technologies applied on housing of power microtransformer device.
As first option a BGA (ball grid array) type package was developed using a wafer level packaging technology (eWLB: embedded wafer level ball grid array).
Alternatively investigations on a LGA (land grid array) type package were conducted using embedding technology based on FR4 laminate.

The feasibility study of both technologies show good results and based on requirements, these technologies can be applied to the packaging of power micro magnetic devices.

Biografie
Dr.-Ing. Dragan Dinulovic (m) studied precision engineering at University of Nis (Serbia). He received his PhD from Leibniz Universität Hannover on microtechnology and MEMS in Year 2007. From 2000 to 2010 he did research at Instuute for Microtechnology (imt) in Hannover. His research area was a development of magnetic MEMS devices.In 2010 Dragan jointed Würth Elektronik eiSos as R&D engineer, where he focusses now on development of thin-film passive components, on integration of passive and active power devices into one package (Power System in Package (PSiP)) or on chip (Power System on Chip (PwrSoC)), and on Energy Harvesting devices. He is author of more than 30 papers.

Automated 3kV Wafer Level Testing

A. PRONIN
Lead Applications Engineer
Keithley Instruments, Applications, Solon, United States

Abstract
Due to the complexities typically associated with high voltage (HV) wafer-level testing — such as instrumentation setup, cabling, probing, automation, and safety — on-wafer HV testing is usually limited to characterization labs or manual benchtop setups that are separate from a fab's standard production workflow. This paper gives practical examples on how to plan for very high voltage wafer testing, as well as implementation details on how to integrate high voltage testing in a production environment.
Keithley has developed several measurement techniques and approaches that enable automated HV wafer level characterization on multiple pins without sacrificing low voltage performance or throughput requirements. These techniques include integration methods that allow sensitive transistor characterization and low current leakage tests to run in the same process flow as HV breakdown and HV capacitance tests. For example, in one automated test sequence we first measure the transistor Ioff current in the pA range and the threshold voltage Vth. Next, we measure the drain current Ion when both the gate and drain are biased above 1kV. Then, we perform capacitance measurements with a 2kV bias level. Last, we run breakdown tests at 3kV levels.
Keithley has also developed a run-time open/short/load impedance compensation technique that enables accurate HV capacitance measurements on-wafer. We will explore these and other HV measurement issues, as well as share our results and experiences in the developing field of HV wafer-level testing.

Biografie
Alexander Pronin is a lead applications engineer at Keithley Instruments. He received his PhD in material science from Dartmouth College. Alex has been with Keithley for over 20 years and has been involved in the definition, development, and support of various projects in test and measurement, including wafer level reliability (WLR) packages, characterization techniques of various non-volatile memory (NVM) devices, and integration of RF S-parameter testing with wafer level process control monitoring (PCM) using Keithley parametric test systems. His recent interests are in the field of HV testing.

Universal pin architecture for efficient test of power analog ICs

T. Dirscherl
Product Manager Power and Analog
Advantest Europe GmbH, Amerang, Germany

Abstract
With the introduction of the high density 64 channel AVI64, the V93000 single scalable platform has added a new member to its universal pin card portfolio that is tailored to the power and analog device test market.
This new module covers diverse applications in the emerging IoT sector, sensor and power management, embedded power and automotive markets.
The presentation will demonstrate the flexible usage of the new AVI64 universal analog pin for a wide range of applications based on real world examples. To name a few:
• Shrinking supply voltages for extended battery life in the mobile market are driving the need for precision trimming of power management devices in the <100µV area.
• SmartDevices for latest charger technologies and sensors are requiring proprietary protocols based on Vcc modulated digital I/O schemes.
• Efficient battery management technologies are driving the need towards higher voltages and precise voltage measurement capabilities.
All of that can be addressed by a single, efficient instrument - The AVI64 universal analog pin
• Per-pin high precision, high voltage VI for Sensors, SmartDevices, PMIC test
• Per-pin AWG & Digitizer for embedded AD/DA testing, threshold searches for a diverse applications and stimulus for sensor applications
• Per-pin high voltage digital I/O for sensors, automotive / industrial interfaces
• Per-pin high voltage TMU for a wide range of timing measurements in the power/analog domain
• Floating high-current unit + differential voltmeter + internal matrix for typical power tests like RDSON, current limit tests for embedded power, automotive, industrial and power management applications
The integration of this rich feature set within a single module is key for lean cost effective configurations and simplifies the standardization within the installed tester fleet to maximize utilization. Further test cost reduction is seen by its capability to increase site counts due the extremely high channel density of the AVI64.

Biografie
Toni Dirscherl holds a degree as Electronic Engineer from the University of Applied Science in Munich, Germany and joined SZ Testsysteme as Development Engineer for Analog DSP frontends in 1997. After serving 3 year as Senior Application Engineer for SZ Inc and Credence in San Jose/California from 2001 to 2003, Toni Dirscherl took over the position as Product Marketing Engineer for Credence-SZ GmbH. Since the acquisition of Credence-SZ by Advantest Europe in 2008, Toni Dirscherl acts as the Product Manager for Advantest’s Analog and Power Solutions. He has published numerous articles.

Affordable isolated DC current measurement based on optocouplers

S. Geissmann
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Switzerland

Abstract
n high voltage reliability tests (HTRB, THB HVDC, ..) the devices under test (DUT) are subjected to a high voltage (usually 80..100% of VCEmax) for a prolonged period of time. Since the DUTs are connected in parallel a failure of one DUT would remove the voltage stress from the other DUTs. To prevent this a common solution is to put a (rather expensive) fuse in series with the DUT. Those fuses could be replaced by relays, but for this the leakage current of each DUT needs to be monitored. Monitoring each channel individually and making it switchable also brings additional benefits like being able to measuring VI-Curve of each element.
Since the leakage current is in the mA-range and DC, common decoupled solutions do not work. One approach would be to introduce a shunt resistor and isolate the ADC. This solution is rather expensive as it requires isolated voltage supplies for the ADC.

The solution presented here is based on a current mirror realized with two optocouplers.The use of optocoupler replaces the resistor with a diode. This change makes the circuit robust against pulse currents. This pulse currents will occur when a DUT is connected to the DC source. With a resistor this would result in an over voltage which could damage the ADC.
This paper presents the findings of using this circuit for measuring leakage currents in a new reliability test setup and the changes which had to be made.

Biografie
After doing a four year apprentice ship at ABB Silvan Geissmann studied Electronic Engineer at the FHNW in Brugg. He then started working in 2007 at ABB Semiconductors in Lenzburg. In 2008 he started a Master of Science in Engineering which he finished in 2011.