Advanced Packaging Conference

Role of Packaging Enabling High Performance Devices

R. Puhakka
President
VLSI Research, San Jose, United States

VLSIresearch

Abstract
Role of semiconductor packaging is rapidly changing as it enables technology and cost advancements in modern high performance computing devices, such as GPUs, MPUs, FPGAs. This is huge technology and market inflection point is impacting Foundries, IDMs, OSATs, Equipment and Materials suppliers. The presentation explores the opportunities created by these inflection points in packaging and how industry stakeholders are impacted.

Biography
Risto Puhakka is President of VLSIresearch, leading the company's commercial operations and market research activities. He is an expert in Semiconductor Capital Equipment markets as well as Semiconductor Manufacturing. Risto advises managers, boards, and investors about semiconductor market trends and strategic industry statistics. He is a regularly invited speaker at conferences about various topics in semiconductor manufacturing and equipment markets.

Risto is a graduate of Helsinki University of Technology (MSc) and UC Berkeley, Haas School of Business (MBA). When Risto is not working he cherishes time with his family, runs very long distances, and is occasionally spotted flying model airplanes.

From SoC to Chiplets: Harnessing the X-Dimension of Fan-Out Packaging

R. Antonicelli
Director, Field Applications Engineering
JCET, Lausanne, Switzerland

Abstract
The increasing demand for high bandwidth memories and powerful cores require new and cost-effective solutions to achieve flexible and scalable system integration.
The semiconductor industry is moving from large, complex and costly single-chips (SoC) strategy towards multiple, integrated and hybrid functional blocks (chiplets) interconnected in diverse, heterogeneous ways.Roberto Antonicelli (MSEE, PhD)
Director, Automotive BU

Biography
Roberto Antonicelli is a professional with over 20 years of experience in the semiconductor industry. At JCET (formerly STATS ChipPAC) he drives Automotive Business Development for US, Europe and Middle-East. Prior to joining STATS ChipPAC in 2010, he has held diverse R&D positions at Infineon Technologies, Alcatel Microelectronics and ST Microelectronics. Roberto obtained his MSEE and PhD from Polytechnic University of Bari, Italy, respectively in 1997 and 2002. Roberto lives in France together with his wife and their three children.

A multi-dimensional approach, combined with fine pitch flip-chip and ultra-high-density fan-out processes, may represent a valid solution to achieve extreme levels of integration and significant cost-savings.

Heterogeneous IC Packaging for Advanced AI Applications

F. Roa
Sr. Director fcCSP / fpfcCSP / PoP Products
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Abstract
Data centers, located in nondescript ultra-large-scale buildings where electric power is more affordable, are the backbone of the data processing and AI training done today. With tens of thousands of high-end central processing units (CPUs) and advanced AI accelerators, these intricate cities of electronics require thousands of kilometers of copper connectivity and megawatts of cooling. Advanced IC packaging trends in the data center are driven by requirements for high memory bandwidth (BW), many-core CPUs and ultrafast networking between racks, servers and storage. The resulting packaging solutions are focused around three key areas: on-package memory for maximum memory BW and capacity as required by AI accelerators; larger-than-reticle-size compute processors for servers; and ever-faster networking devices pushing towards 50 terabits per second (Tb/s) switch capabilities. This three-fold powerhouse of compute and storage, AI acceleration and ultrafast networks to connect discrete functions are pushing advanced IC packaging to the limit. Single IC packaging solutions are still present but are quickly being supplanted by heterogeneous packaging solutions which are required to enable functional performance increases commensurate with demand. IC packaging such as 2.5D silicon-based interposer and high bandwidth memory (HBM) are commonplace as AI accelerators and high-performance switches and routers. Trends in CPUs towards more and more cores to enable fine-grain utilization of this immense resource in the data center has pushed the required gate limit far beyond what can be captured in a single reticle using conventional physical partitioning on a single system on chip (SoC). These compute cores need the highest performance silicon transistors possible and are some of the first products into the latest silicon node. To make room for this compute gate count, high-speed I/Os are being pushed off-chip into discrete I/O chiplets. In addition, the total power requirements and shrinking operating voltages have pushed input current levels to new highs, bringing electromagnetic interference (EMI) considerations back under the microscope, as well as putting local voltage regulation into the package to better contain the incoming current levels.

Biography
Fernando joined Amkor in 2007, and is responsible for advanced packaging development and commercialization. Prior to joining Amkor, Fernando worked for Intel in assembly process development and platform integration. Fernando holds a degree in chemical engineering from Universidad Nacional de Colombia, a Management of Technology degree from Colorado School of Mines and a Ph.D. in chemical engineering from University of Colorado.

Automotive semiconductor packaging and testing: a paradigm shift to innovation

C. Patel
NPI Packaging Group Manager
Presto Engineering, Meyreuil, France

Abstract
With no two package designs being alike, developing today's complex semiconductor packages requires experienced package engineers, state-of the art facilities as well as a strong network of highly skilled partners, including a strong day-to-day collaboration with leading EDA software companies.
In automotive, the tremendous acceleration of innovation (29% of total cost of vehicles expected to be made of electronics in 2030) leads to deep changes in the way of this industry dealt with semiconductor transitioning from commodity adoption of mature technologies to differentiation by disruption.
This differentiation comes as a paradigm shift along very specific requirement such as bill of material, non-standard form factor for our industries, or heterogeneous system in package. Especially EV vehicles and ADAS enabled vehicles demand now packaging able to pass AECQ100/AECQ103 standard with unique property, be integrated into chassis and bodies with extreme operating conditions and while reliability guaranteed. Regarding quality not only the use of new processes or new bill of material requires specifics, out of the standard semiconductor type of qualification plan, but also test coverage for 0 ppm targets.
The presentation will touch specific new challenges which assembly and test of automotive ASICs needs to tackle though use cases of automotive high current sensors for battery inverter control, integrated radars and LiDAR, from package integration of heterogeneous materials, thermal flow in advanced grid array packages, and optoelectronics modules.

Biography
Claire Patel is NPI Packaging Group Manager for PRESTO Engineering Group, which is a recognized expert in ASIC design and semiconductor services, from design to test and qualification to production.
Claire is working as Packaging Engineer with over 10 years on large package offer (QFN, SOIC, WLCSP, BGA, SIP,..) from automotive to consumer products, passing by industrial until spatial products.
She obtained an Double Engineering graduate from Polytech'Grenoble (France) and Polytechnic School of Montreal (Canada).

New Material Development for Advanced Packaging

K. Arnold
Chief Development Officer
Brewer Science, Wafer Level Packaging Materials,
Rolla, United States

Abstract
Today's consumer electronics and high-performance computing needs are dictating many of the changes that are being made within the advanced packaging arena. Advantages of decreased form factor of devices and increased interconnect density to enable better performance and lower costs to consumers are just a few of the justifications for continually modifying the packaging architecture. With package architecture changes comes the need for high-performance materials. A few process flow examples with material need are detailed below.
Two principal approaches to manufacturing fan-out wafer-level packaging (FOWLP) components have evolved: chip-first and chip-last, which refer to the point in the process flow where the chips are attached and over-molded in the package. Chip-first applications hold a majority of the FOWLP market space and have many specific process flows. The die attachment process for FOWLP is a very common and critical operation in advanced packaging, which presents many challenges and requirements depending on which process flow is chosen.
In the chip-first fan-out wafer-level packaging, the die is placed on a substrate with tape or adhesive on the carrier or by using die attach film. It is imperative to have accurate placement of the chip and minimize die shift during the molding process. The requirements for most applications require a "zero" die shift performance, especially for applications such as multiple die stacking for memory devices. These particular devices will be ground much thinner than 50 µm, and the die attach process not only needs to be accurate without shift, but must resist any deformation to avoid bump damage. Below is an image showing die shift performance after the mold process utilizing a novel material to meet the need for different die attach applications.
We have been able to demonstrate less than 2 micron die shift across the wafer after mold processing given the size and distance of the die portrayed above. Work continues in this area with the goal to be less than 1 micron die shift across the wafer.
Another process that has required new material solutions is collective die transfer for hybrid bonding. In this process, die are collected on a carrier, similar to the chip-first FOWLP process. But in this process flow, after the die are all placed the carrier, the carrier is flipped over so the die can be aligned with the target wafer. Alignment in this process flow is critical. Die shift cannot be tolerated as the wafer will next undergo a hybrid bonding process. After the hybrid bonding process is complete, the carrier will be removed. Material requirements to enable this process are stringent. These requirements include: room temperature die bonding, no die damage during debonding, front-end-of-line cleaning requirement for die that subsequently need to be hybrid bonded, 100% die transfer without shift, and compatibility with CMP. This process has been demonstrated with 99% successful die transfer to the target wafer.

Brewer Science has developed novel materials to meet the need for different die attach applications. In this talk, we will focus on demonstrating the performance of our newly developed materials, which assist in successfully grinding device wafers to ≤20 µm and enabling die attach with minimal to "zero" die shift without bump damage and collective die transfer processes. We will explain how the materials work and provide

successful examples.

Biography
Coming soon

Advanced Materials and Interconnection Technologies for Highly Miniaturized IoT Modules

M. Martina
Head of Strategy
Micro Systems Technologies, Berlin, Germany

Abstract
Standardization of semiconductor packaging and interconnection technology is a key aspect to allow for large scale manufacturing and commercialization. However, to achieve maximum performance and higher integration density allowing for smallest form-factors, precisely tailored solutions and the application of novel and unconventional materials and interconnection concepts must be chosen, while manufacturability needs to be preserved.
In the first part of this work, novel materials, assembly, interconnect, and packaging processes were developed, which can be combined to realize highly miniaturized, hermetic IoT devices.
Applying this toolbox, a technology platform to manufacture customized Systems-in-Package (SiP) for IoT applications was developed. The base components are integrated in a SiP with through-package-via (TPV) interconnections and are soldered to an advanced flexible substrate. On top of the SiP, a second interconnection substrate with a customizable sensor configuration can be attached. On the bottom level, the flexible substrate allows for several additional system components to be attached. In a final step, the whole system can be miniaturized or custom-shaped by folding the substrate into the desired form factor.
To realize advanced flexible substrates, novel processes to structure and manufacture liquid crystal polymer (LCP) circuits were developed. Resulting, flexible LCP substrate with lines/spaces down to 15/15 µm were achieved which offer flexibility for folding, biocompatibility, and chemical inertness. Notably, a special lamination process was developed which allows to encapsulate copper traces as well as to embed semiconductors and passives inside the LCP substrate without forming interfaces as it is the case with bond sheets. Resulting, hermeticity could be achieved while drastically increasing reliability. Furthermore, LCP offers low radio-frequency dielectric losses and a stable dielectric constant.
A miniaturized IoT-Module with a volume of only 1.3 cm³, a broad range of sensors including a microphone and electrochemical measurements, in a hermetic housing with electrical feedthroughs in LTCC, with wireless charging and an IoT-SiP was designed and manufactured to demonstrate this packaging approach. The module can be connected to any smartphone via Bluetooth Low Energy (BLE) and allows to monitor temperature, pressure, sound, impedance, illumination, position, and acceleration even under harsh environments and in liquids.

Biography
Manuel Martina received the B.Sc. degree in physics from RWTH Aachen University, Aachen, Germany, in 2011, the M.Sc. degree in physics as well as the Ph.D. degree for his work in near-field optics and microfabrication/nanofabrication from the Eberhard Karls University of Tübingen, Tübingen, Germany, in 2014 and 2017, respectively.
He worked as a Researcher in several fields of microsystems technology and on the interface to biology with the Natural and Medical Sciences Institute, Reutlingen, Germany. From 2017 on, he was working as Manager of Next-Generation Products with the Research and Development Department at Schweizer Electronic AG, Schramberg, Germany. His research included semiconductor embedding and packaging in

high-end printed circuit boards for future automotive radar and industrial 5G applications, and for future power electronics. Since 2021, he is working at Micro Systems Technologies in the fields of advanced semiconductor packaging and packaging substrates.

Thin Cu Plate-able Dielectric Material Developments for RF and Power Device Miniaturization

R. de Wit
Business Development Manager EMEA
Henkel Electronic Materials, Westerlo, Belgium

Abstract
Smart Electronics' market trends like 5G, 6G and ADAS are driving advanced semiconductor packaging innovations towards higher functionality, enhanced connectivity at higher frequencies, RF signal interference isolation (shielding), smaller form factors (miniaturization) and reduced power consumption. To meet these future demands, semiconductor package designs continue to evolve towards challenging System-in-Package, Antenna-in/on-Package and Wafer Level architectures. Especially for next generation RF and Power devices, antennas and radars, the thermo-mechanical, thermal resistance and (di)electric properties of the assembly and packaging materials play a key role as well as fast and low temperature processing/curing. Exploring development work together with laser specialist LPKF last year resulted in a new SVHC free and low warpage Liquid Compression Molding (LCM) encapsulant suitable for Laser Direct Structuring. Deposition of 25/25um L/S Cu tracks and Cu plating of blind vias down to 50um have been demonstrated as presented during Advanced Packaging Forum in February this year. This APC presentation will cover further product development and test work together with LPKF on a new STENCIL PRINTABLE encapsulant aiming for <50um thin dielectric layers with 15/15um L/S Cu tracks and <50um Cu plated blind vias. Next to more functionality in same or even smaller package footprint, this "direct and additive Cu formation" technology can also deliver significant cost savings by introducing only three back-end approved processing steps of molding, lasering and plating (vs typically seven costly and time-consuming semi-additive processing steps like seed layer sputtering, masking, lithography, development, Cu plating, mask removal and flash etching).

Biography
Ruud de Wit is responsible for managing Henkel's Semiconductor, Sensor & Consumer Electronics Assembly Materials business development within EMEA region. Ruud has a BSc degree in Mechanical Engineering followed by several polymer, sales and marketing courses. Ruud is working for Henkel since 1990 in multiple positions including technical customer support, quality assurance and engineering, and global semiconductor account and product management. Last couple of years, Ruud's main focus is on exploring and driving new semiconductor packaging material development needs within Henkel to enable potential customers to design smaller RF and Power devices.

Die-Attach Bonding with Copper Metal Pigment Flakes

G. Elger
Professor for Manufacturing Technologies of Electronics
Technische Hochschule Ingolstadt, Institute for Innovative Mobility, Ingolstadt, Germany

Abstract
Solid state sintering has emerged as a preferred die-attach process of choice for high temperature applications due to the formation of near bulk like interconnects which are capable of providing high temperature operations. Ag sintering under pressure is an industrialized process today. However, low cost alternatives, which offer comparable or better results under the same processing parameters, are desired. Among all metals Cu offers the next best thermal conductivity to Ag, is easily available, recyclable and the raw material cost are a fraction of that of Ag. Therefore, in recent years, focus has shifted to develop Cu sintering as a reliable alternative to the industrialized Ag sintering processes. However, Cu is highly prone to oxidation and the build-up of oxide layers is a diffusion barrier against material transport during sintering. We propose a novel approach by the use of micro-scale (3-5 µm), thin (200 nm) and high surface area (3.5 m²/g) Cu metal pigment flakes from Schlenk Metallic Pigments GmbH. Due to their design, the flakes stack over each other. This results in a dense and homogenous interconnect with a shear strength of ~ 40 MPa, while sintering under pressure of 10 MPa at 275 °C for 5 min. Since the flakes stack over one another, the overall surface area in contact is increased, thereby enhancing sintering. The stearic acid coating on the flakes, introduced during the ball milling process to prevent cold welding of the flakes is observed to be not only effective in preventing oxidation of the flakes, but also avoids agglomeration of the flakes during paste formulation and enabling excellent stencil printing capabilities.
The effective stacking of the flakes also allows for sintering under low bonding pressure and realizing a well sintered interconnect even with a solids content of only 60 wt% in the paste formulation, compared to commercially available Ag sinter pastes with ~90 wt% solids content. A simple two-step sintering process similar to industrialized Ag sinter processes is realized, including pre-drying at 120 °C followed by isothermal sintering at 275 °C in an open bond chamber. The use of PEG600 in the paste formulation allows for an in-situ reduction of Cu oxides.
The paste therefore offers an attractive low cost alternative to Ag sintering in die-attach bonding applications and can be introduced in the same equipment as presently used for Ag sintering under pressure.

Biography
Gordon Elger studied physics and made his PhD 1998 at the Free University of Berlin.
Afterwards, he worked at Fraunhofer-IZM, Hymite GmbH, Electrolux and Philips GmbH in the field of optoelectronic, LED, MEMS, high frequency packaging and CAE, e.g. FEM and CFD for structural analysis and heat management.
Since 2013 he is professor at the University of Applied Science in Ingolstadt (THI) for electronic manufacturing technologies and has built up a research team within the Institute of Innovative Mobility of the THI.

Gordon Elger's research is focused on microelectronics packaging and reliability, e.g. optoelectronic, sensor and power electronic packaging for automotive applications. One focus is the development of first and second level interconnects, e.g. residual free solder processes, new materials and processes for sintering. Another focus is the development of nondestructive measurement and test methods for reliability and quality insurance of interconnects, e.g. an automated transient thermal impedance tester for LED and power electronic devices. His research teams performs reliability analysis of interconnects and electronic modules. Based on the experimental data, models to predict the remaining useful life of interconnects are developed using physical "White Box" modelling (FEM) and data driven "Black Box" approaches.

Since 2020 Gordon Elger is in addition head of the new founded Applied Research Center for “Connected Mobility and Infrastructure” of the Fraunhofer IVI. Sensor data fusion, smart electronic applications, condition monitoring and artificial intelligence based algorithm development for predictive health management are a second field of research within present projects of the new founded Applied Research Center.

Thin Glass for Wafer- And Panel- Level Packaging: On the Route Towards Industrialization

T. Gotschke
senior project manager
Schott AG, Reseach and Development, Mainz, Germany

Abstract
With the development of semiconductor technologies, glass wafers are getting more important as a carrier material for temporary bonding with silicon wafers in semiconductor applications such as 3D IC, RF IC Packaging and Fan-out Wafer Level Packaging. We discuss glass carrier wafer products with unique properties: (i) an extremely low TTV < 0.6 µm along with low flatness that ensures almost no warping or bowing of the glass in the application. (ii) The broad coefficient of thermal expansion (CTE) range from 3.2 to $9.4x10^{-6}$ /K can match Si but can also be closer to higher CTE materials like epoxy molds and metal layers. (iii) Excellent UV transmission enables highly effective laser debonding, e.g. 1.1mm thick Borofloat 33 HT has a transmission >60% at 248nm and >90% at 307nm. Upon the latest breakthrough of glass and related processing technologies, our glass carriers enable the miniaturization of manufacturing in both front-end and back-end processes of semiconductors.

Glasses can be also used as core substrate for panel- and/or wafer-level packaging to achieve heterogeneous integration in increasingly complex packages. Glass has a large number of advantages: The stiffness of glass (iv) allows manufacturing of highly accurate buildup layers with manufacturing precision of 1µm and below. Special glasses can be made with very good dielectric properties (v) and can also be applied in antenna-in-package applications. But most of all, economic glass structuring techniques (vi) which can provide millions of vias and thousands of cut-outs in a glass panel are important and are being developed. SCHOTT's Structured Glass Portfolio FLEXINITY and related technologies provide an excellent starting point for highly sophisticated structured glass substrates required for RFIC Packaging. The biggest hurdle for a large scale commercialization of glass panel packaging is industrial readiness.This is needed to bring glass panel packaging in applications like IC-packaging or, in combination with cut-outs for fan-out, embedding of active and passive components. Also metallization processes with good adhesion, excellent electrical properties and high geometric accuracy for glasses are an important step. In the current manuscript we review the status and discuss our contribution towards achieving industrial readiness for glass in panel- and wafer-level packaging.

Biography
Dr. Tobias Gotschke works with SCHOTT, a specialty glass company, as a senior project manager in the corporate division New Ventures. He joined SCHOTT in 2019 and since then is driving the business development for specialty glass in the advanced packaging industry. In his former career in the LED industry, he gathered a lot of experience in managing larger project portfolios and supply chains as well as driving critical production ramp-ups and development projects in Europe and Asia. In his academic career, he received a PhD in physics from the Humboldt University Berlin (Berlin, Germany) and was working at several universities and research institutes (Technical University Berlin (Berlin, Germany), RWTH Aachen (Aachen, Germany), Research Center Juelich (Juelich, Germany), Paul-Drude-Institute (Berlin, Germany)) in the field of semiconductor nanotechnologies

3D Techniques for Accelerated Failure Analysis

T. Rodgers
Head of Electronics Business Sector
ZEISS Microscopy, Oberkochen, Germany

Abstract
A review of current technologies and workflows from ZEISS to facilitate failure analysis in modern semiconductor packaging. The rapid non-destructive characterisation of devices with X-ray microscopy, the subsequent preparation of these devices for electron microscopy, and some techniques for correlative image analysis will be described.

Biography
Dr. Thomas Rodgers leads the electronics industry strategic marketing team at Carl Zeiss Microscopy, which brings together electronics industry specialists, microscopy experts, and marketing professionals to apply ZEISS' X-ray, electron, and light microscopes to high value problems in the electronics and semiconductor industries. Thomas has degrees in electrical engineering and applied physics from Swinburne University in Australia, a PhD in applied physics from Osaka University in Japan, and an MBA from IMD business school in Switzerland. Prior to joining ZEISS, Thomas worked with Roper Technologies in applications and sales management roles for Princeton Instruments.

Packaging innovation in the Era of Heterogeneous Integration

B. Factor
Director, Technology Strategies
ASE, Inc, Paris, France

Abstract
Some of world's greatest challenges are being solved by the semiconductor technologies enabling global digitization. With unprecedented growth of applications across AI, 5G, IoT, and automotive, never has the need for semiconductor innovation been greater, and our industry is stepping up.

Heterogeneous Integration refers to the integration of separately manufactured components into a higher-level assembly (System-in-Package, known as SiP) that in the aggregate provides enhanced functionality and improved operational characteristics. It is now the key technology direction going forward, driving the pace of advancement for greater intelligence and connectivity, higher bandwidth and performance, and lower latency and power per function, all at a more manageable cost.

ASE's Bradford Factor will introduce the scope, reach and power of heterogeneous integration, describing how broad ecosystem collaboration is positioning the industry to initiate a new era of technology and scientific advances that will continue and complement Moore's Law scaling into the future. Factor will expand by exploring some of the innovations poised to achieve unprecedented impact on the way we live, work, play and communicate.

Biography
Bradford Factor received his Ph.D. from Stanford University in Applied Physics in 1991. After this, he held research positions in France and Greece and at the Polymers Division of NIST in the United States. Bradford started his career in the semiconductor industry in 1995, first at Intel's Assembly Technology Development team in Arizona and then at Lucent Microelectronics in 1999 to work on flip chip materials and assembly. He subsequently worked on the packaging of planar waveguide circuits and optoelectronic devices at Corning in France. He joined ASE Europe in 2002 and support the European customer base, including Israel, focusing on advanced technologies flip chip, wafer level packaging, system-in-package as well as power packaging. He is a currently a board member of IEEE CMPT in France, and has received several patents and published several journal articles.

Enabling Solutions through Packaging Enablement

J. Trewhella
Director of PostFab Engineering
GlobalFoundries, Malta, United States

GlobalFoundries does not permit uploading of our logo

Abstract
Foundries traditionally support customers with technology level PDK (Physical Design Kit) which is independent of the intended package. With applications like 5G, AI and ML demanding increased performance and lower cost there is a need for new levels of chip package co-design. GlobalFoundries is driving definition of an Assembly Design Kit which brings in the package ground rules (DRC), electrical performance (PEX), and layout into a validated reference flow effectively extending the silicon PDK for designers.

Biography
JEAN M. TREWHELLA is Director of Packaging Technology Integration for GLOBALFOUNDRIES, located in Malta, NY and the Past President of IEEE EPS. She received her B.S. in Physics from Antioch College (1987) and M.S. in Applied Physics from Columbia University (1992). Her early career at IBM Research included polymer optical waveguides fabrication, electrical modeling, and opto-mechanical package design for data communication systems. She moved into IBM Systems Group to lead a team developing interconnect hardware for IBM servers/ then transitioned to IBM Microelectronics as Director of IBM Packaging Research and Development Center. Currently at Globalfoundries she is responsible for PostFab New Product Introduction, CPI, and Package Enablement for GlobalFoudnries Technologies.

Eless plating for UBM metallization in high volume production

S. Zuercher
Team Leader Process Engineering & Laboratory
Ap-s, Dresden, Germany

Abstract
- AP&S achieved significant uniformity improvements for under bump metallization depositions via new hardware features -
UBM-eless metallization using NiP and Pd becomes more and more a technology of choice for advanced semiconductor devices. Requirements of metal non-uniformity on device- and wafer-level are continuously reaching higher requirements. To provide best process performance the AP&S eless plating equipment uses different hardware features addressing the needs to improve hydrodynamics of chemical flow to the structured wafer surface. Special flow turbulences support quick media exchange and a homogeneous distribution of chemical reactants on the reactive wafer surface on 150, 200 and 300mm wafers.

Biography
Stefan Zürcher started in 2011 at AP&S as process engineer for wet processes (etching, cleaning, UBM-eless plating, drying). Within 2012 working in R&D department for batch/singlewafer equipment and in application laboratory at AP&S Headquarter. Becoming manager of the new AP&S Democenter in 2015 and AP&S process manager in 2017. Responsible for all tasks related to process performance, optimization and development on AP&S equipment in singlewafer, batch and parts cleaning application. Patents in UBM-eless metallization technologies

New solutions for plasma dicing, and complete solutions for processing of SiC wafers ranging from ingot splitting, grinding, polishing to high speed and chipping free dicing

G. Klug
General Sales Manager
Disco Hi-Tec Europe GmbH, Munich, Germany

Abstract
Wafer thinning (Kezuru and Migaku) and dicing (Kiru) is essential for advanced packaging, for achieving narrow street widths and for making thin dies for 3D-packaging. New solutions on plasma dicing in combination with latest tapes and grinding technology enable the supply of perfect top side, back side and side wall quality on dies in thickness range from 20 – 150 µm.
Plasma dicing has various advantages comparing to the conventional dicing. However, during the plasma dicing process, the sensitive wafer front can be at risk due to the surface being exposed to plasma gas. It is common to protect the wafer front surface by photoresist in the wafer fab, which increases the cost and the processing steps.
DISCO has developed a special surface protection film and a total new processing flow for plasma dicing to overcome these issues.

SiC is getting more and more important for the energy efficient devices. Since SiC is a very expensive material, DISCO focuses on technologies for gaining as many as possible wafers and dies of outstanding quality out of it.
SiC ingot splitting by KABRA:
KABRA is a new method for SiC-ingot slicing by using a laser instead of a wire saw. In this process, a special layer is made inside of the ingot by laser irradiation and then the wafer is split from the ingot. 40% more wafers are obtained out of one ingot compared to conventional method.
SiC ingot and wafer grinding and polishing:
After splitting the wafer from the ingot, the ingot side and the wafer side need to be ground and polished. DISCO has developed grinding wheels and polishing pads (E Pad) suitable for wafer manufactures and device makers.
SiC wafer dicing by blade or laser:
To obtain more numbers of dies from a wafer, cutting streets can be reduced down to 50 µm and less. With our special technologies, cutting speed and quality have been greatly improved, too.

Biography
Coming soon

The Pivotal Role of Uniformity of Electrolytic Deposition Processes to Improve the Reliability of Advanced Packaging

R. Schmidt
R&D Manager Semiconductor
Atotech, Berlin, Germany

Abstract
Heterogeneous integration is considered as the key technology to create large, complex System in Package (SiP) assemblies of separately manufactured, smaller components. Proper control of the uniformity of each process step constitutes one of the main challenges during integration of the different components into a higher-level assembly. In this context, processes that create thick layers by electrochemical deposition are especially susceptible to variations across the substrate. Such processes include copper pillar and bump as well as tin-silver applications. Insufficient coplanarity of electrolytic copper would result in significant reliability issues or evolution of stress in the package. Upcoming hybrid bump designs with features of different dimensions pose additional challenges to the electrolytic copper and tin-silver processes. Purposeful adjustment of differences between the heights of pillars of different diameters may be required after the copper process step in order to obtain the best uniformity for the complete stack with tin-silver on top. In addition to coplanarity, the electrolytic process should allow modification shape of the individual pillar or bump. In this context, a versatile copper electrodeposition process will be discussed that allows adjustment to a broad variety of uniformity parameters and combinations thereof. In combination with suitable tin-silver deposition processes, this process is expected to significantly improve the reliability of copper pillars and bumps for advanced packaging applications.

Biography
For the past 10 years Ralf Schmidt has held various roles related to R&D at Atotech, wherein he focused, amongst others, on the development of various metal deposition processes. He is currently R&D Manager Semiconductor and responsible for all R&D projects, which are related to Semiconductor and Advanced Packaging topics.
Ralf is author of numerous publications and patents in this field and committee member of the Advanced Packaging conference of Semicon Europe as well as the 3D & Systems Summit.

Monitor Mechanical Stress and Damage in Advanced Packaging

R. Hillinger
Business Development Manager
Kistler Instrumente, Advanced Manufacturing,
Winterthur, Switzerland

Abstract
AI, 5G, IoT, ADAS, AR/VR and other new applications is giving the semiconductor industry plenty of growth opportunities. With the adoption of these technologies the pressure is on, to increase performance. The industry is using the power advantages of lower technology nodes and Advanced Packaging to put increased functionality on a single small form-factor which makes production processes even more challenging.
This advancements in semiconductor technology and added device complexity put additional pressure on monitoring and controlling Semiconductor packaging processes. The optimization of processes is a pre-condition for high reliability which is achieved by selecting appropriate materials and controlling critical process parameters. Currently Chip test, monitoring and control of packaging processes is widely done via optical and displacement Sensors. Improved methods for process monitoring and failure identification are needed to maintain or improve the quality and yield of a packaging process.

The physical force quantity causing a device failure may not be accessible to conventional measuring methods but is equally important to control and monitor production processes such as bonding, pick and place and encapsulation.

Piezo dynamic force measurement technology allows force to be monitored and controlled with high resolution even at low forces. As a result, deviations can be detected early, errors avoided, and Semiconductor Advanced Packaging Equipment builders can achieve higher and more accurate machine performance. Semiconductor Manufacturing-Packing companies in the semiconductor industry benefit from higher process visibility, performance, lower quality cost and traceability of process data.

Biography
Robert Hillinger has a degree in Electrical Engineering from the HTL Mödling in Austria. Since his studies he has worked as an Electrical Engineer, Product Manager and Business Manager in the Automation Industry. In 2018 he joined Kistler Instrumente in Winterthur, Switzerland who is a leading Measurement Company with own R&D, Production and global presence. Robert Hillinger works as Business Development Manager and supports Semiconductor customers to get better process visibility with Piezo Force Sensor Technology.

Laser Assisted Deposition for Electronics Mass Production

R. Birnbaum
Director of Business Development
IO Tech, Jerusalem, Israel

Abstract
We can divide all printing technologies into non-digital and digital methods. Usually, the non-digital methods are used for high throughput printing. The most common are screen printing and stamp pressure printing.

Digital printing techniques can be divided into nozzle based and laser-based technologies. The former uses a physical hole to ensure the printing volume/resolution, while in the latter the resolution is defined by the size of the focused beam. The nozzle-based technology (NBT) can be operated using either of two dispensing modes. The first, is the mode which underlies the inkjet technology and is called “drop on demand”. The material is printed drop by drop. In the second mode, which is used in micro-extrusion printers, the material is printed continuously. Nozzle based technologies allow printing of a large range of material types, with robust and stable properties. For this reason, this method is very useful for die bonding and different assembly applications. A major drawback however, is the requirement for constant maintenance due to clogging of the nozzles. There is an undesired trade-off here between throughput and resolution. The speed of the system decreases in proportion to the resolution. In fact most of these systems are “single nozzle” as opposed to standard inkjet which includes hundreds of nozzles in parallel The precision and speed is limited by the constraints of the motorized system.

Another method is LAD (Laser Assisted Deposition) also called LIFT (Laser Induced Forward Transfer). In it, a carrier substrate is coated with the material to be printed, and a pulsed laser beam is focused onto its interface with the material. The incident laser pulse is absorbed by a thin layer of the donor material. At sufficiently high laser pulse energy, a drop of the printing solution is locally deposited on the printing substrate. The physical process behind this consists of a fast evaporation of the solvent which causes bubble formation and vapor expansion, forming the jetting of a droplet. LAD is a nozzle free drop-on-demand method. It is therefore possible with LAD to print practically all flowable materials.

This paper describes the basics of LAD and presents a few applications in electronics, where each one emphasizes certain capabilities of the method. Amongst these capabilities are the printing quality and resolution, and the ability to print high viscosity materials printing in 2D and 3D shapes.

Biography
Ralph Birnbaum received his PhD from Imperial College, U.of London and an MBA from INSEAD.
For the past two decades has been working in marketing and business development in the electronics and chemicals industries, both as a consultant and for various companies like Orbotech, Nano Dimension and is now Director of Business Development with ioTech

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