FORWARD AS ONE
SEMICON® EUROPA
semi

Advanced Packaging Conference

Heterogeneous IC Packaging for Advanced AI Applications

M. Kelly
Vice President Advanced Package & Technology Integration
Amkor Technology, Inc., Tempe, United States

Abstract

Data centers, located in nondescript ultra-large-scale buildings where electric power is more affordable, are the backbone of the data processing and AI training done today. With tens of thousands of high-end central processing units (CPUs) and advanced AI accelerators, these intricate cities of electronics require thousands of kilometers of copper connectivity and megawatts of cooling. Advanced IC packaging trends in the data center are driven by requirements for high memory bandwidth (BW), many-core CPUs and ultrafast networking between racks, servers and storage. The resulting packaging solutions are focused around three key areas: on-package memory for maximum memory BW and capacity as required by AI accelerators; larger-than-reticle-size compute processors for servers; and ever-faster networking devices pushing towards 50 terabits per second (Tb/s) switch capabilities. This three-fold powerhouse of compute and storage, AI acceleration and ultrafast networks to connect discrete functions are pushing advanced IC packaging to the limit. Single IC packaging solutions are still present but are quickly being supplanted by heterogeneous packaging solutions which are required to enable functional performance increases commensurate with demand. IC packaging such as 2.5D silicon-based interposer and high bandwidth memory (HBM) are commonplace as AI accelerators and high-performance switches and routers. Trends in CPUs towards more and more cores to enable fine-grain utilization of this immense resource in the data center has pushed the required gate limit far beyond what can be captured in a single reticle using conventional physical partitioning on a single system on chip (SoC). These compute cores need the highest performance silicon transistors possible and are some of the first products into the latest silicon node. To make room for this compute gate count, high-speed I/Os are being pushed off-chip into discrete I/O chiplets. In addition, the total power requirements and shrinking operating voltages have pushed input current levels to new highs, bringing

electromagnetic interference (EMI) considerations back under the microscope, as well as putting local voltage regulation into the package to better contain the incoming current levels.

Biography

Mike joined Amkor in 2005 and has led package developments for EMI shielding, thermally enhanced packages, sensors and high density MCM packages including 2.5D TSV and high-density fan-out (HDFO). He has worked in electronics and IC package design and manufacturing for 25 years, managing projects ranging from polyester flexible circuits to eutectic flip chip, IC package design and signal integrity. Mike has more than 40 patents in the field and holds master’s degrees in Mechanical and Chemical Engineering.

Advanced materials and interconnection technologies for highly miniaturized IoT modules

M. Martina
Head of Strategy
Micro Systems Technologies, Berlin, Germany

Abstract

Standardization of semiconductor packaging and interconnection technology is a key aspect to allow for large scale manufacturing and commercialization. However, to achieve maximum performance and higher integration density allowing for smallest form-factors, precisely tailored solutions and the application of novel and unconventional materials and interconnection concepts must be chosen, while manufacturability needs to be preserved.

In the first part of this work, novel materials, assembly, interconnect, and packaging processes were developed, which can be combined to realize highly miniaturized, hermetic IoT devices.

Applying this toolbox, a technology platform to manufacture customized Systems-in-Package (SiP) for IoT applications was developed. The base components are integrated in a SiP with through-package-via (TPV) interconnections and are soldered to an advanced flexible substrate. On top of the SiP, a second interconnection substrate with a customizable sensor configuration can be attached. On the bottom level, the flexible substrate allows for several additional system components to be attached. In a final step, the whole system can be miniaturized or custom-shaped by folding the substrate into the desired form factor.

To realize advanced flexible substrates, novel processes to structure and manufacture liquid crystal polymer (LCP) circuits were developed. Resulting, flexible LCP substrate with lines/spaces down to 15/15 µm were achieved which offer flexibility for folding, biocompatibility, and chemical inertness. Notably, a special lamination process was developed which allows to encapsulate copper traces as well as to embed semiconductors and passives inside the LCP substrate without forming interfaces as it is the case with bond sheets. Resulting, hermeticity could be achieved while drastically increasing reliability. Furthermore, LCP offers low radio-frequency dielectric losses and a stable dielectric constant.

A miniaturized IoT-Module with a volume of only 1.3 cm³, a broad range of sensors including a microphone and electrochemical measurements, in a hermetic housing with electrical feedthroughs in LTCC, with wireless charging and an IoT-SiP was designed and manufactured to demonstrate this packaging approach. The module can be connected to any smartphone via Bluetooth Low Energy (BLE) and allows to monitor temperature, pressure, sound, impedance, illumination, position, and acceleration even under harsh environments and in liquids.

Biography

Manuel Martina received the B.Sc. degree in physics from RWTH Aachen University, Aachen, Germany, in 2011, the M.Sc. degree in physics as well as the Ph.D. degree for his work in near-field optics and microfabrication/nanofabrication from the Eberhard Karls University of Tübingen, Tübingen, Germany, in 2014 and 2017, respectively.

He worked as a Researcher in several fields of microsystems technology and on the interface to biology with the Natural and Medical Sciences Institute, Reutlingen, Germany. From 2017 on, he was working as Manager of Next-Generation Products with the Research and Development Department at Schweizer Electronic AG, Schramberg, Germany. His research included semiconductor embedding and packaging in high-end printed circuit boards for future automotive radar and industrial 5G applications, and for future power electronics. Since 2021, he is working at Micro Systems Technologies in the fields of advanced semiconductor packaging and packaging substrates.

Thin Cu Plate-able Dielectric Material Developments for RF and Power Device Miniaturization

R. de Wit
Business Development Manager EMEA
Henkel Electronic Materials, Westerlo, Belgium

Abstract

Smart Electronics' market trends like 5G, 6G and ADAS are driving advanced semiconductor packaging innovations towards higher functionality, enhanced connectivity at higher frequencies, RF signal interference isolation (shielding), smaller form factors (miniaturization) and reduced power consumption. To meet these future demands, semiconductor package designs continue to evolve towards challenging System-in-Package, Antenna-in/on-Package and Wafer Level architectures. Especially for next generation RF and Power devices, antennas and radars, the thermo-mechanical, thermal resistance and (di)electric properties of the assembly and packaging materials play a key role as well as fast and low temperature processing/curing. Exploring development work together with laser specialist LPKF last year resulted in a new SVHC free and low warpage Liquid Compression Molding (LCM) encapsulant suitable for Laser Direct Structuring. Deposition of 25/25um L/S Cu tracks and Cu plating of blind vias down to 50um have been demonstrated as presented during Advanced Packaging Forum in February this year. This APC presentation will cover further product development and test work together with LPKF on a new STENCIL PRINTABLE encapsulant aiming for <50um thin dielectric layers with 15/15um L/S Cu tracks and <50um Cu plated blind vias. Next to more functionality in same or even smaller package footprint, this “direct and additive Cu formation” technology can also deliver significant cost savings by introducing only three back-end approved processing steps of molding, lasering and plating (vs typically seven costly and time-consuming semi-additive processing steps like seed layer sputtering, masking, lithography, development, Cu plating, mask removal and flash etching).

Biography

Ruud de Wit is responsible for managing Henkel's Semiconductor, Sensor & Consumer Electronics Assembly Materials business development within EMEA region. Ruud has a BSc degree in Mechanical Engineering followed by several polymer, sales and marketing courses. Ruud is working for Henkel since 1990 in multiple positions including technical customer support, quality assurance and engineering, and global semiconductor account and product management. Last couple of years, Ruud's main focus is on exploring and driving new semiconductor packaging material development needs within Henkel to enable potential customers to design smaller RF and Power devices.

Die-attach bonding with copper metal pigment flakes

G. Elger
Professor for Manufacturing Technologies of Electronics
Technische Hochschule Ingolstadt, Institute for Innovative Mobility, Ingolstadt, Germany

Abstract

Solid state sintering has emerged as a preferred die-attach process of choice for high temperature applications due to the formation of near bulk like interconnects which are capable of providing high temperature operations. Ag sintering under pressure is an industrialized process today. However, low cost alternatives, which offer comparable or better results under the same processing parameters, are desired. Among all metals Cu offers the next best thermal conductivity to Ag, is easily available, recyclable and the raw material cost are a fraction of that of Ag. Therefore, in recent years, focus has shifted to develop Cu sintering as a reliable alternative to the industrialized Ag sintering processes. However, Cu is highly prone to oxidation and the build-up of oxide layers is a diffusion barrier against material transport during sintering. We propose a novel approach by the use of micro-scale (3-5 µm), thin (200 nm) and high surface area (3.5 m^2/g) Cu metal pigment flakes from Schlenk Metallic Pigments GmbH. Due to their design, the flakes stack over each other. This results in a dense and homogenous interconnect with a shear strength of ~ 40 MPa, while sintering under pressure of 10 MPa at 275 °C for 5 min. Since the flakes stack over one another, the overall surface area in contact is increased, thereby enhancing sintering. The stearic acid coating on the flakes, introduced during the ball milling process to prevent cold welding of the flakes is observed to be not only effective in preventing oxidation of the flakes, but also avoids agglomeration of the flakes during paste formulation and enabling excellent stencil printing capabilities.

The effective stacking of the flakes also allows for sintering under low bonding pressure and realizing a well sintered interconnect even with a solids content of only 60 wt% in the paste formulation, compared to commercially available Ag sinter pastes with ~90 wt% solids content. A simple two-step sintering process similar to industrialized Ag sinter processes is realized, including pre-drying at 120 °C followed by isothermal sintering at 275 °C in an open bond chamber. The use of PEG600 in the paste formulation allows for an in-situ reduction of Cu oxides.

The paste therefore offers an attractive low cost alternative to Ag sintering in die-attach bonding applications and can be introduced in the same equipment as presently used for Ag sintering under pressure.

Biography

Gordon Elger studied physics and made his PhD 1998 at the Free University of Berlin.
Afterwards, he worked at Fraunhofer-IZM, Hymite GmbH, Electrolux and Philips GmbH in the field of optoelectronic, LED, MEMS, high frequency packaging and CAE, e.g. FEM and CFD for structural analysis and heat management.
Since 2013 he is professor at the University of Applied Science in Ingolstadt (THI) for electronic manufacturing technologies and has built up a research team within the Institute of Innovative Mobility of the THI.

Gordon Elger’s research is focused on microelectronics packaging and reliability, e.g. optoelectronic, sensor and power electronic packaging for automotive applications. One focus is the development of first and second level interconnects, e.g. residual free solder processes, new materials and processes for sintering. Another focus is the development of nondestructive measurement and test methods for reliability and quality insurance of interconnects, e.g. an automated transient thermal impedance tester for LED and power electronic devices. His research teams performs reliability analysis of interconnects and electronic modules. Based on the experimental data, models to predict the remaining useful life of interconnects are developed using physical “White Box” modelling (FEM) and data driven “Black Box” approaches.

Since 2020 Gordon Elger is in addition head of the new founded Applied Research Center for “Connected Mobility and Infrastructure” of the Fraunhofer IVI. Sensor data fusion, smart electronic applications, condition monitoring and artificial intelligence based algorithm development for predictive health management are a second field of research within present projects of the new founded Applied Research Center.

Thin glass for wafer- and panel- level packaging: On the route towards industrialization.

M. Letz
senior principal scientist
Schott AG, Reseach and Development, Mainz,
Germany

SCHOTT

Abstract

With the development of semiconductor technologies, glass wafers are getting more important as a carrier material for temporary bonding with silicon wafers in semiconductor applications such as 3D IC, RF IC Packaging and Fan-out Wafer Level Packaging. We discuss glass carrier wafer products with unique properties: (i) an extremely low TTV < 0.6 µm along with low flatness that ensures almost no warping or bowing of the glass in the application. (ii) The broad coefficient of thermal expansion (CTE) range from 3.2 to 9.4×10^{-6} /K can match Si but can also be closer to higher CTE materials like epoxy molds and metal layers. (iii) Excellent UV transmission enables highly effective laser debonding, e.g. 1.1mm thick Borofloat 33 HT has a transmission >60% at 248nm and >90% at 307nm. Upon the latest breakthrough of glass and related processing technologies, our glass carriers enable the miniaturization of manufacturing in both front-end and back-end processes of semiconductors.

Glasses can be also used as core substrate for panel- and/or wafer-level packaging to achieve heterogeneous integration in increasingly complex packages. Glass has a large number of advantages: The stiffness of glass (iv) allows manufacturing of highly accurate buildup layers with manufacturing precision of 1µm and below. Special glasses can be made with very good dielectric properties (v) and can also be applied in antenna-in-package applications. But most of all, economic glass structuring techniques (vi) which can provide millions of vias and thousands of cut-outs in a glass panel are important and are being developed. SCHOTT's Structured Glass Portfolio FLEXINITY and related technologies provide an excellent starting point for highly sophisticated structured glass substrates required for RFIC Packaging. The biggest hurdle for a large scale commercialization of glass panel packaging is industrial readiness.This is needed to bring glass panel packaging in applications like IC-packaging or, in combination with cut-outs for fan-out, embedding of active and passive components. Also metallization processes with good adhesion, excellent electrical properties and high geometric accuracy for glasses are an important step. In the current manuscript we review the status and discuss our contribution towards achieving industrial readiness for glass in panel- and wafer-level packaging.

Biography

Martin Letz works with SCHOTT, a special glass company, as a senior principal scientist. He joined SCHOTT in 2001 and was involved in several projects regarding materials for semiconductor structuring. Since several years he focusses on glasses and glass ceramics for electronic applications and their properies. One focus is on materials for antenna and filter structures for wireless data transfer. A second focus is on miniaturization of electronics using glass packaging. Prior to that he received his phd in solid state physics from the University of Stuttgart in Germany and had several positions in research institutions and Universities (Tartu University (Estonia), Max-Plack Institut (Stuttgart, Germany), Queens University (Kingston, Canada), University of Mainz (Germany)) working on different aspects of strong correlations in condensed matter.

The Pivotal Role of Uniformity of Electrolytic Deposition Processes to Improve the Reliability of Advanced Packaging

R. Schmidt
R&D Manager Semiconductor
Atotech, Berlin, Germany

Abstract

Heterogeneous integration is considered as the key technology to create large, complex System in Package (SiP) assemblies of separately manufactured, smaller components. Proper control of the uniformity of each process step constitutes one of the main challenges during integration of the different components into a higher-level assembly. In this context, processes that create thick layers by electrochemical deposition are especially susceptible to variations across the substrate. Such processes include copper pillar and bump as well as tin-silver applications. Insufficient coplanarity of electrolytic copper would result in significant reliability issues or evolution of stress in the package. Upcoming hybrid bump designs with features of different dimensions pose additional challenges to the electrolytic copper and tin-silver processes. Purposeful adjustment of differences between the heights of pillars of different diameters may be required after the copper process step in order to obtain the best uniformity for the complete stack with tin-silver on top. In addition to coplanarity, the electrolytic process should allow modification shape of the individual pillar or bump. In this context, a versatile copper electrodeposition process will be discussed that allows adjustment to a broad variety of uniformity parameters and combinations thereof. In combination with suitable tin-silver deposition processes, this process is expected to significantly improve the reliability of copper pillars and bumps for advanced packaging applications.

Biography

For the past 10 years Ralf Schmidt has held various roles related to R&D at Atotech, wherein he focused, amongst others, on the development of various metal deposition processes. He is currently R&D Manager Semiconductor and responsible for all R&D projects, which are related to Semiconductor and Advanced Packaging topics.
Ralf is author of numerous publications and patents in this field and committee member of the Advanced Packaging conference of Semicon Europe as well as the 3D & Systems Summit.

Monitor mechanical stress and damage in Advanced Packaging

R. Hillinger
Business Development Manager
Kistler Instrumente, Advanced Manufacturing,
Winterthur, Switzerland

Abstract

AI, 5G, IoT, ADAS, AR/VR and other new applications is giving the semiconductor industry plenty of growth opportunities. With the adoption of these technologies the pressure is on, to increase performance. The industry is using the power advantages of lower technology nodes and Advanced Packaging to put increased functionality on a single small form-factor which makes production processes even more challenging.
This advancements in semiconductor technology and added device complexity put additional pressure on monitoring and controlling Semiconductor packaging processes. The optimization of processes is a pre-condition for high reliability which is achieved by selecting appropriate materials and controlling critical process parameters. Currently Chip test, monitoring and control of packaging processes is widely done via optical and displacement Sensors. Improved methods for process monitoring and failure identification are needed to maintain or improve the quality and yield of a packaging process.

The physical force quantity causing a device failure may not be accessible to conventional measuring methods but is equally important to control and monitor production processes such as bonding, pick and place and encapsulation.

Piezo dynamic force measurement technology allows force to be monitored and controlled with high resolution even at low forces. As a result, deviations can be detected early, errors avoided, and Semiconductor Advanced Packaging Equipment builders can achieve higher and more accurate machine performance. Semiconductor Manufacturing-Packing companies in the semiconductor industry benefit from higher process visibility, performance, lower quality cost and traceability of process data.

Biography

Robert Hillinger has a degree in Electrical Engineering from the HTL Mödling in Austria. Since his studies he has worked as an Electrical Engineer, Product Manager and Business Manager in the Automation Industry. In 2018 he joined Kistler Instrumente in Winterthur, Switzerland who is a leading Measurement Company with own R&D, Production and global presence. Robert Hillinger works as Business Development Manager and supports Semiconductor customers to get better process visibility with Piezo Force Sensor Technology.

Laser Assisted Deposition for electronics mass production

R. Birnbaum
Director of Business Development
IO Tech, Jerusalem, Israel

Abstract

We can divide all printing technologies into non-digital and digital methods. Usually, the non-digital methods are used for high throughput printing. The most common are screen printing and stamp pressure printing.

Digital printing techniques can be divided into nozzle based and laser-based technologies. The former uses a physical hole to ensure the printing volume/resolution, while in the latter the resolution is defined by the size of the focused beam. The nozzle-based technology (NBT) can be operated using either of two dispensing modes. The first, is the mode which underlies the inkjet technology and is called “drop on demand”. The material is printed drop by drop. In the second mode, which is used in micro-extrusion printers, the material is printed continuously. Nozzle based technologies allow printing of a large range of material types, with robust and stable properties. For this reason, this method is very useful for die bonding and different assembly applications. A major drawback however, is the requirement for constant maintenance due to clogging of the nozzles. There is an undesired trade-off here between throughput and resolution. The speed of the system decreases in proportion to the resolution. In fact most of these systems are “single nozzle” as opposed to standard inkjet which includes hundreds of nozzles in parallel The precision and speed is limited by the constraints of the motorized system.

Another method is LAD (Laser Assisted Deposition) also called LIFT (Laser Induced Forward Transfer). In it, a carrier substrate is coated with the material to be printed, and a pulsed laser beam is focused onto its interface with the material. The incident laser pulse is absorbed by a thin layer of the donor material. At sufficiently high laser pulse energy, a drop of the printing solution is locally deposited on the printing substrate. The physical process behind this consists of a fast evaporation of the solvent which causes bubble formation and vapor expansion, forming the jetting of a droplet. LAD is a nozzle free drop-on-demand method. It is therefore possible with LAD to print practically all flowable materials.

This paper describes the basics of LAD and presents a few applications in electronics, where each one emphasizes certain capabilities of the method. Amongst these capabilities are the printing quality and resolution, and the ability to print high viscosity materials printing in 2D and 3D shapes.

Biography

Ralph Birnbaum
Herve Javice
Guy Nesher
Michael Zenou