Advanced Packaging Conference

Packaging Trends for AI

J. Vardaman
President
TechSearch International, Inc., Austin, United States

Abstract
Artificial Intelligence (AI) makes it possible for machines to learn from experience, adjust to new inputs and perform human-like tasks. AI or deep learning is expected to be applied to a wide range of applications, including connectivity or Internet of Things (IoT), big data processing and servers, cloud services, autonomous driving, 5G communications, smart factory or Industry 4.0, robotics, AR/VR. The package choice depends on many factors including design, density, reliability, and supply chain. This presentation examines the applications using AI and the packages in production today. The presentation also discusses future packages expected for these applications. Package choice, design, and materials impact and the importance of co-design will be discussed.

Biography
E. Jan Vardaman is president and founder of TechSearch International, Inc., which has provided market research and technology trend analysis in semiconductor packaging since 1987. She is the co-author of How to Make IC Packages (by Nikkan Kogyo Shinbunsha), a columnist with Printed Circuit Design & Fab/Circuits Assembly, and the author of numerous publications on emerging trends in semiconductor packaging and assembly. She is a senior member of IEEE EPS and is an IEEE EPS Distinguished Lecturer. She is a member of SEMI, SMTA, IMAPS, and MEPTEC. She received the IMAPS GBC Partnership award in 2012 and the Daniel C. Hughes, Jr. Memorial Award in 2018. She is an IMAPS Fellow. Before founding TechSearch International, she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC), the electronics industry's first pre-competitive research consortium.

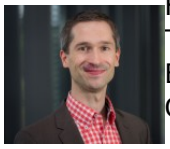
Semiconductors in a world where safety rules supreme

M. Schuldenfrei
Technology Fellow
Optimal Plus, Business and Technology, Holon, Israel

Abstract
Advanced packaging solutions incorporate multiple die into packages using a broad range of new techniques and technologies. These solutions have many benefits – lowering cost, reducing power consumption, increasing performance and more. However, they come with elevated risk – the more complex the solution, the more care we need to take to ensure we are delivering perfect parts. After all, in safety-critical applications like the autonomous and connected car, failures cannot be tolerated.
In this presentation, we will present some of the quality and reliability challenges introduced by advanced packaging technologies and how Big Data Analytics can be leveraged to mitigate the risks.

Biography
Michael joined OptimalPlus in 2006, and brings over 30 years of software and information technology experience. Since joining the company he has served in several leadership roles including Chief Software Architect and CTO. Prior to that he served as Senior Software Architect at SAP, where he led a joint development project with Microsoft. He was also a Software Architect at Microsoft, where he led consulting engagements with the company's major customers, and VP of R&D at ActionBase, heading up development of the company's business management enterprise solutions.

Development of a Modular Test Setup for Reliability Testing under Harsh Environment Conditions



K. Meier
Technische Universität Dresden, Institute of Electronic Packaging Technology, Dresden, Germany

Abstract
The increasing contribution of electronics to the functionality of automotive vehicles pursues the demand for highly integrated, low power, and very reliable electronics. To fulfil the application requirements of automotive electrification and connectivity the electronics packaging performance has become a dominant factor of the electronics system capability. In addition, chip package interaction has become important in advanced semiconductor technology nodes.
The Industry is developing and manufacturing various package approaches to meet different application needs. These packages are exposed to multiple load cases. Both, the large number of package approaches as well as the variety of mission profiles have to be considered in the development process of reliable packages which leads to the need to develop a modular test setup concept.
In this presentation a modular test setup is going to be shown which addresses the ability to perform multiple reliability analysis of different package types at board and package level according to standard (e.g. AEC-Q100) or mission profile specifications. Using the test setup packages with sizes of up to 50x50 mm², a pitch as small as 0.4 mm and very high I/O counts (>1,000) can be considered. The recently used configuration is capable for simultaneous testing of 16 packages. Since its modular design, the setup can be adopted to other test lot sizes and test group configurations easily.
As an initial verification prove point biased temperature humidity tests (THB 85/85) for up to 1,500 hours on a FCCSP package have been accomplished. Detailed characterisation of the developed test setup - offering a maximum voltage of 35 V or maximum current of 1.5 A for up to 8 individual channels - under THB conditions has been done. Monitoring with a high resolution in terms of time (<1 s), voltage (<1 mV) and current (<<1 µA) is available. This enables tracking of immediate humidity responses and package humidity uptake. Additional setup enhancements have be implemented to prepare for conducting temperature cycling on board and uniaxial vibration tests.

Biography
Dr. Karsten Meier is with the Institute of Electronic Packaging Technology at the Technische Universität Dresden (Dresden, Germany) since 2006. After studying electrical engineering he received his Ph.D. from Technische Universität Dresden in 2015. During his studies he spent a research visit at the Packaging Research Center at the Georgia Institute of Technology in Atlanta (Georgia, USA). At the Institute of Electronic Packaging Technology he is working with the board level reliability group and responsible as assistant director. His research activities cover projects on packaging technology developments and package reliability for 5G and automotive applications, power electronics, material characterisation, and thermo-mechanical simulation. Recently, he also supports a research collaboration with the Center for Advanced Life Cycle Engineering at the University of Maryland (Maryland, USA) on combined mechanical and thermal loadings on solder interconnections. Karsten Meier is author of multiple publications. He is a member of the IEEE EPTC sub-committee Advanced Packaging, the IEEE ECTC sub-committee Thermal/Mechanical Simulation and Characterisation, and the IEEE ESTC sub-committee Reliability of Electronic Devices and Systems. As a reviewer he supports the IEEE EuroSimE conference.

Product on Board Test Method for Advanced Reliability Performance of a Large 0.3 mm Pitch Wafer Level Chip Scale Package

G. Seidemann
Intel Deutschland GmbH, Neubiberg, Germany

Abstract
Board level reliability tests are well known for electronic packaging qualification for consumer markets in the semiconductor industry. The existing JEDEC/IPC board level methodology tests on daisy chains (DC) for chip-package-board-interaction (CPBI) apply well to traditional packaging solutions for non-extreme low K dielectric (ELK) fab nodes. Future products require new methods of reliability testing for advanced silicon nodes and advanced packaging, especially for the demanding automotive industry.
Currently, DC designs do not accurately reflect a product design. DC designs have a reduced layer stack and usually no back-end of line (BEOL) ELK stack. Thus, the second level interconnect performance of the ELK and/or reduced pin count, is not covered. The new approach to reflect product conditions is a component on board setup with industrial standard or to the customer life board with live product. This allows quantification of the complete value chain including chip, package, and board as a component manufacturer. The method reported here comprises results from advanced wafer level chip scale packages (WLCSP) and others. The full functional test used for live components on board including automatic handling generates a higher sensitivity and throughput compared to DC testing. The reuse of this methodology for high volume manufacturing monitoring (HVMM) is also possible.
In temperature cycling tests on board (TCoB), *a significantly reduced cycle count to failure (up to a factor of 3)* with live *product on board compared to daisy chain on board tests-t*he analyzed failure mechanisms are the same. This is due to the higher sensitivity of the full functional test program, specifically, the IR drop sensitivity. This allows for the study of the initiation and propagation of cracks or delamination providing a tool set for enhanced CPBI validation.

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tool set for enhanced CPBI validation.

Stretching the Performance Envelope of ATE PCBs

T. Bleakley
VP Integration
Harbor Electronics, Integration, Santa Clara, United States

Abstract
In today's production test environment, high power, high speed, high ball count, tight pitch and increased parallelism drive complexity into the ATE interface / probe card PCB.

These factors inevitably drive PCB layer counts up, beyond what can be achieved in single lamination printed circuit boards, forcing more expensive and time consuming processes such as sequential lamination and HDI techniques.

This presentation will discuss PCB fabrication constraints, technology extenders and introduces an alternative to standard PCB processing techniques. Power integrity, signal integrity, manufacturing throughput and reliability characteristics of available options will be compared.
Specific examples to be discussed include:
-Multitier PCB with 0.3mm DUT pitch in a 310mil thick PCB.
-Memory test application with 100,000 pads and via interconnects in a 600mil thick PCB
-WLCSP application with 0.35mm pitch in a 250 thick PCB

Biography
Tom Bleakley is Vice President of Integration at Harbor Electronics where he oversees PCB design, assembly and test, applications and field service engineering. Tom’s team is responsible for ensuring that Harbor PCBA designs integrate well with fab, assembly and field support operations, optimizing probe card and load board PCBA performance as well as delivery times.

Tom has spent his entire career in semiconductor test. Before Harbor with Everett Charles Technologies as a Product Manager. Before ECT, Tom served in Product Engineering and Test Technology roles with Intel’s Desktop Chipset group in Folsom, CA, and with Intel Communications group in Sacramento, CA.

Tom began his career as a hardware design engineer with Micro Component Technology (MCT) in Shoreview, MN designing DC parametric and pin electronics hardware before moving to an Applications Engineering role.

Tom holds a bachelor of science degree in electrical engineering (BSEE) from North Dakota State University.

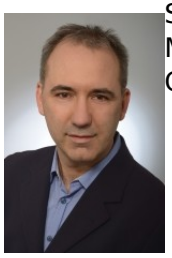
Reliability Requirements of Advanced Packaging in the Era of Electrified, Automated and Connected Driving

P. Gromala
Simulation senior expert
Robert Bosch GmbH, AE/ECU3, Reutlingen, Germany

Abstract
Development of automotive electronic systems is driven by three major trend: Electrification, Automation, and Connectivity. Each of these trends will bring specific reliability challenges:
Electrification will revolutionize the entire powertrain and the required road infrastructure. Gradually but steadily, combustion engines will decrease their market share. Power electronics will be one of the key drivers of this development by remarkable innovations. New encapsulating materials will be introduced to meet these new requirements. In addition, sensors and control electronics will be added directly to the power stages for enhanced performance and safety. This increases the heterogeneity and complexity of these systems.
Automated driving will revolutionize transportation system. By 2025, conditionally and highly automated driving will reach SAE levels 3 and 4, respectively. By 2030, it will also be available in complex traffic situations, e.g., urban areas, and will reach SAE level 5. The highly automated vehicles will increase safety, provide greater comfort, and improve the traffic flows. New service modes seem to give a clear preference to car-sharing options over individual ownership. Consequently, the total operational time will significantly increase.
Connectivity will introduce consumer inspired technology components to harsh environments. Advanced integration and packaging schemes, such as system on chip (SoC) and system in package (SiP) based on smallest technologies nodes (e.g., 7 nm), will be introduced to automobiles with high reliability and fail-safe operation requirements.
In my presentation I will try to answer what are the emerging reliability challenges for electronic packaging due to three major trends in automotive.

Biography
Dr Przemyslaw Gromala is a simulation senior expert at Robert Bosch GmbH, Automotive Electronics in Reutlingen. Currently leading an international simulation team and FEM validation and verification lab with the focus on implementation of simulation driven design for electronic control modules and multi-chip power packaging for hybrid drives. His technical expertise includes material characterization and modeling, multi-domain and multi-scale simulation incl. fracture mechanics, V&V techniques, and prognostics and health management for safety related electronic smart systems.
Prior joining Bosch Mr Gromala worked at Delphi development center in Krakow, as well as at Infineon research and development center in Dresden.
He is an active committee member of the IEEE conferences: ECTC, EuroSimE, iTherm; ASME: InterPACK.
Active committee member of EPoSS – defining R&D and innovation needs as well as policy requirements related to Smart Systems Integration and integrated Micro- and Nanosystems.
He holds a PhD in mechanical engineering from Cracow University of Technology in Poland.

Chip Package Interaction Test structure design to address challenges from products with RF specific back end of line metallization options on Flip Chip ETS substrate



S. Capecchi
MTS Reliability Engineer
Globalfoundries, Dresden, Germany

Abstract
The growing interest in applications for 5G communication has generated some efforts in developing new Back End of Line (BeoL) schemes in the Semiconductors industry. In particular, BeoL stacks with Ultra Thick Metal (UTM) for RF mmWAVE applications have come to the forefront. However the high thickness of the UTM (~3um) can induce significant residual stress, which brings up new challenges related to wafer and die warpage. The die warpage becomes quite critical during the temperature cycle that the silicon die undergoes during the flip chip assembly process.
In addition, the market pressure to reduce assembly costs in packaging is driving the use of coreless Embedded Trace Substrates (ETS). The use of low cost substrates such as ETS can potentially reduce the assembly process margins: an ETS coreless substrate can be more prone to warpage during the assembly process than core substrates. The combination of silicon die and ETS substrate warpage can cause assembly yield loss as well as potential reliability issues.
In this work we present the study of a Chip Package Interaction (CPI) test vehicle, with a Cu double Ultra Thick Metal implemented in a GLOBALFOUBDRIES 22FDX® BeoL stack. This test vehicle has been assembled using an Embedded Trace Substrate (ETS). This work is focusing on testing CPI structures that have been implemented to catch warpage and stress related fails through electrical test before and after the reliability environmental stress. Three different types of CPI sensor structures have been designed and implemented in the CPI test vehicle, in order to detect cracks in the BeoL and die warpage driven fails during and post assembly.
Assembled dies of this test vehicle have undergone JEDEC standard reliability environmental test stresses. In conclusion, the GLOBALFOUNDRIES 22FDX® double UTM BeoL used in this work proved to be robust enough to pass the JEDEC standard reliability environmental test stress in a standard flip chip package with ETS substrate.

Biography
Simone Capecchi
Member of Technical Staff, Reliability Engineering
Globalfoundries, Dresden, Germany

Simone Capecchi is currently employed as Member of Technical Staff in the Reliability Engineering Group of Globalfoundries in Dresden, Germany. The focus of his work is on Chip Package Interaction Reliability.
Still in Globalfoundries Dresden, Simone spent four years in the wafer bumping engineering group sustaining high volume production as well as introducing new technologies
Prior to joining Globalfoundries, Simone lead an engineering group in STMicroelectronics for 3 years.
Simone also worked as Senior Engineer in Intel Ireland and Intel US, sustaining high volume production as well transferring technologies from the development site to a high volume manufacturing site.
Simone has also experience in the optical components fabrication in Nortel Networks where he developed processes for telecommunication components.

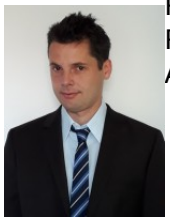
Effect of harsh temperature ramp rates on solder joints of Wafer-Level CSPs in board level reliability tests.

S. Schambeck
BMW Group, Munich, Germany

Abstract
Board level reliability qualifications based on automotive mission profiles take a huge amount of time. This is caused by harsh operation conditions in the field as well as the extended lifetime requirements compared to consumer electronics. Further reduction of the testing time is the major goal of accelerated testing. Temperature cycling tests simulate thermomechanical stress in the component and its interconnect technology. Optimizing the parameters of thermal cycling conditions is the most used approach in the literature to accelerate field relevant failure mechanism. A decrease in the parameter temperature ramp time influences testing time in two ways: Reduction in cycles to failure and direct reduction of cycle time. However, the quantitative effect on lifetime and the resulting failure mechanism have to be evaluated, especially for conditions which are less usual like liquid to liquid thermal shock. Some authors argue, that different failure mechanism may be triggered by those potentially exaggerated conditions. Nevertheless, cross sections of liquid to liquid aged components can only rarely be found in the literature. This investigation shows the lifetime as well as the failure mechanism in a Wafer-Level CSP and a common 1206 resistor over a broad range of different ramp rates. This includes conventional thermal cycling and thermal shock up to liquid to liquid testing. Electrical monitoring of the WLCSP solder joints indicates, that the characteristic lifetime is decreased for harsh ramp rates. Cross sections demonstrate, that the failure mechanism is solder fatigue in all cases. Detailed analysis shows, that the microstructure aging is comparable in all stages of damage evolution in terms of precipitate coarsening, onset of recrystallization and crack growth.

Biography
Simon Schambeck received his Bachelor’s degree in Physics at the University of Regensburg, Germany in 2014 and finished his Master’s Degree in Physics in 2017. He wrote his Master’s Thesis in a working group focusing on epitaxial nanostructures. Parallel to his studies he assisted in development departments at OSRAM OLED GmbH and BMW Group. Currently he is working in the engineering department for semiconductor standards and environment simulation of the BMW Group in Munich. He is doing research on board level reliability testing for his PhD thesis including simulation of solder joint lifetime, test definition and characterization of failure mechanisms.

Holistic Approach to Improve the Reliability of Advanced Heterogeneous Packaging by Chemistry



R. Schmidt
R&D Manager Semiconductor
Atotech, R&D Semiconductor, Berlin, Germany

Abstract
Heterogeneous integration involves the assembly of separately manufactured components and requires the combination of a broad variety of different materials with different characteristics. Redistribution layers (RDLs) consisting of Cu conductor lines and organic dielectric are key components of a variety of technologies to connect the various functional components. In particular, fan out wafer level packaging (FOWLP) with decreasing lines and spaces (L/S) was developed as an enhancement to standard WLP to allow for higher performance, decreased form factor, and significant cost reduction. Next generation FOWLP require decreasing the RDL pitch down to 1 µm or even below, which involves challenges in terms of reliability of the Cu conductor lines.
With decreasing L/S, mechanical properties of RDL Cu lines become increasingly important. This is especially true with regard to the variety of materials, which are in direct contact upon heterogeneous integration of different components. In order to improve the reliability of such assembly, the mechanical properties of the individual materials need to be optimized. However, this improvement is limited by issues upon scaling down the Cu conductor lines. Thus, a different approach is required to provide sufficient reliability. In addition to optimization of the individual materials, a holistic approach would include the surrounding materials within the package. Recent findings emphasize the importance of the formation of a proper composite with the adjacent dielectric to improve the reliability of the Cu conductor lines. Utilization of the surrounding materials by composite formation constitutes a promising strategy to fulfill reliability criteria of upcoming FOWLP applications. Composites may benefit from synergistic effects and overcome limitations of the individual components. Different chemistry solutions will be discussed with respect to their impact on composite formation and suitability for potential 5G applications.

Biography
For the past 8 years Ralf Schmidt has held various roles related to R&D at Atotech, wherein he focued, amongst others, on the development of innovative copper plating processes. He is currently R&D Manager Semiconductor and responsible for all R&D projects, which are related to Semiconductor and Advanced Packaging topics.
Ralf is author of numerous publications and patents in this field and committee member of the Advanced Packaging as well as Stratetic Materials Conferences of Semicon Europa.

Board Level Reliability results for a two side molded WLCSP

T. Kamphuis
Package Pathfinding
NXP, Package Innovation, Nijmegen, Netherlands

Abstract
Increasingly WLCSP are used as solution for packaging, especially when the area needed for I/O matches the area needed for the function. Industry trend is to go thinner devices and smaller pitches. The mechanical integrity of WLCSP's is stressed not only in the application, but also during board assembly at the customer. The breakthrough technology presented provides protection for both the top and bottom of the product, thus protecting the 8 corners of the device. Balancing the front and back side thickness of the compound enables reduction of the overall height while at the same time improve the BLR performance compared to more well-known 5 side protected WLCSP in the same package thickness.
In 2018, I have presented the process flow and issues related to handling for 2 side molded WLCSP, using different molding materials and processes. I also indicated the board level reliability results for TMCL and drop test, however these were not completed at the time of the conference.
In the meantime, we do have the results and the analysis of the results for sharing. The presentation will focus on the Surface Mounting process optimization as well as on the final TMCL and drop test results as function of minimum and typical solder quantity. The last part will be the outlook on this activity to bring this to an industrial standard for the selected materials.

Biography
Tonny Kamphuis received his master in Mechanical Engineering at Twente University in 1986. The same year he joined Philips Semiconductors in the field of IC assembly equipment. He worked in Kaohsiung Taiwan from 1991 to 1992, after which he joined the discrete assembly equipment development department in Nijmegen. He has developed die bonders, wire bonders, molding machines as well as all type of handling equipment for both reel to reel and strip to strip based industrializations. Since the year 2000 he is focusing on assembly process development and industrialization for IC again. In 2007 NXP was founded, at NXP, he has filed several patents related and is focusing on package pathfinding.

Advanced Assembly Materials for Enabling Heterogeneous Integration and System-in-Package (SiP) Applications

R. Trichur
Director, Global Head of Advanced Packaging Market Segment
Henkel Corporation, Irvine, United States

Abstract

For a majority of the wafer fabs and applications, as the front-end lithography nodes move towards 7nm and lower, the upfront cost of the photolithography equipment and the total cost of ownership of the process outweighs the benefit gained from this technology. Only less than a handful of manufacturers can continue to invest in the bleeding edge front end lithography technology. Due to technological complexity of such processes, the pace of node shrinkage has slowed down sharply compared to Moore's law. In the last few years, backend packaging technology has moved from being considered an afterthought for assembling the silicon device to the forefront for improving the performance of the packaged device. Mega trends like big data, artificial intelligence, 5G connectivity and autonomous driving applications are the drivers for advanced packaging of semiconductor devices. Advanced packaging enables these next generation devices to have higher bandwidth, faster processing speeds, reduction in form factor, reduction in total cost of packaging, and other benefits depending on the packaging technology used.

Advanced packaging architectures present a myriad of assembly challenges that require innovation in packaging materials and processes. Requirements for packaging density, performance and cost vary between end applications such as mobile, high performance computing and automotive components. Various challenges are addressed by advanced packaging materials in all these applications.

In this paper, we will present the pain points of advanced packaging methods and recent advancements in assembly material technologies for encapsulation using liquid compression molding (LCM), underfills (CUF, NCP NCF), warpage control, electro-magnetic interference (EMI) shielding materials that enable these advanced packages. Advanced assembly material development is critical to meet the stringent performance and packaging requirements for high performance micro-electronic devices.

Biography

Ram Trichur is the Global Head for Advanced Semiconductor Packaging Market Segment in Henkel's Adhesives Technology division. Ram has 19 years of experience in the microelectronics industry covering both the front-end wafer processing and backend assembly processes, 3 patents with over 40 publications and technical articles in leading industry conferences and magazines. Ram received his master's degree in Electrical Engineering from University of Cincinnati and completed his executive education in business management from Stanford University's Graduate School of Business.

Low Phosphorus Content Of Electroless-Ni for Power Device

Y. Sakuma
Deputy manager
C.Uyemura & Co.,Ltd., Technical Support Group,
Nagoya, Japan

Abstract
In packaging of power modules and small motors for automobile, surface finishes are required for proper solder joint formation, and Ni/Au or Ni/Pd/Au and so on are generally used as the metallization. As a deposition method of these metals, wet plating is drawing attention because of mass productivity and cost performance. Recently, SiC power devices have been developed to maximize the efficiency of the systems, however it will still take more time for the solution of thermal problems. Therefore some manufacturers has been already starting to evaluate high melting point solder (300 °C or higher). Another technical item to consider is to decrease in Si thickness. In this case, there are some problems regarding increasing wafer warpage after plating, suppression of Sn-Ni IMC thickness and crack after reflow due to the reflow temperature rising by change to high melting point solder. We found that low-P content electroless Ni can solve these issues.

i) Improvement of wafer warpage
According to Ni plated wafer warpage simulation by Stoney's formula, when Si thickness is halved, the amount of the warpage becomes about four times greater. In our previous research, it was revealed that the differences of thermal expansion coefficient of each layer were more dominant than the internal stress of deposited Ni film for wafer warpage. From further investigation, we also found that thinner Ni improved wafer warpage regardless of P content of Ni deposit.

ii) Suppression of Sn-Ni IMC thickness
By rising reflow temperature, increasing of Sn-Ni IMC thickness and cracks are caused in case of conventional middle-P content electroless Ni. Low-P content electroless Ni deposit can suppress the Ni erosion amount than that of middle-P content. These phenomena are considered to be derived from crystal structure of Ni-P deposit.

In this study, we considered the mechanism of technical advantages of Low-P content electroless Ni for thin wafer and high melting point solder.

Biography
Yuichi sakuma was employed at the C.Uyemura&Co., LTD. ,after graduated as Master of Science in chemistry from Kindai university ,Osaka Japan in 2007.

Our company is the world leader in providing a solderable electroless nickel/immersion gold (ENIG) process in the printed circuit board field, and the knowledge and technique for UBM are supported from this background.

Suitable Total Process Integration of Plasma Dicing for Each Device Category

S. Okita
Chief Engineer
Panasonic Smart Factory Solutions, Plasma Dicing, Kadoma, Japan

Abstract

With the evolution of advanced package technology of electronic components and semiconductor, demands have become severe for chip thinning, miniaturization, flexibility, and high reliability [1].
Plasma dicing is a promising singulation technology that dices wafers mounted on ring frames by plasma processing. It can offer many advantages over other dicing methods for thinning / miniaturization of chips, improvement in chip flexural strength, damage-less / particle-less processing and cost reduction [2].
To introduce plasma dicing it is necessary to optimize the total process integration and plasma dicing conditions according to chip size and structure of each device.
For small size devices without TEG on the dicing street, the process flow using photolithography mask is effective. Very small size, narrow streets and odd shaped chips can be realized by plasma dicing. The mask can be removed by ashing, but if there are high bumps, the ashing time will be longer and CoO (Cost of Owner-ship) will be worse. Therefore, Panasonic developed a method to remove the mask in the ring frame mounting state using a chemical without dicing tape damage. As a result, Panasonic have been able to provide a total process that enables mask removal without residue without deteriorating CoO.
In case of dicing street with TEG, singulation can be realized by a hybrid process combining laser grooving and plasma dicing. By using a suitable water-soluble mask for the same method, it was possible to remove the mask without residue after dicing, while forming and protecting the mask on structures such as bumps.

[1] S. Okita, Plasma Technologies Ease Wafer Manufacturing of IoT Devices, AEI February 2017
[2] S Okita, Improvement of the chip flexural strength by the Plasma Dicing technology, 2015 International Symposium on Dry Process

Biography

Shogo Okita is the chief engineer at Panasonic Smart Factory Solutions, currently involving the development of plasma dicing equipment and process as well as the total process integration of plasma dicing.
In 1997, he joined Matsushita Electric Industrial Co.,Ltd. (now, Panasonic Co.,Ltd.) as a process engineer. Since then, he has been engaged in R&D activity and product development and worked in development of various plasma sources and processes for dry etching equipment in the Si & Compound semiconductor, MEMS and LCD devices fields. He is the author of many patents.
He received the B.S. degree in physics from Kwansei Gakuin University, Japan.

Addressing Impact of Shrinking Line/Space Dimensions on PR Strip, UBM/RDL Etch and Wafer Thinning Processes

A. Vijayendran
Veeco, San Jose, United States

Abstract
Moore's law sharpened focus on shrinking gate dimensions to drive performance and cost. This paper explains emerging challenges as Moore's law slows, with focus transitioning to the packaging side as the industry adopts heterogeneous integration and smaller line/space dimensions for better performance.
Technical requirements are more challenging; e.g., the interconnect and bumping process flow is as follows: barrier/seed layer deposition, patterning, plating, photoresist (PR) strip, and etch. Designers are using redistribution layers (RDL) in flip-chip designs to redistribute I/O pads to bump pads without changing the I/O pad placement. Under bump metallization (UBM) enhances reliability by providing the critical interface between the metal pad and solder bump.
Higher I/O density with improved reliability and performance also leads to shrinking line geometries (from >10µm to sub-1µm) along with smaller bump diameter and pitch. As a result, the photoresist becomes more difficult to remove, calling for more effective methods.
Shrinking dimensions pose similar challenges in UBM/RDL etch. A critical requirement is to minimize undercut while removing barrier/seed layers. Higher undercut impacts mechanical integrity while insufficient removal leads to poor yield.
As thinner devices also drive performance and/or optimized form factor, wafers get thinner in MEMS, Power, RF, Image Sensors. Grinding damages the wafer surface, leaving microcracks, residual stresses and edge chipping. A subsequent process is needed to repair the surface, reduce stress and achieve desired thickness. Wet processing has emerged as a preferred method for surface treatment and wafer thinning while offering higher uniformity at lower cost.
This presentation explains technical results for PR strip, UBM/RDL etch and wafer thinning steps.

Biography
Anil Vijayendran earned his MBA from the University of California, Berkeley, and a master's and bachelor's degree in chemical engineering from Massachusetts Institute of Technology. He has served in roles of increasing responsibility in technical, marketing and product development and is currently vice president of marketing of Veeco's precision surface processing business unit, where he leads all end-to-end product management and marketing for the PSP division. Prior to his role with Veeco, Vijayendran was the vice president of technical marketing for MiaSolé and has previously served as the director of product management at Novellus Systems, a Lam Research company.

T. Oppert
Vice President Global Sales & Marketing
PacTech - Packaging Technologies GmbH, Nauen, Germany

Biography
Mr. Oppert is "Vice President Global Sales & Marketing" at PacTech, a manufacturer of advanced packaging equipment for the microelectronics industry and a leading provider of subcontracting services for wafer level packaging & bumping.

Earlier he held positions as Product Manager, Manager Sales & Marketing and Business Unit Manager in the advanced packaging industry. He earned a master's degree in Electrical Engineering from the Technical University of Berlin in 1995.
Thomas Oppert is senior member of IEEE and IMAPS and author and co-author of more than 70 technical papers & publications related to advanced packaging, especially bumping and bonding processes as well as flip chip & laser soldering technology.
He is a member of the Technical Committee of the SEMI Advanced Packaging Conference yearly held during Semicon Europe.

Mechanical Debonding for ultrathin chiplet manufacturing

E. Brandl
Business Development Manager
EVG, St Florian am Inn, Austria

Abstract
In-package integration of heterogeneous silicon to form chiplets is gaining momentum. To use vertical integration wafer thinning is of essence for heterogeneous integration of chiplets. To support the valuable wafer throughout the whole process with high yield, the employed temporary bond to a carrier wafer additionally to the separation must be well controlled and understood. Mechanical Debonding offers the advantage of using a Si support carrier in combination with room temperature debonding. For the intermediate adhesive dual layer systems with an adhesive and a release layer are studied, where the adhesive can be either a thermoplastic or a curable material. This leads not only to divergent process steps at bonding but also to a different behavior at elevated temperatures. Different materials and material classes are compared, therefor metrology for relevant parameters like total thickness variation (TTV) is employed after every critical process step to control the whole process.
In the presentation we will show different temporary bonding integration flows for chiplets, such as needed for heterogeneous integration in fan out devices, as well as high performance interposer packages. In more detail, the thickness evolution during processing and thinning will be reviewed and presented by high resolution thickness maps.

Biography
Elisabeth Brandl is business development manager at EV Group for temporary and adhesive bonding.

She holds a Master degree (DI) in technical physics from the Johannes Kepler University Linz specialized on nanoscience and - technology. During her master thesis at the institute of semiconductor and solid state physics she gained experience for semiconductor processing and nanofabrication.

Innovative Panel Plating for finer line spacing and better uniformity to allow semiconductor or embedded die assembly for Heterogeneous Integration

R. Boulanger
President
ASM Pacific Technology, ASM NEXX, Billerica, United States

Abstract
Panel Plating requirements are much more demanding as more applications migrate from Silicon to Panel assembly such as Panel level Fan Out to leverage the large sizes of the Panels. More recently Heterogeneous Integration like Intel's Embedded Bridge (EMIB) or various other embedded die concepts are also pushing the boundary for typical panel structures. Line widths and spaces less than 10 Microns, thickness uniformity better than 10%, via topology free of voids and the same height as the redistribution lines are critical.

Traditional Panel Plating Tools are mostly for bulk processing and are not designed to handle these additional requirements so a new tool was required to overcome these challenges. An Electroplating process is used with a Single panel per reservoir approach. An overhead transporter will bring the individual panels that will have been pre inserted in a rigid panel holder designed to handle large currents as well as reduce the warpage to a series of plating reservoirs as well as pre and post processing steps with the tool .

The first process is to reduce voiding by removing all air in a vacuum chamber and then inserting degassed water in the same chamber to "prewet' the panel. The Plating cells are customized for each metal layer but include a mechanism to allow the panel to be lowered in a structure with a shield to better align the electrical current between the material anodes and the Panel Holder as well as a louvered shear plate that is activated at a certain frequency to improve the seed layering. This whole mechanism needs to be very close to the panel and minimize any warping.

This presentation will demonstrate that it is possible to achieve better line density, bump thickness uniformity and void free vias to allow semiconductor like assembly for Heterogeneous Integration on a standard Printed Circuit Board instead of more expensive semi additive processes or silicon interposers

Biography
Richard Boulanger graduated as an Industrial Engineer from Ecole Polytechnique of the University of Montreal. He worked for IBM in Canada and in the United States for Semiconducotr Assembly and Ceramic Processing. He held several positions including Site Quality manager, Memory Business Unit manager and Director of Strategy.

He then worked for Universal Instruments Corporation as a Vice Preseidnet of a new division to focus on Flip Chip asembly machines. Afterwards, he left for Europe as the Die Bonder Vice Presient of Kulicke and Soffa and General manager of Alphasem and then as CEO of ALSI who design Laser Dicing and Grooving machines that was rhen sold to ASM Pacific Technology.

His present positio is President of ASM NEXX who design and build Wafer and Panel Plating Tools

Advanced Plasma Surface Activation for Hybrid Fusion Bonding

T. Schmidt
Product Manager
SUSS MicroTec, Bonder Division, Sternenfels, Germany

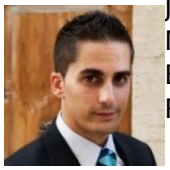
Abstract
Wafer bonding can be considered as one of the key enabling technologies for future 3D devices in the microelectronic/photonic system industry. However, complementary metal-oxide-semiconductor (CMOS) structures present on those devices require dedicated and compatible low temperature (LT) bonding schemes such as hybrid bonding.
In LT bonding research hybrid bonding has lately become more and more the focus of attention, due to distinct advantages especially within semiconductor processing.
In this paper SUSS MicroTec introduces a novel highly flexible approach for atmospheric plasma surface activation that allows for versatile full wafer treatments and high bonding energies. The absence of directed ions and electrical fields in general translate in full CMOS compatibility of the new plasma concept, making it especially suited for hybrid bonding. The described surface activation approach can be optionally integrated in automated bond cluster platforms from SUSS MicroTec via an innovative tool integration concept also presented in this paper. The integration concept comes along with distinct advantages over vacuum plasma, such as increased throughput, higher cleanliness, lower tool footprint, reduced wafer handling, lower cost of ownership etc. as demonstrated in the scope of this publication.
The highly flexible chemistry that can be used within the new plasma activation approach also enables metal-oxide removal, i.e. reduction of copper oxide surfaces present at wafer-to-wafer (W2W) and collective die-to-wafer (D2W) hybrid bonding applications for 3D integration schemes.

In this work surface free energy (including polar and dispersive components), defectivity, bond-strength, surface hydration and the dependence of surface pre-treatment have been studied. Water contact angles (WCA) down to <7°C and free surface energies in the range of 77 mN/mm have been obtained, resulting in wafer bond strengths for low temperature fusion bonding significantly exceeding 2 J/mm².

Biography
Thomas Schmidt is Product Manager in the Bonder Division of SUSS MicroTec in Sternenfels. After his graduation in Microsystems Technology at the University of Applied Sciences in Kaiserslautern he has held various positions in MEMS/semiconductor processing and has lectured on advanced lithography as well as on MEMS and CMOS fabrication.

Since December 2017 Thomas Schmidt is a member of the Bonder Division of SUSS MicroTec with responsibility for the product line "Permanent Wafer Bonding" focusing on automated cluster platforms. This platforms address established bonding techniques for MEMS/packaging as well as hybrid fusion bonding for advanced packaging.
Thomas Schmidt has authored and co-authored several papers on various topics, including microthermoforming and microoptics.

Packaging of a MOEMS LIDAR sub assembly for distance metering on a 3D housing



J. Abdilla
Manager Process Development R&D
BESI Austria GmbH, Process Development R&D,
Radfeld, Austria

Abstract
MOEMS technology has undergone swift progress in recent decades. The ever prominent need for miniaturization and low cost has led many manufacturers to resort to MOEMS to address the optical requirements in their respective areas. One prominent use for MOEMS is in laser beam scanning systems and it is the laser sensor that most tech and car companies see as an essential component for self-driving cars.

This paper addresses the challenges of packaging MOEMS actuated micro mirrors (developed by STM) to create a laser scanner sub assembly for distance metering, on a standard die bonding platform embarked upon during the L4M2 ENIAC funded project. The complexity of the packaging is attributed to several issues, from the handling of the 3D solid metal housing, requiring high precision and versatility when compared to standard flat substrates common in semiconductor assemblies, to various sub assembly procedures and handling of delicate MOEMS micro mirrors with keep-out zones and flex substrates. Such MOEMS devices also require a low defect yield in order to obtain a robust, reliable functional system. As such advanced metrology was integrated into a BESI die bonder in the form of a 3D image capturing system based on white light interferometry, capable of providing fast, real time, in-situ inspection of crucial parts, which are not possible to detect using conventional 2D cameras. Tilt measurement and bond line thickness measurement are all software features which were developed at BESI to analyse the 3D images and feedback the data for process auto correction by means of a 6-axis bondhead with possibilities of varying x, y, z, theta, Y-tilt and X-tilt positions. A new clean room kit system installed in the die bonder was also developed to address ISO class 4 and lower since MOEMS are highly susceptible to debris and foreign matter.

Biography
Jonathan Abdilla is Manager for Process Development at Besi Austria GmbH. He has a degree in Mechanical Engineering B.Eng (Hons), an MBA (Executive) from the University of Malta and a Diploma in Computing Information systems from the University of London. He has thirteen years of experience in the assembly & test of semiconductor devices. Prior to joining Besi Austria in 2014, Jonathan worked as an Assembly Line Process Engineer at STMicroelectronics Malta from 2006 until 2014. At Besi Austria, he is responsible for the Process Development group which focuses on research and development of advanced packaging and new pick and place technologies. Jonathan is also involved in coordinating Besi Austria's participation in several national and EU funded projects.

Half-inch FOWLP Process Line utilizing Minimal FAB

K. Miyake
Executive Officer
PMT Corporation, Fukuoka, Japan

Abstract
Minimal fab technology is a different method of semiconductor production. Integrated chip (IC) manufacturing facilities usually require billions of dollars in investment, which can be provided by only a few companies with the potential for high capital investments. Moreover, the conventional IC fabs require months to set up; whereas, minimal fabs can be up and running in days.
The minimal fab does not require a clean room environment. Instead, the wafers are placed in a secured, clean-room-like container termed as the “shuttle” and loaded on the process stations. The transparent red material makes the wafer visible and blocks the UV radiation. It has been noted that the minimal fab uses maskless exposure technology, which means the traditional photomask preparation time (which typically takes months) can be avoided. Minimal fabs use direct draw and exposure, which makes it possible to avoid the photomasks. Furthermore, as the production is on wafer-to-wafer basis, the feedback is rapid.
From an operational perspective, owing to the high capital cost and duration involved in set-up, conventional fabs require 24 hours of operations. Whereas, minimal fabs are able to operate effectively based on flexible production and working hours. Furthermore, minimal fabs require less time to convert research into production. Moreover, as minimal fabs do not require clean room environments, and as their systems are designed to be energy efficient and smaller, power consumption is estimated to be just one-tenth of that of conventional IC fabs. Therefore, Minimal fabs prove to be both operationally flexible and cost-efficient.

Half-inch FOWLP Process Line utilizing Minimal Fab will be presented.

Biography
Dr. Kenji Miyake received his Ph.D. degree in the Graduate School of Science and Engineering from Yamaguchi University in Japan.
He worked for Texas Instruments Japan for 28 years, since 1980.
He conducted many international IT projects as Asia Pacific
Assembly Automation Manager in Texas Instruments Japan.
He moved to PMT Corporation from Texas Instrument Japan in 2010. He has engaged in Minimal Foundry as Executive Officer, PMT Corporation.
He has contributed the international semiconductor symposiums that are AEC/APC (Advanced Equipment Control/Advanced Process Control) and ISSM (International Symposium of Semiconductor Manufacturing) as Program Committee since 2005.