Advanced Packaging Conference (APC)

S. Kroehnert
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Biography

Dipl.-Ing. Steffen Kröhnert received his master degree in Electrical Engineering and Microsystem Technology at Technical University of Chemnitz, Germany, in 1997. In the same year he started his professional career as Development Engineer in the Corporate Package Assembly, Interconnect and Test Development Center for Semiconductors of Siemens AG in Regensburg, Germany. After carve out of the Semiconductors Business Unit to Infineon Technologies AG in 1999, he worked as Project Manager and moved to Infineon Dresden GmbH & Co. OHG in 2002 to support local setup of Package Development Department for Memory Products. He became R&D Area Manager Component Development and took over Technology Platform ownership for FBGA products. From 2006 he was working as Senior Manager in Qimonda Dresden GmbH & Co. OHG, the carve out of the Memory Products Business Unit of Infineon Technologies. Begin of 2007 he was assigned to Qimonda Portugal S.A., the largest Packaging, Assembly and Test facility of Qimonda, in order to setup and lead the Package Development team at this volume production site. Since 2009 he is Director of Technology at NANIUM S.A. in Vila do Conde, Portugal, the largest independent Semiconductor Packaging, Assembly and Test Foundry (OSAT) in Europe. Steffen is author and co-author of 23 patent filings in the area of Semiconductor Packaging Technology. He is member of IEEE CPMT, IMAPS, MEPTEC, SMTA, VDI, VDE and GPM. He actively contributes as Co-Chair to SEMI Europe's Advanced Packaging Conference (APC), as Technical Committee member to IEEE Electronic Components and Technology Conference (ECTC), IEEE Electronics System-Integration Technology Conference (ESTC) and IMAPS European Microelectronics Packaging Conference (EMPC), and as Assistant Technical Co-Chair (Europe) to IMAPS Device Packaging Conference and International Symposium on Microelectronics.

Innovative Interconnects in System in Package Drive Application

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Abstract

Infineon Regensburg is one of the leading locations worldwide for innovations of assembly and packaging. The investigation of innovative interconnects is one of the core competencies. We will provide an overview of recent developments plus an outlook to the future.

In 2004 Infineon introduced the TSLP package into the market. This was not only a thin package, but also a package that allowed 4 times smaller pads compared to a VQFN package. The small contact pads of the TSLP allowed improved heat dissipation and improved signal integrity. IFX Regensburg was the location where chip embedding technologies were investigated and introduced in the market. The first example is the eWLB technology, where chips were embedded into a mold compound. The eWLB fan-out assembly and

packaging technology was introduced into market for mass production in 08/09. This was the first time that a redistribution layer was applied to a molded chip to get a fan-out routing. Meanwhile we extended this eWLB technology further towards 3D system integration. Work included introducing integrated antennas TEV (Through Encapsulant Vias) and the EZL (embedded Z-line) interconnect technologies. A novel package technology with innovative interconnects was investigated and developed also for power devices e.g. for DrBladeTM. This package technology was a package without wirebonds and flipchip bonds. With DrBladeTM, which includes the innovative packaging technology, Infineon is among the 4 finalists of the innovation award of the German Economy 2015
In future low parasitic interconnects are required for optimum signal integrity as well as for unnecessary heating. A coherent development taking into account chip, package, and board is needed. We present examples that summarize the outstanding capabilities of various packages and corresponding interconnect types, e.g. the chip embedding Technologies to demonstrate that assembly and packaging is becoming of ever more importance as product differentiator.

Biography
Bernd Römer received his diploma in mechanical engineering and precision engineering from the University of Applied Sciences Giessen/Germany in 1983.
He joined Infineeon Technologies former Siemens Semiconductors in 1983.

Bernd had various engineering and management positions in the area of semiconductor package / product development, technology & innovation, research & development and production.
As Senior Principal Packaging and System Integration he is the leading a Trends & Integration conpepts team within the Infineon Packaging Innovation group.
Bernd Römer is an active member in different organizations like ITRS TG Assembly & Packaging, IEC, JEDEC, and JISSO International Council (JIC).

Chip Interconnect in LED Packages - Methods and Materials

I. Galesic
R&D Engineer
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Abstract
A wide variety of interconnect methods are applied in packaging of light emitting diodes (LED). The technologies mostly coming from IC industry and using LED specific materials for optimized and stable optical performance. Development activities have to consider that the LED market segments automotive lighting, general lighting and consumer electronics have different requirements in terms of performance and cost.
Important aspects for the selection of appropriate substrate and interconnect materials are power class and thermal management as well as reliability and life time requirements. In terms of quality the understanding of degradation mechanisms in LED packaging is a crucial factor. The challenge of materials development for mass production of high brightness LEDs is to use inexpensive materials with stable optical properties (no discoloration) under operating and aging conditions (heat, current, light, humidity and reactive gases). In order to contribute to the continuous increase of luminous efficacy of LEDs the reflectivity of packaging materials (metals and polymers) have to increase.
Adhesive bonding and soldering are established techniques for LED die attach, whereas sintering is less common. Adhesive bonding is carried out with electrically conductive or insulating adhesive materials based on polymer matrix. For chip soldering pastes and thin film techniques are applied. Adhesion of the LED die to substrate plays a key role for product performance and lifetime. In particular when forces caused by expansion or shrinking of polymer materials during temperature change "pull" at LED chip.
The LED chip technology can be split into top emitting and side emitting type. For top emitting chips usually a metal based joint is formed, whereby for side emitting chips transparent or high reflective adhesive materials are needed. Additionally, the side emitting type requires a high reflective substrate surface like Ag platings, which has a limited corrosion stability.

Biography
Ivan Galesic is key expert for backend technology and materials innovation at Osram in Regensburg, Germany. He received a Ph.D. in 2000 from the Institute of Inorganic and Analytical Chemistry at University of Frankfurt am Main. In the same year he joint Infineon Technologies in Villach (Austria) and was responsible for wafer back-side metallisation and thermal processes (CVD, annealing and alloying). From 2003 to 2007 he joined Infineon in Regensburg and he developed thin-film chip soldering for power packages. In 2007 Ivan Galesic started working at Osram as R&D engineer for plasma processes. He is currently responsible for development and implementation of LED package substrate materials and platings (galvanic and electroless).

Development of ultra high speed on-chip Optical Interconnects by state of the art Si etching process and Nano Imprint Lithography

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Abstract
The computing power of the chips is progressively increasing, which makes the speed of the conventional interconnections lag behind. Experts are adding more and more active devices by incorporating various 3D chip integration techniques (e.g. C2C, C2W, TSVs inclusion, etc.). So, to get maximum advantage of the speed of active devices, the interconnects must catch up with the speed and optical interconnection link could be the best choice for this.

Within the project of '3D Chip Stack Intraconnects' at TU Dresden, the possibility of fabricating an optical connection link between two (or more) active layers of the chip is explored. Depending upon the TSV sizes and connection link possibilities, a desired shape of the connection is carved on the Si. A state of the art etching process, yielding positive profiled structures, is developed in order to achieve variable angles depending on the requirement of the connection shapes of respective TSVs. The etching process is the combination of various types of dry plasma etching processes. It was optimized for desirable angles and low surface roughness to improve the efficiency of the final optical interconnection link. This Si imprint master is then used to develop polymer stamps. Using these stamps, pre-fabricated air TSVs can be filled to provide ultra high speed data, of the order of a couple of hundreds of Gbps, interconnection link. The final optical link is prepared under vacuum using Nano Imprint Lithography and transparent polymer SU-8. A set of simple SU-8 filled TSVs were examined for their optical signal carrying capacities and the primary results have shown excellent connectivity (loss of less than 2 dB).

Inclusion of photonic devices and polymers for the interconnects and waveguide last process, gives a novel approach to the conventional (C2C, C2W, etc.) fabrication techniques. This More-than-Moore approach is driving advanced packaging towards improved efficiency, high yield, low parasitic and inexpensive solution.

Biography
The author's full name is Sujay Ashok Charania, was born on 27th July, 1990 in Ahmedabad, India. He achieved his Bachelor of Engineering in Electronics and Communication in 2011 with distinction from Gujarat University, India. After that the author moved to Germany to work on his area of interest and joined M.Sc. in Nano Electronics System at TU Dresden.

He has worked on a project titled "Design of a compression system using ADV212 in raw pixel mode" at SAC-ISRO, India. At TU Dresden he has worked on '3D Chip Stack Intraconnects' project as a student research assistant. At present he is working on the development of Laser diode drivers, which will be used with the structures discussed in the paper to prepare very high speed on-chip optical interconnects.

3D MEMS WAFER LEVEL PACKAGING USING TSVs & TGVs

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Abstract
Future demand for smaller size and lower cost MEMS devices will inevitably lead to the need for fully integrated sensor solutions which are much smaller than today's available form factors. In the area of 3D MEMS Wafer Level Packaging, Silex Microsystems has been focusing on developing solutions for heterogeneous integration and is now presenting interconnects with Through Silicon Via (TSV) and Through Glass Via (TGV). These 3D interconnection technologies enable vertical chip stacking by bonding, decreasing the packaging size (highly dense packaging) as well as the costs, thanks to the reduction in volume and mass. The TSVs enable shorter redistribution layers (RDL) and the smaller size translates to better performance since the signal travels a shorter route and parasitic capacitances decrease, thereby further improving the system performance.

Silex will describe the manufacturing of metalized TSVs and TGVs for RF applications, where characterization showed low insertion losses for both TSVs and TGVs, with less than -0.04 dB per coplanar TSV at 5 GHz frequency, and around -0.006 dB at 5 GHz for the TGVs. Further, in a joint effort with MASER Engineering, an extensive reliability and failure analysis was conducted, focusing on understanding TSVs' failure mechanism. X-ray inspection was used to quickly identify defective TSVs. The ongoing quality and reliability investigation now focuses on identifying weak links through the application of high currents and the use of heat tomography technique to detect hot spots.

A through molded via element was also created in collaboration with Fraunhofer IZM, using Chip in Polymer (CiP) reconfigured wafers, where the TSV interposers and CMOS biosensor chips were interconnected using a PCB-based redistribution layer, enabling low-cost heterogeneous integrated packaging, as well as separation between electrical connections and the active biosensor's wet I/Os. Silex will also present a solution for thin glass wafer handling.

Biography
Jessica Liljeholm, born 1987, received the Master of Science degree in Chemistry and Chemical engineering from Royal Institute of Technology (KTH) in 2011. She did her M.Sc. work at Expancel's R&D department and started to work at the same department as an Analyst engineer. Thereafter she started at Silex Microsystems, the largest pure play MEMS foundry, as a R&D Project Manager in 2011. She has been active in several of Silex customer programs as well as EU programs related to new TSV developments such as CAJAL4EU and EPAMO. She is now starting at an industrial PhD position at Silex Microsystems, which will aim for research within polyMEMS - Polymer-Based Integration Platforms for Future Generation Miniaturized Heterogeneous MEMS Systems. In 2013, she received the Best Paper for the 2013 IWLPC in San Jose, CA.

T. Oppert
Vice President Global Sales & Marketing
PacTech, Nauen, Germany

Biography
Biography Thomas Oppert

Mr. Oppert is "Vice President Global Sales & Marketing" at PacTech in Nauen, Germany, a manufacturer of advanced packaging equipment for the microelectronics industry and a leading provider of subcontracting services for wafer level packaging & bumping.

Earlier he held positions as Product Manager, Manager Sales & Marketing and Business Unit Manager in the advanced packaging industry. He earned a master's degree in Electrical Engineering from the Technical University of Berlin in 1995.

Thomas Oppert is a senior member of IEEE-CPMT and IMAPS and author and co-author of more than 60 technical papers & publications related to advanced packaging, especially bumping and bonding processes as well as flip chip & laser soldering technology.

He is an active member of the Organizing Committee of the SEMI Advanced Packaging Conference yearly held during Semicon Europa.

A New Alternative Low Cost Package Solution for High Bandwidth Memory PoP

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Abstract
Package-on-Package (PoP) technology was widely used in mobile phones for the bottom flip-chip chip-scale package (FCCSP) digital AP to stack with a top wirebond low power double data rate (LPPDDR) chip-scale package (CSP). The bottom FCCSP package form factor and its pin up of top solder balls were limited by the LPDDR BGA matrix, which had been defined by JEDEC. Because of high-bandwidth memory requirements for smart phones, a lot of new PoP solutions to accommodate more I/Os between the top LPDDR memory package and the bottom digital application processor package are becoming a reality.

In this study, HBW PoP is a 3D structure that combines an "organic substrate interposer" with an embedded mold compound in the bottom package as the connection interface with the top package is introduced. This design will bring benefits, not only providing more I/Os, but also more flexibility to accommodate different package sizes to stack on the top, for non-LPDDR devices like PMIC, RFIC, etc., to form multi-functional system-in-package (SiP) modules, or even the increasingly important applications of wearable electronics or the internet of things (IoT). That is, compared with a traditional PoP without an interposer, an additional organic substrate interposer (with full matrix I/O pad layout) can build a fully functional system and achieve the wide I/O memory goal. This structure, however, will bring some major assembly challenges, such as package warpage, mold compound voiding, and in-line process defect detectability issues. The solutions to solve those defects were developed with considerable engineering efforts.

In the study, many mechanical simulation models and design of experiments (DOE) studies were used. Moreover, mold compound and substrate core material properties (such as the coefficient of thermal expansion [CTE] or modulus property adjustment) can effectively reduce package warpage. Subsequently, improvement of over package cost were addressed in the study.

Biography
Jensen Tsai is the Deputy Director of Engineering Center in SPIL (Siliconware, Taiwan), which is 3rd biggest assembly house in the world now.
He has over 18 years of job experience on semiconductor industry, especially focus on wire bond and flip chip advanced assembly technology.

A New Reliable Adhesion Enhancement Process for Directly Plating on Molding Compounds for Package level EMI Shielding

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Abstract

Plating on molding compound is a relatively new field which could open up new package designs. One major application is conformal self EMI shielding of ICs (package level shielding). This is currently done mainly by metallic cans, however, this technique also increases the space requirements and reduces flexibility of component layout on the PCB, that would not be suitable to handset products.
An alternative and more space saving approach is "Conformal Self EMI Shielding (package level shielding)". Also this metal layers can perform not only for EMI shielding but also for good heat spreader, compared to metal cans.
A popular method to provide a metallic seed layer for "Conformal Self EMI Shielding" is sputtering and conductive paste, however, in order to make it more cost effective and feasible for mass production; there is a need for classical electroless plating metallization along with adhesion enhancement process. While in some instances conductive paste and sputtering metallization will provide adequate adhesion - it has the technical drawbacks of poor sidewall coverage and limited metal layer thickness that would not fulfill for lower frequency noise shield. As a result, scale- up for mass production is relatively difficult and costly.
Classical electroless and electrolytic plating metallization are much more desirable but have been so far limited by insufficient adhesion by existing chemical treatment. In this paper we will present a new approach, where components encased by molding compounds are directly coated with an electroless copper or nickel plating layer. By this method spatial requirements are minimized.

Biography

After receiving a bachelor degree for Metallurgical Engineering from Inha University in Korea, K.Kim joined MacDermid Korea as a technical service engineer for PCB industry plating in 2001.
He joined Atotech Korea in 2004 and was in charge of technical sales of plating technology to organic interposer and mother board suppliers in Korea until 2007. He joined Surface Technology Team of Atotech and developed 'Non-Etching Adhesion Promoter' in China until 2012. Currently he has been developing adhesion promoter for plating on molding resin materials since 2012 when he joined Molecular Adhesion Technology team of Atotech, located in USA.

Testing solder ball alloy materials for reliability improvement in eWLB technology

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Abstract
Depending upon the end user application a specific focus in terms of Drop Test, Thermal Cycling on Board is required and the chosen alloy has often been tailored for this use. Furthermore, alloys with similar composition but from different suppliers do not necessarily have equivalent performance and behavior. This raises other questions such as supply chain, second sourcing and IP considerations.
The present work aims to evaluate and compare the processability and reliability of solderballs with a standard SAC305 and a similar alloy with dopants designed to enhance drop shock performance. Two nominally identical alloys of the reliability enhanced solderball from different suppliers are employed to respond to the question of second sourcing.
Test vehicle #1 was utilized in a complimentary study using an additional 2 solderball alloys expected to improve drop shock performance -Ni doped SAC (2.0Ag,0.75Cu,0.07Ni) and SAC (1.0Ag, 1.0Cu). Alloys with a reduced silver component and increased level of copper are well known to improve drop shock performance however a balance must be achieved with Thermal Cycling on Board, since this type of alloy usually displays poorer TCoB performance.
Regarding the SAC 305 alloys, it was noted that the presence of dopants slightly postpones the first fail appearing in terms of drop shock and a slight performance impact in terms of TCoB. With respect to the comparison between two suppliers (for sourcing purposes), although it seems there is a better performance in terms of drop shock resistance from one of them, more pronounced in TV #2, the same cannot be state about TCoB results.As for complementary evaluation over Ni doped SAC (TV #1), it achieved the higher value of drops until first fail occurs as well as the failure rate along the time. By other side, this alloy reached the worst performance on thermal fatigue which indicates the combination of Ni addition and a medium Ag percentage cannot overcome a SAC305 (doped or not) alloy.

Biography
Hugo Barbosa have been working at NANIUM for approximately two years as R&D Materials Development Engineer. He received a MSc. degree in chemical engineering from Aveiro University in 2013.

Excimer Laser patterning for high density interposer and substrate fabrication

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Abstract
Mathias Böttcher, Michael Töpper, Karin Hauck, Martin Wilke, Juliane Krause, Klaus-Dieter Lang

Within "More than Moore" concepts interposer based packaging technologies, known as 2.5D/3D system integration, open up a wide range for miniaturized multi-functional system solutions mostly known as System in Package (SiP). Pending on the final application dedicated interposer concepts are available for grabbing multiple active components, fabricated by using different technologies and materials, e.g. sensors, logic, RF and memory-ICs, as well as passive devices, including antennas. In many cases the application of high density multi-layer wiring and µ-pillar interconnects are needed.
In order to support further system miniaturization and extension of system performance on one hand and to meet costs and time to market challenges on the other hand the development of organic interposer applications as well as the use of Excimer laser patterning technics for high density substrates is at high interest for R&D, prototyping and volume production.
A short outline of high density substrate technologies developed and available at IZM will be presented. Starting with a brief discussion of basic elements of interposers, several technology concepts developed and validated for high density interposer applications will be shown. The pro and con of different process approaches will be discussed. Focus will be on the application of laser technology compared to photo- and etching-processes. Especially the strong influence of the polymeric material to the system functionality and reliability will be given. Challenges related to µ-pillar applications and high density wiring will be addressed and generic results will be presented. Using the variety of interposer technologies investigated at IZM a high level comparison of challenges and opportunities will be shown and discussed.
A brief outlook of future development work for system applications will be given.

Biography
Mathias Boettcher started his carrier in 1982 at the Dresden University of Technology where he got his PhD in electrical engineering. In 1997 when Mathias joined the young AMD Team in Dresden and was deeply involved into the selection, transfer and start-up of a new C4 bumping technology for microprocessors at AMD's FAB30. In 2002, he got a new opportunity at Infineon and was the technical leader of the R&D team for memory module development at the Dresden site and later on in a similar position at the production site at Qimonda Malaysia. Since 2009 Mathias is leading the development team at Fraunhofer IZM-ASSID focusing on wafer processing for 3D-System integration, covering TSV, RDL and Bumping.

A. Longford
Consultant
PandA Europe, Lambourn, United Kingdom

Biography

Andy Longford (C.Eng FIET)is Managing Partner (CEO) and Senior Consultant at PandA Europe, a technical & market Consultancy Company involved in Semiconductor chip Packaging and Electronics Interconnection. He has worked on chip package designs for a number of years and is currently involved with emerging chip package design analysis and technical support work. He is a member of a number of technical committees, including SEMI Europe (APC), and also provides Secretariat Services for IMAPS-UK.

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The Growth of Advanced Packaging: An Overview of Technologies, Applications and Market Trends

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Abstract
The semiconductor industry has followed Moore's law, scaling the CMOS technology to smaller and more advanced technology nodes while, at the same time, reducing the cost. The industry is reaching now limitations in continuing this scaling process in a cost effective way. While technology nodes continue to be developed and innovative solutions are being proposed, the investment required to bring such technologies to production are significantly increasing. To overcome these limitations, new packaging technologies have been developed, enabling integration of more performing as well as various type of devices within the same package.
Today, several different packaging technologies are available in the industry: from encapsulation based technologies (MEMS and sensors, wafer level optics) to fan-in and fan-out packages, from embedding dies within organic substrates to flip chip bumped packages and 3D stacked devices using through-silicon-via interconnect technologies. The suitability of each of these platforms and market adoption will depend on the final product and application needs.
This paper will provide an overview1 of current trends seen in the industry across all the packaging platforms (3D WLCSP2, WLCSP3, FanOut4, Embedded Die4, Flip Chip5 and 3DIC6). Packaging technology evolution, including interconnect and substrate trends, challenges, materials needs and applications will be presented. Industry landscape and dynamics will be also reviewed. Presentation will include examples of teardowns to illustrate the latest packaging techniques currently available for various devices.

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(6) Yole Developpement, 2.5D & 3DIC Business Update, 2015

Biography
Rozalia has 24 years of experience across various industries, from industrial to electronics and semiconductors. For more than 17 years, she was involved in the research, application and strategic marketing of Advanced Packaging and 3D Interconnect, with global leading responsibilities at specialty materials (Rohm and Haas Electronic Materials), equipment (Semitool, Applied Materials, Lam Research), device manufacturing (Maxim IC) and OEM (NCR) organizations. In 2013 she joined Yole Developpement to lead and further grow the Advanced Packaging and Semiconductor Manufacturing activities within Yole.
Throughout her career, Rozalia has been very actively supporting various industry activities: Program Director of EMC3D Consortia, chair of several 3D Committees and activities (ITRS, ECTC, IMAPS DPC), chair Advanced Packaging Committee at ECTC, IMAPS DPC General Chair, Global Semiconductor Forum General Chair and several additional memberships with SRC IPC, CPMT, IWLPC, EMPC, EPTC, 3DIC committees.
She has won several awards, including 2006 R&D 100 international award for Electrodeposition of SnAgCu wafer bumping, 2013 IE Business School Entrepreneurship Project of the Year and winning project at Fudan University Venture Day in Shanghai for developing affordable renewable energy solutions to address rural electrification in Africa and Dale Carnegie's "The Highest Achievement Award" . She has over 60 publications (including 3 book chapters focused on 3D IC technologies), several keynotes and panel participations, and four patents.
Rozalia has a Global Executive MBA from Instituto de Empresa Business School (Spain), M. Sc. In Management of Technology from KW University (USA) and an M.Sc in Chemical Engineering from Polytechnic University "Traian Vuia" (Romania).

New processing scheme for embedding and interconnection of ultra-thin IC devices in flexible chip foil packages

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Abstract
The paper will present the concept and the successful technological demonstration of a new processing scheme for the manufacture of flexible chip foil packages and experimental data on the mechanical behavior of thin silicon embedded in polymer laminates.
Technological Concept:
By a first processing step thin or ultra-thin microelectronic devices are bonded onto a film substrate in face-up orientation. Then devices are embedded in a planar polymer layer, which can be structured by a photolithographic process. After opening the vias above the IC contact pads a thin film redistribution process is carried out, which results in a fan-out routing for the I/O contact pads. Finally the top wiring layer can be covered by a polymer film layer. Such concept results in a chip-foil-package where fragile ICs are embedded in the center of a three layer plan-parallel polymer laminate of an overall thickness below 150 µm.
Technical Results
We prepared 25µm thin microcontroller IC (Microchip, PIC16LF1519). For the first demonstrators we used sheets of polyimide films with a thickness of 50 µm and a diameter of 150 mm, which were temporarily attached onto silicon carrier wafer. This allows photolithographic patterning for a large number of chip packages in parallel. We used sputter deposited copper films for interconnects and top wiring layer. Finally the polyimide films were released from the carrier and cut into separated chip-film-packages.
It was verified that a high yield has been reached for the electrical interconnects. Detailed results will be presented in the paper.
Furthermore, it was experimentally confirmed that embedding of 30 µm thin silicon samples in polymer laminates nearly triples the fracture strength of the fragile silicon components. This result is in very good agreement with FEM calculations of the deformation of thin silicon embedded in polymer films.

Biography
Christof Landesberger received the diploma degree in physics from Ludwig Maximilians University in Munich. He joined Fraunhofer Institute in Munich in 1990. Since 2000 he is heading the research group "substrate preparation and handling" at Fraunhofer EMFT. He has been working in the field of ultra-thin silicon since more than 15 years and prepared more than 20 patent applications in the field of processing techniques for ultra-thin semiconductors. His current research topics are focusing on new packaging technologies for ultra-thin semiconductor devices and handling techniques for fragile substrates by means of electrostatic forces. Christof is chairman of the international workshop "Thin Semiconductor Devices" (www.be-flexible.de) since year 2000.

Intermetallic Coverage (IMC) in Cu and Ag Ball Bond

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Abstract
Gold,Cu,Pd coated Cu(CuPd and alloyed Ag bonding wires are commonly used for inter-connection in integrated circuits. Though Au wire is still considered to be good in reliability, corrosion resistance and high productivity, rising cost of it leads to the trend in using other types of wires. Due to inherent stiffness and hardness Cu and CuPd wires induce high stress on the bond pad and underlying structure. This pave ways to investigate on Ag based bonding wires. Where Ag wires have issues on free air ball (FAB) morphology. In addition, when bonded to Al bond pad, both Cu and Ag ball bond reliability is not as good as Au bond. Among the factors that contribute for better reliability, as intermetallic coverage (IMC) was well established in Au ball bonding in the packaging industry by wet chemical etching method, it is vital. The rule of thumb for a reliable bond in Au ball bonding is to attain greater than 80% IMC (gold aluminide) and 5.5 g/mil2 ball shear at time zero. There is no clear method adopted to measure the IMC in Cu and Ag ball bonds, either with alloyed or coated wires, particularly when bonded to Al bond pad. The paper enumerates a cost effective and quick procedure to observe the IMC in Cu and Ag ball bonds when bonded to Al pad metallization. In Au ball bonding at time zero, gold aluminide nucleates in a fraction of micron. Whereas, Cu and Ag ball bonding nucleate with copper aluminide and silver aluminide in nano-meter scale. Therefore, to observe the aluminides clearly, a pre-thermal treatment is needed. The pre-treatment ranges from 150□C to 250□C for 30minutes up to 5hours. Similar to IMC study of Au ball bond, Al bond pad is dissolved using 10 to 20 vol% KOH or NaOH solution. Later, topsy-turvy the Ag ball bond to observe the silver aluminide. time zero and hence, ball shear between 8 and 11 g/mil2 is recommended for good reliability and bondability.

Biography
B.Senthil Kumar received the B.E. in Mechanical engineering from University of Madras, Chennai, India and the M.S. degree in Precision engineering from the Nanyang Technology University (NTU), Singapore. He is a Staff Engineer for Heraeus in the bonding wire R&D Department, Hanau, Germany. He was the senior engineer for Infineon Technology Singapore to develop a Copper wire bonding process development for Automotive packages. His current efforts include developing fine copper and silver alloyed wire for various application related packages. He had published and presented six technical papers at advanced package conferences. He has a total of 15 years of semiconductor industry experience.

Application of 3D integration technology to X-ray detector read-out chip

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Abstract
We report on application of the 3D integration technology to the specific type of the X-ray imaging detectors. Similar work was already performed by CEA LETI, France and CERN, Switzerland. The motivation is a significant reduction of the dead space between X-ray chip modules. Originally, this type of chip uses wire bonds as interconnection to ceramics substrate. We replace the wire bonds with TSV. The read-out chip was developed by CERN electronics department and fabricated in IBM foundry, USA. Read-out chip is premade with Through Silicon Via (TSV) landing pads in M1 metal layer. Together with Fraunhofer IZM institute, Germany, we are designing and fabricating TSVs in the read-out chip, Re-distribution layer (RDL), and PCB substrate. The end system will be a stack of X-ray sensor bump bonded to read-out chip which is on other side bump bonded to the substrate. Substrate is LTCC ceramics or PCB board designed in the course of this work. When designing the TSV structure, a challenge was to choose the ratio between thickness of the chip and diameter of the TSV. A thicker chip is more rigid but it would also require larger diameter of the vias. The RDL is designed on the back side of the read-out chip without using an interposer. RDL is designed in the single layer in order to reduce the complexity of fabrication. The challenge was to route all the signals in the single layer at the same time leaving enough space for bump pads. The RDL is the possible source of the digital signal leakage. This effect was modeled analytically and sources of leakage are identified. An additional challenge was to test the chips during fabrication. The plan is to use a probe station with the probe card accommodated to the bump pad structure and to test the chips in wafer at the technology step after RLD deposition. The presentation will give details of the challenges and solutions.

Biography
Milija Sarajlic graduated in Physics from Belgrade University, Serbia in 2001. He joined Institute for Microelectronics in Belgrade where he worked on the development of Silicon based pressure sensors, photodiodes, chemical sensors and photonic micro and nanostructures. In 2013 he joined DESY Detectors Group where is currently working on the application of 3D integration technology to the X-ray pixelated detectors. He has more than ten years of experience in Microelectronics technology and he is author or coauthor on over than 30 scientific papers in peer reviewed journals and conference proceedings. He is holding Master degree in Microelectronics and PhD in Applied Physics from Belgrade University

Cycle Time Improvement Methodology of Thermal Compression Bond Technology

J. Tsai
Deputy Director
SPIL, Taichung, Taiwan

Abstract

As for mainstream portable application (included smart phone, tablet, handset gamer ..etc handheld consumer electronics, Flip Chip package form factor is providing the ideal solution for high I/O and fine bump pitch solution which included higher electrical and thermal performance product characterization.With developing the fine pitch during chip attach process, there is a methodology called thermal compression bonding (TCB) chip joint technology to realize chip to substrate interconnect purpse. While advanced Si node migrating from 28nm to 16nm or 14nm, The standard bump pitch also shrink from 150 to 100um below. Because of Cu pillar technology need to be utlized bond on trace substrate (BOT)technology.So higher chip attach alignment accuracy chip attach methodology is required to adopt Cu pillar bump pitch shrink market trend.

This paper will research fine bump pitch design on singulated uint and laminated sbustrate.The bump pad area without pre-solder which called bump on trace (BOT) for this technology evaluation.Chip attach technology utilize thermal compression bond and capillary UF dispensing to protect bump in order to keep good singal connection. Following paper called it as TCB+UF technology. By using different flux transfer methodologies were applied into DOE study to approach high throughput UPH and reduce process cycle time. The characterization analysis will utilize simulation methodology & typical reliability testing (Temperature Cycle Test, unbias HAST and High Temperature Storage Test) condition as a quality judgment metrology for TCB+UF process evaluation. Finally, this paper will explore methodolgy while utilizing TCB+UF key process feasibility data for future fine pitch product implementation.

Biography

Jensen Tsai is the Deputy Director of Engineering Center in SPIL (Siliconware, Taiwan), which is 3rd biggest assembly house in the world now.

He has over 18 years of job experience on semiconductor industry, especially focus on wire bond and flip chip advanced assembly technology.

New Flipchip Technology

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Abstract

Abstract: "New Flipchip Technology"
Flipchip Technology is getting more and more important for future packaging solutions. This presentation gives an overview of different Flipchip Technology Solutions provided by industry.
Mainstream Technologies such as C4 and NCP / ACP and ESC processes are explained.
After that special metal joint interconnections will be explained. For each process type of mechanical interconnection is discribed. There are metal joint interconnections and contacting interconnections. For both of them metalic composition is explained, process flows are shown and typical key characteristics for electrical resistance, process time, minimum pitch to be applied are explained.
To increase productivity and reduce process time several method are possible. Several process fullfill this need are under level of industrialisation or already in use for high volume production.
In Focus of this presentation will be specially processes being applicable in Packaging industry:
a. Thermosonic GGI (Gold to Gold Interconnect Process
b. High Speed 2-step Flipchip Process NCP
c. Ultrasonic solder interconnection process.
Those 3 processes being selected due to their very high speed. They are highly reliable and suitable for high miniturization and fine pitch applications. Those can cover a wide range of industrie´s product applications.
Typical characteristics and process parameters for GGI, 2step NCP and US solder connection will be described and analysed. Machine requirements and process flow are shown in very much detail. Reliability data will be shown and explained.
All those processes are suitable to be used in Device Manufacturing, Waferlevel and Embedded Packaging Technology & Assembly.
One main importance when achieving long term reliability of Flipchip process is surface treatment beforehand such as plasma activitation of organic compounds or plasma cleaning to eliminate organic contaminations or inorganic materials on the substrate and chip surface.

Biography

Degree of Diplom-Ingenieur in Process Engineering on Technical University in Munich / Germany in 1988. Since then Project Management & Sales for different kinds of Industy, mainly in chemical Industry. Since 1998 Sales & Project management in Microelectronics & Semiconductor Industry for F&K Delvotec, Wirebonding and Diebonding Technology. Profund experience in handling packaging projects in both Semiconductor and Device-Manufacturing Industry. Since 2006 Sales Director for Microelectronics Equipment at Panasonic Factory Solutions Europe (PFSE). Main target is to establish new PFSE business fields in the Backend and Frontend Industry in Europe: Dieattach, Flipchip, Plasma Cleaning and Plasma Etch Technolgies.

Pressureless Silver Sintering at Temperatures below 250 °C for large-area copper-to-copper bonds

T. Röhrich
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TU Berlin, Nano-Join, Berlin, Germany

Abstract
Silver nanoparticles allow sintering at temperatures below 250 °C forming highly conductive silver layers. Once sintered, they show the melting temperature of the bulk material. Therefore they are promising candiates as interconnecting materials in high-performance next-generation power devices and microelectronic packages. They are expected to withstand high-temperature environments and to have high joint reliability and durability. Several approaches have been discussed using silver nanoparticles. The way nanoparticles are applied and the varying size of the particles is crucial to the formation of the sintered structure and the adherence to the substrate material.
In this study a pressure-less sintering technique has been developed for low-temperature copper-to-copper bonding utilizing silver bulk material which is capable to generate small silver nanoparticles upon heating. Silver pastes were made from a bulk metal-organic complex and additional agglomerated silver nanoparticles. The organic silver complex is easy to produce, stable in air and suitable for large-scale production. In an intermediate heating step the silver components with organic contents of only around 10 wt % were heated to 190 °C in an oxygen-free atmosphere and submitted to a predefined dwell time during which excess organics are released. After cooling the samples to room temperature, the remaining silver material was found to be pasty. Sintering was performed in ambient atmosphere in a furnace at temperatures of 220 °C to 240 °C. Bare copper of up to 20 mm x 20 mm in size was used as substrate material. Cross-sections of the sintered samples were made and investigated by optical microscopy. The ratio of pores in sintered silver layers were compared by means of graphical analysis of cross-sectional images. Determination of shear strength gave values up to 35 MPa exceeding those of conventional Sn-based solders. Further investigations, particularly reliability studies, are in progress.

Biography
2009: Graduation as Dipl.-Ing. in Material Science/ TU Berlin
2009 - 2015: Research Assistant at Chair of Joining and Coating Technology/ TU Berlin
2012 - 2015: Head of Group Microjoining & Laserprocessing at Chair of Joining and Coating Technology/ TU Berlin
since May 2015: EXIST scholarship holder at TU Berlin/ Start-up project: Nano-Join

Best Cost Solution and Performance Improvements of Flip Chip Underfill by De-Void System

A. Chih Horng Horrng
Founder and President of AblePrint Technology Co.,Ltd (APT)
AblePrint Technology Co.,Ltd (APT), Zhunan, Taiwan

Abstract

Authors: CHIH HORNG HORNG, CHUN AN LIN, CHAN LU SU, AblePrint Technology Company, Taiwan

Abstract:
With ever increasing needs for more I/Os and the miniaturization of electronics due to the increased use of handheld applications, flip chip packaging is encountering severe challenges as the pitch and gap are constantly shrinking. These challenges must be addressed in order to meet not only the higher reliability requirements but also cost demands, the so called Total Cost of Ownership (TCO). TCO not only includes aforementioned but also enhance process yield through decreasing process complexity and difficulties for mass production. APT foresees this trend and dedicated itself in offering a solution to address these technical difficulties.

This paper describes de-void system, State-of-art Void Terminator System (VTS), achieves flexibility in managing its process of Capillary Underfilling(CUF), so that high performance and reliability standards for emerging products toward mass production. By using the unique features of the APT de-void system to cure the CUF even extremely large voids can be eliminated with excellent void free performance and very favourable productivity achieved with boosting up dispensing (UPH). Meanwhile, this paper also disclose how APT simplifies CUF flip chip assembly process by passing flux residue cleaning, carrier pre-baking and even plasma cleaning.

Biography

AUGER CHIH HORNG HORNG, is the Founder and President of AblePrint Technology Co.,Ltd (APT). Over 20-year semiconductor experience, he is an expert to work closely with its customers through a clear understanding of their needs and objectives, figure out the essential requirements, assess their needs and deliver the right solutions using a big picture approach.
Prior to establish APT, he was the manager of POWERTECH TECHNOLOGY INC. in Taiwan responsible for process improvement and R&D research on advanced packaging. He holds a Master's Degree in Electrophysics, National Chiao Tung University.

New method for reticle lay out, enabling singulation quality improvement and minimum saw lane

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Manager Assembly Industrialization
NXP, Package Innovation, Nijmegen, Netherlands

Abstract
For production of integrated circuits, optical and process control modules, (OCM and PCM) are usually applied to control the placement of reticle fields (RF) on the wafer and check the wafer fabrication process. Once the wafer is finished, the OCM/PCM is no longer needed and actually are making the process of final die singulation more complicated. Increasing quality requirements on sidewall cracks and chipping, require new methods to do die singulation. These methods, plasma etching for instance, require OCM/PCM to be placed in such a way that at least a lane of 10 micron free of PCM/OCM is available. For conventional wafer technology nodes, commonly used by OEM suppliers, alternative methods have been developed to enable this. For low K nodes, typically the PCM and OCM are placed in the saw lane, consuming unnecessary large area of silicon and making the die singulation difficult, due to saw lane has to first be freed up from metal content using additional processes, such as laser grooving, which may have their own merits next to costs. A new method for the PCM/OCM placement will be proposed, suitable for low K technology nodes as well as conventional nodes. This method allows the use of the existing PCM/OCM, without impacting the low K wafer manufacturing other than the need for a new reticle, while at the same time enable saw lane width reduction and non-mechanical die singulation processes.

Biography
Tonny Kamphuis

Mechanical Engineering, Twente University
Philips/NXP since March 1986

Assembly Industrialization Manager
Package Innovation & Subcon Operations
NXP Netherlands

J.-C. Eloy
CEO
Yole Développment, Grenoble, France

Biography

JC Eloy has created YOLE Développement in 1998 and is managing Yole Développement in term of international development and strategic orientations of the company. He is directly in charge of the Mems and 3D IC activities at Yole Développement JC Eloy and the 20 analysts of YOLE Développement are working directly with the key players of the industry from equipment and materials suppliers to device manufacturers and system integrators. Jean-Christophe Eloy has been 6 years manager of the marketing department of CEA/LETI (France), applied R&D organization involved in the semiconductor, Mems and instrumentation fields (1300 researchers). He then created the semiconductor practice at Ernst & Young in Europe and worked as senior manager in charge of the development of European activities. Jean-Christophe Eloy is involved since 1991 in the Mems and semiconductor areas. EDUCATION JC Eloy is Engineer from INPG/ENSERG (semiconductor and telecommunications) and has a MBA from EM Lyon.

Beyne Eric

E. Beyne
imec fellow & 3D System Integration Program Director
Imec, Leuven, Belgium

Biography

Eric Beyne obtained a degree in electrical engineering in 1983 and the Ph.D. in Applied Sciences in 1990, both from the Katholieke Universiteit Leuven, Belgium. Since 1986 he has been with IMEC in Leuven, Belgium where he has worked on advanced packaging and interconnect technologies. Currently, he is imec fellow and program director of imec's 3D System Integration program.

Since the early 90's he has been involved in multi chip modules and integrated passive device technologies for miniaturizing electronic systems and realising SiP solutions. Around 2000 these developments were focussed on ambient intelligence, a predecessor for what is currently known as IoT devices. In the meantime 3D integration technologies (TSVs, Die and wafer stacking) have been developed, enabling even denser 3D and SiP integration for IoT devices.

Kroehnert Steffen

S. Kroehnert
Director of Technology
NANIUM S.A. - Niederlassung Dresden, Technology, Dresden, Germany

Biography

Dipl.-Ing. Steffen Kröhnert received his master degree in Electrical Engineering and Microsystem Technology at Technical University of Chemnitz, Germany, in 1997. In the same year he started his professional career as Development Engineer in the Corporate Package Assembly, Interconnect and Test Development Center for Semiconductors of Siemens AG in Regensburg, Germany. After carve out of the Semiconductors Business Unit to Infineon Technologies AG in 1999, he worked as Project Manager and moved to Infineon Dresden GmbH & Co. OHG in 2002 to support local setup of Package Development Department for Memory Products. He became R&D Area Manager Component Development and took over Technology Platform ownership for FBGA products. From 2006 he was working as Senior Manager in Qimonda Dresden GmbH & Co. OHG, the carve out of the Memory Products Business Unit of Infineon Technologies. Begin of 2007 he was assigned to Qimonda Portugal S.A., the largest Packaging, Assembly and Test facility of Qimonda, in order to setup and lead the Package Development team at this volume production site. Since 2009 he is Director of Technology at NANIUM S.A. in Vila do Conde, Portugal, the largest independent Semiconductor Packaging, Assembly and Test Foundry (OSAT) in Europe. Steffen is author and co-author of 23 patent filings in the area of Semiconductor Packaging Technology. He is member of IEEE CPMT, IMAPS, MEPTEC, SMTA, VDI, VDE and GPM. He actively contributes as Co-Chair to SEMI Europe's Advanced Packaging Conference (APC), as Technical Committee member to IEEE Electronic Components and Technology Conference (ECTC), IEEE Electronics System-Integration Technology Conference (ESTC) and IMAPS European Microelectronics Packaging Conference (EMPC), and as Assistant Technical Co-Chair (Europe) to IMAPS Device Packaging Conference and International Symposium on Microelectronics.

Lan Albert

A. Lan
Senior Director
Siliconware Precision Industries Co., Ltd. (SPIL), Taichung, Taiwan

Biography

Albert Lan is the senior Director of Engineering Center in SPIL (Siliconware, Taiwan), which is 3rd biggest assembly house in the world now.
He has over 20 years of job experience on semiconductor industry, especially focus on bumping and flip chip advanced assembly technology.
Currently, he also take on vice chairman of Semiconductor Equipment and Materials International Taiwan Association and the chairman of TILA (Taiwan Intelligent Leader Association).