Low Power Conference

L. Le Pailleur
Conference Chair and Technology Line Management Director
STMicroelectronics, Crolles, France

Biography

In 1989, Laurent Le Pailleur received the degree in electrical engineering from ENSICAEN (National Engineering School) , the M.S. degree in instrumentation and automation from Caen University and the Business degree from IAE (Enterprise Administration Institute). He has been working on mixed-signal video systems and imaging digital processors with Philips Semiconductors as designer then design team manager. In 1997, he joined STMicroelectronics, Grenoble, to develop dedicated solutions for wireless and multimedia applications. He also enjoyed various positions as audio and power management product line manager, 2.5G mobile platform product manager then 3G mobile digital System-on-Chip product management director. This allowed him to develop deep understanding on RF, analog and digital technologies, architecture, cost structure and system partitioning. He built new methodologies as head of technology management (semiconductor, packaging and IPs) with ST-Ericsson. He is now director for advanced Cmos technology line with STMicroelectronics, Crolles, as well as ST Management Committee Member within the 10nm international development team, covering bulk, FD-SOi and FinFet technologies.
He participated to numerous international conferences and hold multiple patents.

Highly Energy Efficient Nanotechnologies and Applications

J.-M. Chery
Chief Operating Officer
STMicroelectronics, GENEVA, Switzerland

Abstract

After decades of steady gradual evolution, the semiconductor industry is now facing its biggest and most interesting challenge. The number of connected electronics devices is growing exponentially, starting with mobile devices and it is now accelerating with the internet of things. To sustain this exponential growth, the semiconductor industry requires a real breakthrough in energy efficiency both for the connected devices and for the communication infrastructure. At the same time, the traditional planar bulk CMOS technology is plateauing in power consumption and performance after 28nm. Therefore innovative solution for very energy efficient systems are mandatory to continue the growth the semiconductor industry enjoyed, covering ultra low power systems, energy management and harvesting. We will explore some of these solutions which have to be as well cost effective and simple to put in very large volume production.

CV of presenting author
Jean-Marc Chery is Chief Operating Officer, General Manager, Embedded Processing Solutions (EPS) at STMicroelectronics . He also holds overall responsibility for the EPS Technology R&D and Front-End Manufacturing, as well as the Packaging & Test Manufacturing for the whole Company. Chery is Vice Chairman of ST's Corporate Strategic Committee

M. Horstmann
Director Products & Integration
GLOBALFOUNDRIES, Dresden, Germany

CV of presenting author
Manfred Horstmann serves as Director at GLOBALFOUNDRIES in Dresden and is since 2009 responsible for 28nm technology development and subsequent production ramp. Manfred currently leads since b/o 2014 the Product & Integration organization with focus on 28nm volume production and yield improvement for multiple customers.

Prior to this role he served 18 years in various leadership positions in research and development (R&D) at AMD and GLOBALFOUNDRIES. Before 2009 Manfred Horstmann focused as engineering senior manager at AMD in Dresden on definition, development and technology transfer of high-speed CMOS transistors from 0.35um down to the 28nm technology node. Center of this work was the development of high speed CMOS transistors and innovative integration concepts using a collaborative approach with technology development partners.

Manfred Horstmann received his diploma degree in physics (MSc) from Technical University Aachen in 1994. From 1994 to 1996 he continued his work as member of technical stuff of Research Center Juelich. 1996 he received the PhD degree from Technical University Aachen on sub-100nm high speed compound semiconductors, awarded with the Borcher's medal of Technical University Aachen.
He holds over 130 patents and authored or co-authored over 150 technical contributions. He was elected from the board of directors from Research Center Juelich as member of the scientific advisory board for their solid states institutes as well as serves since 2010 as advisor for the Helmholtz association in Germany.

From 32/28nm partial depleted volume production to energy efficient fully depleted solutions in 28nm and beyond

M. Horstmann
Director Products & Integration
GLOBALFOUNDRIES, Dresden, Germany

Abstract
Within the semiconductor industry, pure leading edge foundries serve a special mission by delivering state-of-the-art competitive logic performance with a strong focus on system-on-chip (SoC). Therefore they have to support a broad portfolio of different technology options on each node and GLOBALFOUNDRIES is an industry leader by representing this particular business model.
GLOBALFOUNDRIES has a long time experience in leading-edge semiconductor manufacturing and technology capabilities one particular on silicon on insulator (SOI) based high performance microprocessors. To achieve the "high performance per watt" figure of merit technology elements like partial depleted (PD) -SOI, strained-Si, ultra low K BEOL and HKMG is needed together with an efficient multiple core- and power-efficient design. Those technology elements were developed and optimized for multiple generations beginning from an 180nm down to the 28nm technology node which runs currently in high volume production.
In particular the 28nm node should remain for a long time at the sweet spot in Foundry Industry for yield,

performance and cost. This node will be the basis to add technology features like (Flash, HV, MEMS etc.) but also will enable new innovations like fully depleted devices, reducing power consumption even further. Therefore, extreme thin (ET) planer SOI devices with back bias options (BB) and their potential application in 28/20nm will be presented. Being a planar device, ET-SOI devices allow the continuation of previous nodes manufacturing and design experience. Vt-tunability and low GIDL currents are a clear advantage of ET-SOI BB devices for SoC applications, too.
The presentation will conclude with an outlook on nodes beyond 20nm with 3d FINFET concepts.

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Ultimate scaling of CMOS technologies

T. Skotnicki
ST Company Fellow
STMicroelectronics, Crolles, France

Abstract
Electronics is more and more pervasive in everyday life: smartphones, connected cars, Internet of Things. All this is not only about mobile energy efficient technologies, but also about energy harvesting and storage, about power management, and also about sensors and MEMS devices. UTBB (ultra-thin body and BOX) FD-SOI (Fully Depleted Silicon On Insulator) is a planar semiconductor technology that is particularly well suited for low power applications such as Internet of Things. We will demonstrate this on the example of the 28nm UTBB SOI technology that ST is offering for LP mobile applications. We will also describe briefly the energy harvesting technologies that help to reduce power required from the supply. Convergent use of the intrinsically low power consumption offered by the UTBB SOI and of the energy harvesting, further reducing the demand on the supplied power, will be shown as the key enabler for low power applications such as Internet of Things. The paper describes the development of the FD-SOI technology, the choice of devices centering and their main characteristics, We will explain how the intrinsic device characteristics enabled by their UTBB SOI structure contribute to promoting the technology for high speed energy efficient operation, even in low voltage conditions.

CV of presenting author
Thomas SKOTNICKI is the STMicroelectronics Fellow and Director of Advanced Devices at STMicroelectronics Crolles, France, that he joint in 1999. He received his Master and EE degrees from the

Warsaw University of Technology in 1979, the PhD diploma from the Institute of Electron Technology, Warsaw Poland in 1985, and in 1993 he received the HDR (Habilitated for Directing Research) diploma from the Institut National Polytechnique de Grenoble, France. In 2007, he received the title of Professor from the President of Poland. The focus of his program at STMicroelectronics is on Low Power / Low Variability for 20nm and beyond CMOS, on innovative device structures, new memory concepts and cells, and on integration of new materials for CMOS. Recently he has extended the scope to include Energy Harvesting for autonomous Low Power systems and devices. He holds about 80 patents on new devices, circuits and technologies. He has presented over 50 Invited Papers and Short Course Lectures, co-edited one book, (co-) authored about 350 scientific papers (review based), and several book chapters in the field of CMOS devices and circuits. From 2001 to 2007, he served as Editor for IEEE Transactions On Electron Devices. He has been teaching at EPFL (Lausanne) and INPG (Grenoble), and has supervised and led to successful defence 25 PhD theses. He has been serving in numerous Conference Program and Executive Committees (IEDM, VLSI, ESSDERC, ECS, SNW, IWJT), Academia Advisory Boards, Governmental Expert Commissions, R&D Program Steering Committees, ITRS, and Award Committees. He is an IEEE Fellow and SEE Senior Member.

FinFeT: challenges and opportunities

K. Barla
Unit Process & Modules Department Director
IMEC, Antwerpen, Belgium

Abstract
The multi-gate architecture has been demonstrated as a key enabler for further CMOS scaling thanks to its improved electrostatic and short-channel effect control. FinFets represent one the architecture of interest. It has been introduced by Intel in manufacturing at 22 nm technology and recently they provided first details of the FinFet evolution allowing 14nm technology to reach expected performance and cost. In this presentation we will present the benefits and challenges of FinFet structures for further technology scaling towards 7nm and below.

CV of presenting author
Kathy Barla is Unit Process & Modules Department Director at IMEC since October 2012. Kathy has 30 years of experience in microelectronics working for ST Microelectronics at Crolles for many years and at the International Semiconductor Development Alliance, IBM East Fishkill, to develop & transfer the 28nm technology. After a PhD in materials sciences, she started as Research Engineer at CNET, France Telecom Research Center dedicated to microelectronics. Then she moved to STMicroelectronics as Process Engineer to take in charge the development of gate dielectrics. In STMicroelectronics she was involved in many of the FEOL & BEOL process technology challenges starting with 0.5 m up to 20nm technology. She acquired an extensive experience in managing 200 & 300 mm R&D Unit Process. In her new position at IMEC, Kathy took up the responsibility in strengthening the links between unit process and modules with device & integration development. She is supporting concurrent innovation at the level of materials, unit steps and modules to shift the frontiers of technology development.

M. Hasan
Solutions Engineer
Imagination Technologies, Kings Langley, United Kingdom

CV of presenting author
Munir has recently joined Imagination Technologies as a Solutions Engineer for Europe. He is primarily focused on supporting customers with integrating MIPS processors into their SoC for the next generation of

applications. Prior to joining Imagination Technologies, he had been working as Design Evaluation Engineer for Analog Devices Inc in the Digital Video Products group. He has an MEng in Electrical an Electronic Engineering from Imperial College London.

System landscape for More Moore - from technology to architecture

M. Badaroglu
Sr Program Manager
Qualcomm Technologies, Leuven, Belgium

Abstract
So far CMOS scaling enabled simultaneous system throughput scaling by concurrent delay, power, and area shrinks with thanks to Moore's law. System scaling is getting more difficult with the limitations in interconnect and bandwidth/power as well as the difficulties and cost of monolithic integration. This requires a mobile-centric approach that ensures the optimal balance of performance and power. In this talk we present the system scaling enabled by More Moore technologies and potentially leading to holistic pathfinding between architecture and technology.

CV of presenting author
Mustafa Badaroglu is senior program manager at Qualcomm, Leuven, Belgium. In this role, he has the responsibility to assess/track feasibiliy and supply chain readiness of new technologies through consortia projects and supplier collaborations in the areas of logic and memory, interconnect, lithography, optical IO, and 3D integration.

Prior to joining Qualcomm, he was principle scientist at imec, Leuven, Belgium, working on targeting on More Moore technology requirements for design. Before imec he was design manager with ON Semiconductor in the automotive and power product development division, leading chip product development activities to hand over to high volume production.

Dr. Badaroglu received the B.Sc. degree from Bilkent University, the M.Sc. degree from the Middle East Technical University, the Ph.D. degree from the Katholieke Universiteit Leuven (KU Leuven), all in electrical engineering, and the M.Sc. degree in Industrial Management from KU Leuven. He is the chair of the Process Integration, Devices, and Structures (PIDS) chapter of the International Technology Roadmap of Semiconductors (ITRS).

MIPS: Multi-Threaded RISC Architecture to Enable Higher Performance in Low Power Applications

M. Hasan
Solutions Engineer
Imagination Technologies, Kings Langley, United Kingdom

Abstract
RISC Processors have been able to achieve low power due to the simplicity of its Pipeline Stages and Decode Logic, thus making it suitable for a wide range of applications; from Embedded Controllers to Network Servers.
A factor that limits a Processor's Performance is the latency when accessing data from memory. With Processors cycle times reducing faster than the memory access time, there is a critical performance

bottleneck. Deeper levels of Cache are able to mitigate this bottleneck, but this comes at the cost of increasing Area. Multi-threading offers a solution; it ensures another sequence of instructions progress through the pipeline, while the current memory access is being completed. Thus, Multi-threading increases throughput performance while maintaining low power.
This presentation will discuss why MIPS Architecture is ideal for Multithreading, how it has been implemented, the Performance and Power benefits and example Applications using this technology.

CV of presenting author
Munir has recently joined Imagination Technologies as a Solutions Engineer for Europe. He is primarily focused on supporting customers with integrating MIPS processors into their SoC for the next generation of applications. Prior to joining Imagination Technologies, he had been working as Design Evaluation Engineer for Analog Devices Inc in the Digital Video Products group. He has an MEng in Electrical an Electronic Engineering from Imperial College London.

Low-power multiprocessing: from embedded to servers multi-core

F. Clermidy
Senior expert
CEA-LETI, Grenoble, France

Abstract
Energy efficiency is nowadays required for all the multi-core applications, from embedded to servers. Being a natural focus in embedded systems, lessons learnt from this application field can be applied to servers or even High Performance Computing. However, constraints and objectives are different: larger power consumption, higher memory bandwidth and performance objective for servers compared to fixed reduced power budget objective for embedded systems. This comes with large-scale chips for servers while relatively small-size chips are used for embedded systems.
In this talk, we will discuss solutions for power efficient multi-core embedded systems and their application to server chips. Advanced technologies such as FDSOI and 3D stacking will also been considered as ingredients useful for closing the gap between these two application fields.

CV of presenting author
Fabien Clermidy obtained his master degree in 1994, his Ph.D in Engineering Science from INPG, Grenoble in 1999 and his supervisor degree from INPG in 2011.
He is currently head of the digital design laboratory at CEA-LETI. The lab main activities are targeting multi-core architectures and low-power design with some chips developed in the last few years: MAGALI, a 23-core targeting 3GPP-LTE applications; P2012 (coll. with ST), a 64-core multiprocessor for augmented reality applications; WIOMING (coll. with ST/STE), a DRAM on multi-core platform.
Fabien Clermidy has published more than 70 journal and conferences papers and is author or co-author of 15 patents. He is currently associate editor for TCAS-I journal.

F. Clermidy
Senior expert
CEA-LETI, Grenoble, France

CV of presenting author
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Fabien Clermidy has published more than 70 journal and conferences papers and is author or co-author of 15 patents. He is currently associate editor for TCAS-I journal.

Architectures for Energy Efficiency and power management

D. Jacquet
System architect
STMicroelectronics, grenoble, France

Abstract
With the increasing demand of processing power to be delivered by the System On Chips, it is key to improve their
energy efficiency, not only for thermal or battery life duration purposes but also for environmental considerations
such as green supercomputers, wireless base stations and micro servers.
After a first section dedicated to the different techniques for energy efficiency { DVFS, Body Biasing, Power domains,
AVS & process sensors }, we will see how the FD-SOI technology can further enhance the efficiency of those techniques and
create new opportunities like Wide DVFS and dynamic leakage management. The architecture of the key IPs to implement those
techniques is detailed. The benefit of FD-SOI in multi-processing computing systems will also be illustrated showing
the added value compared to bulk technology. Silicon results will demonstrate the potential of body-bias for obtaining
very high speeds in very-low voltage conditions.

CV of presenting author
David Jacquet is a Senior Principal Engineer at STMicroelectronics. He joined STMicroelectronics in 1995 as a Design and Architecture team lead for the development of a 64-bit VLIW DSP. In 2003 he moved into a new role leading the SOC low power architecture for digital baseband and application processor products for mobile platforms at ST-Ericsson. He currently leads the architecture activities for energy efficient high performance CPU/GPU implementation at STMicroelectronics.
David holds a degree in microelectronics engineering from ENSERG-ENSIMAG in Grenoble, France.

Enabling the IoT through ultra-low voltage operation: down to the threshold and below

M. Alioto
Prof.
NUS, ECE, Singapore, Singapore

Abstract
The demand for smaller integrated systems with significant computation-ability is driving a massive shift towards extremely compact energy-autonomous systems (e.g., wearable electronics, Internet-of-Things). Their size scaling is well-known to be limited by their energy efficiency, hence aggressive voltage downscaling is a forced choice in such applications, with voltages being pushed down to near-threshold (and sometimes even below).
This talk addresses the fundamental issues entailed by the operation at near-threshold and below and

related solutions. Due to the significantly different performance/energy/resiliency/leakage design tradeoff at ultra-low voltages, this talk provides a fresh view on near-threshold circuits (and below) and debunks several wrong assumptions stemming from traditional low-power common wisdom. In particular, design techniques that do (or do not) work at ultra-low voltages are discussed for logic and memory arrays. Also, near-threshold automated design flows and design hints for critical sub-systems (e.g., clock distribution) are discussed.
To put things in perspective, design trends at near-threshold and below are discussed, including fine-grain voltage distribution/power gating, heterogeneity, specialization, among the others. Finally, the availability of designers with across-level expertise (e.g., circuit/architecture, architecture/software) is envisioned to be a fundamental necessity to truly enable the energy benefits promised by ultra-low voltage operation.

CV of presenting author
Massimo Alioto is Associate Professor at the Department of Electrical and Computer Engineering, National University of Singapore. Previously, he was Associate Professor at the University of Siena, Visiting Scientist at Intel Labs - CRL (2013), Visiting Professor at the University of Michigan - Ann Arbor (2011-2012), University of California - Berkeley (2009-2011) and EPFL - Lausanne.
He is (co)author of 200 publications on journals (70, mostly IEEE Transactions) and conference proceedings, and two books. His primary research interests include ultra-low power VLSI circuits, self-powered and wireless nodes, near-threshold circuits for green computing, error-aware and widely energy-scalable VLSI circuits, circuit techniques for emerging technologies.
Prof. Alioto was the Chair of the "VLSI Systems and Applications" Technical Committee of the IEEE Circuits and Systems Society (2010-2012), and Distinguished Lecturer (2009-2010). He is currently Associate Editor in Chief of the IEEE Transactions on VLSI Systems, and served as Guest Editor of several journal special issues. He also serves or has served as Associate Editor of a number of journals (including ACM Transactions on Design Automation of Electronic Systems, IEEE Transactions on CAS - part I). He serves or has served as panelist for several funding agencies and research programs in the US and Europe. He was Technical Program Chair of the ICECS 2013, NEWCAS 2012 and ICM 2010 conferences, and Track Chair in a number of conferences (ICCD, ISCAS, ICECS, VLSI-SoC, APCCAS, ICM).

Ultralow-Voltage Design and Technology of Silicon-on-Thin-Buried-Oxide (SOTB) CMOS for Highly Energy Efficient Electronics in IoT Era

S. Kamohara
Chief Engineer
Low-Power Electronics Association & Project (LEAP), Renesas Electronics Corporation, Tokyo, Japan

Abstract
Ultralow-voltage (ULV) operation of CMOS circuits is effective for significantly reducing the power consumption of the circuits. Although operation at the minimum energy point (MEP) is effective, its slow operating speed has been an obstacle. The silicon-on-thin-buried-oxide (SOTB) CMOS is a strong candidate for ultralow-power (ULP) electronics because of its small variability and back-bias control. These advantages of SOTB CMOS enable power and performance optimization with adaptive Vth control at ULV and can achieve ULP operation with acceptably high speed and low leakage. In this paper, we describe our recent results on the ULV operation of the CPU, SRAM, ring oscillator, and, other logic circuits. Our 32-bit RISC CPU chip, named "Perpetuum Mobile," has a record low energy consumption of 13.4 pJ when operating at 0.35 V and 14 MHz. Perpetuum-Mobile micro-controllers are expected to be a core building block in a huge number of electronic devices in the internet-of-things (IoT) era.

CV of presenting author
Shiro Kamohara received the B. S. degree in physics from Keio University in 1986, M. E. degree from University of Tokyo Institute Technology in nuclear engineering in 1988 and Ph.D. from Tokyo metropolitan University in electrical and electronic engineering in 2008. He joined the Central Research Laboratory of Hitachi Ltd. in 1988. Since 1995, he was the member of Semiconductor & Integrated Circuit Div. of Hitachi Ltd. He is a member of Renesas Technology Corp since 2003 and Renesas Electronics Corp since 2010. He concurrently served as Semiconductor Leading Edge Technologies, Inc (Selete) since 2006. Now he has

doubled as Low-power Electronics Association & Project(LEAP). He was the visiting industrial fellow of the University of California at Berkeley in 1996.

Material Solutions to address the Wireless Low Power Demands

C. Mazure
Chief Technology Officer, Executive Vice President
Soitec, Bernin, France

Abstract
Engineered substrates are well established for the manufacturing of numerous devices which are essential for mobile chipsets and wireless applications. Silicon-on-sapphire (SOS) is being used for the fabrication of high performance RF devices. SOI-on-high resistive substrates (SOI-HR) is the preferred solution for the manufacturing of RF Front End Module (FEM) devices and has become the de facto standard for switches and antenna tuners. Movement sensors are made using SOI substrates. Fabrication of backside illuminated imagers (BIS) includes thin film transfer onto a new substrate of the originally processed layer.
The recent big innovation is the introduction of fully depleted (FD) CMOS technologies to make possible low power, low VDD IC operation without significant performance loss. FD devices can be vertical, (FinFETs, 3D MOSFET), or planar (FD-SOI). Their key characteristic is that the silicon channel is undoped.
FD-SOI is an evolutionary innovation because it has the advantage of being a planar transistor structure that extends the applicability of bulk design flows with existing design and EDA tools. It is a non-disruptive MOSFET architecture change for SOC design and processing. FD-SOI requires ultra-thin Si (<20nm) over an ultra-thin buried oxide (BOX<25nm) for improved electrostatics. FDSOI is particularly optimized for mobile CMOS technologies.
In this review, the contributions and benefits of the different substrates solutions will be discussed focusing on the devices used in the mobile space.

CV of presenting author
Dr. Mazure joined Soitec in 2001. He is the Head of Corporate R&D, responsible for the management of Academia and Industry R&D collaborations. He helps define company strategy; analyze technology trends; anticipate new applications and products; identify incubator and spin-off opportunities.

Prior to joining Soitec, Dr. Mazure worked for Infineon Technologies in Munich, Germany, where he headed the ferroelectric FeRAM development program. Later, as Director of Business Development at Infineon he initiated the Infineon-Toshiba FeRAM Development Alliance. Before moving to Germany, he worked for the IBM/Infineon DRAM Development Alliance in East Fishkill, New York; and for Motorola in Austin, Texas. During his years at Motorola Semiconductor, in APRDL, he worked on SOI, BiCMOS high performance SRAM. He has extensive expertise in materials, unit processess, CMOS integration, MOSFET and Memories.

Dr. Mazure holds two doctorates in sciences, one from the University of Grenoble, France, and the other from the Technical University of Munich, Germany. He has authored or co-authored more than 120 technical papers and holds more than 100 US patents and significantly more worldwide.

He is a member of several international technology and advisory committees, IEEE Fellow member and a regular invited speaker at international conferences and workshops.

FD SOI and Internet of Things

H. Jones
CEO

IBS, Inc., Los Gatos, United States

Abstract
The high cost of migrating to 16/14nm and 10nm FinFETs is resulting in other options being evaluated by companies that want low power and low cost for high volume applications, including the emerging Internet of Things.

The benefits of FD SOI, for supporting Internet of Things, will be applicable to medical, consumer, multimedia, industrial, and other applications.

Scalability of FD SOI will allow the technology to be used for Internet of Things and other applications for the next 10 to 20 years.

CV of presenting author
Handel Jones is the founder, owner, and CEO of International Business Strategies, Inc. (Los Gatos, CA), which has been in business for more than 25 years. Prior to IBS, Handel Jones was Vice President at Rockwell International, where he managed 1,500+ engineers in avionics, communications, and semiconductors. Handel Jones was also in charge of international sales and marketing as well as business strategies for some of the business units.

As CEO of IBS, Handel Jones provides strategic support for major global corporations in multiple industry segments. The clientele base includes Intel, IBM, Qualcomm, Broadcom, Microsoft, Nokia, Samsung, Sony, Toshiba, Apple, Cisco, Siemens, Motorola, Fujitsu, NEC, Hitachi, Renesas, TSMC, STMicroelectronics, TI, and others. IBS has customers in the U.S., China, Europe, South Korea, Japan, India, and other countries. IBS has also provided support to the French Government on Nano 2017 (their advanced technology initiatives).

IBS also interfaces and supports financial institutions such as Goldman Sachs, Carlyle, Blackstone, CitiGroup, Credit Suisse, Exane BNP Paribas, Warburg Pincus, Walden, KKR, Morgan Stanley, Bain Capital, Bank of America, TPG, and others.

A major part of the activities of IBS is involved with strategies for successful global business participation. This requires deep understanding of markets, competition, technologies, and the strengths and weaknesses of the management teams. The IBS analysis approaches can be applied to corporations, industries, as well as countries.

There is also the need to understand future trends as well as the potential impact of destructive factors.

IBS has strong expertise in China and published its first book called *Chinamerica*, which provides a detailed comparison between the industrial base and political policies of the U.S. and China (McGraw-Hill, 2010) as well as a second book called *China Global Revolution: How China Can Become No. 1* (2014). Articles have been contributed to the China Daily, Global Times, and Forbes.

The growth and opportunities in China is of special interest to IBS, and specifically to Handel Jones.

C. Mazure
Chief Technology Officer, Executive Vice President
Soitec, Bernin, France

CV of presenting author
Dr. Mazure joined Soitec in 2001. He is the Head of Corporate R&D, responsible for the management of Academia and Industry R&D collaborations. He helps define company strategy; analyze technology trends; anticipate new applications and products; identify incubator and spin-off opportunities.

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Dr. Mazure holds two doctorates in sciences, one from the University of Grenoble, France, and the other from the Technical University of Munich, Germany. He has authored or co-authored more than 120 technical papers and holds more than 100 US patents and significantly more worldwide.

He is a member of several international technology and advisory committees, IEEE Fellow member and a regular invited speaker at international conferences and workshops.

Using Configurable Processor Technology to achieve power efficient architectures

M. Binning
Senior AE Manager
Cadence Design Systems Inc, Bracknell, United Kingdom

Abstract
This discussion will centre around how "configurable and extensible" processor technology can be leveraged to create highly power efficient processor cores for such diverse domains as "always-on" functionality (including voice triggering and sensor fusion applications) and highly efficient complex Image and video processing.
We will explore some of the fundamentals of the Cadence® Tensilica® Xtensa® technology, and use some examples from the above domains to illustrate how the Xtensa architecture can be used to create these apparently diverse, but highly efficient, solutions and their associated software tools.
Finally we will explore how these architectures can be seamlessly integrated into state-of-the-art implementation flows in a very short time, targeting high efficiency implementations whether the emphasis is on lowest power or highest performance.

CV of presenting author
Bio - Marcus Binning

Having spent his early career in digital and embedded software design, Marcus Binning spent eight years deploying and supporting complex EDA tools (Zycad HW accelerators and emulation tools, and formal verification tools from Chrysalis Symbolic Design) into a variety of European customers.

Since 2000 he has headed up the application engineering effort in Europe for the Tensilica® Xtensa®

configurable processor technology (now owned by Cadence Design Systems, Inc.). As an acknowledged expert in the ASIP (Application Specific Instruction set Processor) field, he has been involved with (and directly contributed to) a number of successful, complex customer designs in companies both small and multi-national.

He holds a Bsc. (Hons) in Electrical and Electronic Engineering from the University of Bristol, and currently works in the UK office of Cadence Design Systems.

Optimize Power Consumption and Delivery from RTL to GDS

J. Toublanc
Business Development Manager
ANSYS, Sophia Antipolis, France

Abstract
Energy efficiency could have different meaning depending of final applications or technologies. Most of the time, it could be translated into 3 main challenges for the project: minimize the power consumption in "standby" operational mode, boost the performance/power ratio in "functional" mode and certify the power delivery integrity. To optimize overall power efficiency, each of these items needs to be addressed during the design cycle.

Such a methodology involves many power consumption analyses and budgeting, for multiple operational modes and early enough to eliminate wasted power and anticipate physical implementation requirements. Complementary, with advanced process and reduced power supplies, the accuracy of the Chip-Package power delivery network co-analysis is critical.

ANSYS's innovative technologies connect PowerArtist, an RTL power analysis and optimization solution, and RedHawk, a SoC power integrity and sign-off solution, to enable a comprehensive power-efficient methodology - from early in the design process to silicon sign-off.

The presentation provides an overview of early RTL power prediction and analysis-driven power reduction associated with accurate power Integrity and Reliability analysis from virtual prototype to tape-out stages.

CV of presenting author
Jerome is a business development manager in Europe and is driving ANSYS-Apache's Power and Noise solutions for full System Integrity. Prior experiences focused on different SoC implementation tools such as Place & Route or Power Analysis and also include analog/digital full-custom circuit design. He received his Engineer Degree in Microelectronics from ESIEE-Paris (France) in 2000.

Explore, track and validate power and thermal targets from architecture specifications to validation

L. Blanc
Principal Application Engineer
Docea Power, Grenoble, France

Abstract
Power aware design is more pervasive than ever. In the mobility segment, smart phones, tablets and notebook designs are differentiated by battery life, performance/functionality/features all within a challenging mechanical/thermodynamic form factor. Most designs are thermally limited for reliability/ergonomic and even

safety reasons like in automotive. To design modern systems it is imperative to model and simulate the power and thermal behavior across a variety of usage scenarios.

Design flows have been traditionally built to cover development and validation of functional requirements. Specifically at the architecture level where most of the power can be saved the industry is still in a handcrafted era dominated by more and more complex spreadsheets which are error prone to estimate power consumption while exploration capabilities are very limited.

Docea Power provides innovative software solutions to model, simulate and explore various performance, power and thermal trade-offs of SoC and platform architectures. The presentation will highlight how the power and thermal architects now have the capability to forecast power/thermals earlier in the design phase, explore "what ifs" at system level and validate power/thermal management policies for more optimal hardware and software design over the spectrum of use.

CV of presenting author
Lionel has joined Docea Power in 2013, with a strong power management expertise acquired during his 10 years spent Texas Instruments (Nice) as a system architect and platform modeling technology leader within the OMAP business. Prior to joining TI, Lionel has been a co-founder and principal consultant Engineer at Esterel Technologies. Lionel has been granted a PhD in Computer Science from the University of Nice in 1999.

R. Barbarin
Account Chief Technologist
Hewlett Packard, Grenoble, France

CV of presenting author
Rémi Barbarin is HP Chief Technologist at Hewlett Packard where he specializes in providing end-to-end IT solutions for the Aerospace and Defense industry where energy efficiency is crucial both for Datacenters and High Performance Computing solutions.

In this capacity, he is called to provide strategy recommendations, innovation workshops, technology briefings, and best practice sharing sessions as well as engage leading experts from all HP organizations worldwide.

Remi's role also encompasses the supervision of the architects and of solution work done for the Aerospace Industry in EMEA. His responsibilities include as well technology strategy, continuous improvement, marketing and communication.

Holding both a MBA and an engineering degree, Remi has an extensive background both in R&D and IT. In HP since 2000, he held various leadership roles in Enterprise Services, Product Manufacturing and Corporate IT.
Remi is 40 years old, lives near Grenoble in the French Alps with his wife and two daughters. During his time off, he enjoys practicing martial arts.

Power Dissipation in the Design of Consumer Products and Drones

Y. Levy
VP Corp. Business Development
Parrot, Paris, France

Abstract

New Consumer and Robotics Devices require intense image and signal processing. Processors with 64-bits CPU and multi-core GPUs consume several Watts that need to dissipate in consumer products.

New Semiconductor nodes (20, 14nm...) lead to even higher power consumption especially on the leakage side, while the need for more Embedded computation also increases. Fans, large heat sinks can no longer be the solution.

Parrot, as a chip designer and user of these chips into its own products is facing new challenges that need to be taken into account for designing new consumer products.

Drones are 3D mobile robots that will ultimately fly autonomously for a number of missions (mapping, agriculture, surveillance, even delivery) and will need to carry heavy processing power in very light vehicles.

CV of presenting author
Yannick Lévy is the VP of Corporate Business Development of Parrot. Yannick is responsible for investments into subsidiaries of Parrot group as well as start-ups collaborating with Parrot. He manages the business development of these companies. Previously, Yannick headed the Digital Tuner Business Unit of Parrot, renamed from DiBcom that he founded in 2000 as the CEO, and sold to Parrot in 2011. DiBcom has developed the World leading chipsets for Digital TV and Radio reception in Cars and other mobile devices, its chips are used by car makers like BMW, Mercedes, Audi, Nissan, Hyundai. Prior to DiBcom, Yannick graduated from Supélec in 1991 and obtained his Ph. D. in Electrical Engineering in 1994 from the University of Notre Dame, U.S.A. He held several positions in R&D, Sales and Management at Sagem, SES Astra and Atmel prior to founding DiBcom.

Using SoCs to build datacenter servers

G. Renaud
Technology Consultant
HP, Eybens, France

Abstract
Rather than using virtualization and other technics to efficiently use the power of traditional servers, we'll see how Moonshot is offering a different approach for the design of servers that fit perfectly identified workloads. By using technologies coming from the mobile industry such as SoC, specific processors and accelerators, Moonshot proposes servers tailored for specific range of applications that deliver a better performance/energy ratio.
After reviewing the architecture of one of these software-defined servers, we will walk through a real customer use case to analyze the steps needed to get a perfect fit between hardware and software that allows an improvement in energy efficiency.

CV of presenting author
Gallig is working as a technology consultant part of the EMEA Discovery Lab. After spending 13 years at HP in the enterprise server group with various roles and responsibilities, his current job it to engage with customers and partners to identify applications that could leverage the software-defined approach from HP. Gallig is also part of an internal organization which is working closely with the engineering teams and that is reviewing upcoming HP server products.

Business Growth with Energy Efficient Networks

R. Di Muro
Product Marketing Program Manager

Ericsson, Stockholm, Sweden

Abstract
The seminar highlights the importance of energy efficiency for Mobile operators, focus on delivering better-performing network with good control of the total cost of ownership. Use case of real deployment with lower power consumption will be shared.

CV of presenting author
Rodolfo Di Muro has over 19 years of experience in Transmission and Telecommunication with know-how in packet and optical networks, radio network, value propositions, and business cases.

Experienced and competent in operator business cases, working as Product Marketing Program Manager in Business Unit Networks in Ericsson, Stockholm (Sweden) since 2012.

Responsible as product marketing to highlight product benefits and product positioning for all transmission products, working in Coventry (UK) and Genoa (Italy) since 2007.

Product strategist with product road map responsibility since 2001 (in Marconi, Coventry, UK).
Technology strategy with coordinating University Research projects across Europe, also from 2001.

From idea to realization, Rodolfo has followed all the Implementation steps as design, software optimization, and in building prototype in optical amplifier (E-band) in the Nortel, Advanced Research Group in Harlow (UK) in 1997, and working as system network design for Nortel Transmission group (2000).

Key professional achievements: Electronic degree (1992, Bologna University), PhD (Parma University 1995), MBA (Warwick University, 2008), IPR technical consultant, IEEE technical reviewer, filed 18 patents (IPRs), published 54 technical papers, Chairman for IET in Coventry and Warwick branch (2001).

Ultra Low Power wireless sensors in Buildings

G. Chabanis
Pervasive Sensing Manager
Schneider Electric, Technology Strategy, Grenoble, France

Abstract
The talk will content the description of main characteristics of our developed ultra low power wireless sensors platform in the context of SE applications with a particular focus in Buildings.
The architecture and power consumption of the wireless sensors per function will be presented with impact on autonomy depending on storage solution and type of sensors within the range of ambient buildings sensors. The optimized ZigBee Green Power (ZGP) sensors platform allows to measure a range of sensors like temperature, humidity, light, door/window contact, motion/presence sensor (PIR), CO2 with an average power consumption varying from 1 µA to 20µA depending on sensor types and measurement frequency. The optimized ZGP implemented protocol requires only 110 µJ to send a frame providing the flexibility to adjust the transmission frequency from few sec to few minutes depending on application requirements and still operated without wire for power supply. A unique disruptive ultra low power CO2 sensor co-developed in Partnership with Gas Sensing Solution will be described showing typical sensor technology challenges to overcome in order to be compatible with wireless solution.
The remaining and overcame challenges of the platform will be also discussed targeting the diversity of sensors power consumption constraint, the weaknesses of today storage technologies and trends we

foresee.

CV of presenting author
Gilles received his PhD in Physical Chemistry in 1997 from the University of Montpellier before working as a Post Doctoral Research Fellow at the Chemistry Department of University College London on a European Research project aiming at developing semiconducting oxide gas sensors. He gained many years of experience on sensors development as innovation project leader for the development of Aircraft Fire Detection systems at Siemens. Thereafter, he worked as product manager for Aerospace fire detection for Siemens before joining Schneider Electric Innovation Department in 2007 as project leader of the homes sensors project dedicated to the development of self-powered wireless multisensors for Buildings in the frame of the Homes Programme.
Gilles is currently Pervasive Sensing manager in Schneider Electric Technology Strategy Department in Grenoble, France.

Use of Highly Energy Efficient Nanotechnologies in Active Implantable Medical Devices

R. Dal Molin
Director of Scientific and Technical Coordination
SORIN CRM, Clamart, France

Abstract
More than 1 000 000 pacemakers and more than 200 000 defibrillators are implanted in the world each year. More than 200 000 Infusion pumps for diabetes and pain are implanted per year. Neurodevices for pain management, epilepsy, Parkinson and many others are growing rapidly currently more than 150 000 are implanted each year. In 2010, 219 000 people worldwide had cochlear devices implanted. In the U.S alone some 900 000 people are believed to be deaf or near deaf. In India, there are an estimated 1 million profoundly deaf children; only about 5,000 have cochlear implants.
All these devices are battery operated rechargeable or non rechargeable.
The most critical are the non-rechargeable one, which should operate at least 10 years to avoid multiple surgeries. To increase the longevity of these devices minimal power consumption circuits have to be designed. In the presentation we will discuss the designs and technologies used for such devices.

CV of presenting author
Renzo Dal Molin is the Director of Scientific and Technical Coordination for SORIN CRM (Cardiac Rhythm Management), which is a business unit of SORIN GROUP.
He is responsible for research mainly conducted in
European projects.
His scope is to bring innovation in pacemakers, implantable sensors and defibrillators, active implantable medical devices communication and home monitoring systems.
He is Vice Chairman of EPoSS,(European Technology Platform
on Smart Systems) Chairman of Working Groups Smart Systems
for Healthy Living and Applied Micro-Nano-Bio Systems.
He is very active in telecommunication standardization as
he was involved in ECC reports 149 and 150 published by the European Communications Office and rapporteur of ETSI
standards EN 301 559 and EN 301 489-35. He is Project Coordinator or SORIN CRM responsible for European or national projects.
He has a 34 years experience in bioelectronics, ASIC design, Microelectronics Packaging, Interconnect and Assembly.
He obtained his master in Electronics and Biomedical Engineering in 1979 from ESSTIN and University of Nancy
France.
He then occupied in SORIN CRM different positions like

hardware & software project engineer, pacemaker & defibrillator project manager, MEMS analog&digital integrated circuits design manager.
He holds more than 20 US and European patents.